

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

NLAS4052

Analog Multiplexer/ Demultiplexer

Double-Pole, 4-Position Plus Common Off

The NLAS4052 is an improved version of the MC14052 and MC74HC4052 fabricated in sub-micron Silicon Gate CMOS technology for lower $R_{DS(on)}$ resistance and improved linearity with low current. This device may be operated either with a single supply or dual supply up to ± 3 V to pass a 6 V_{PP} signal without coupling capacitors.

When operating in single supply mode, it is only necessary to tie V_{EE} , pin 7 to ground. For dual supply operation, V_{EE} is tied to a negative voltage, not to exceed maximum ratings.

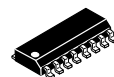
- Improved $R_{DS(on)}$ Specifications
- Pin for Pin Replacement for MAX4052 and MAX4052A
 - One Half the Resistance Operating at 5.0 Volts
- Single or Dual Supply Operation
 - Single 2.5–5 Volt Operation, or Dual ± 3 Volt Operation
 - With V_{CC} of 3.0 to 3.3 V, Device Can Interface with 1.8 V Logic, No Translators Needed
 - Address and Inhibit pins are Logic is Over-Voltage Tolerant and May Be Driven Up +6 V Regardless of V_{CC}
- Address and Inhibit pins are Standard TTL Compatible
 - Greatly Improved Noise Margin Over MAX4052 and MAX4052A
- Improved Linearity Over Standard HC4052 Devices
- Popular SOIC, and Space Saving TSSOP, and QSOP 16 Pin Packages



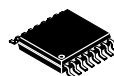
ON Semiconductor®

<http://onsemi.com>

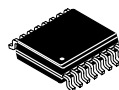
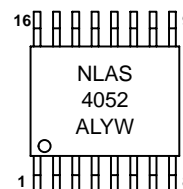
MARKING DIAGRAMS



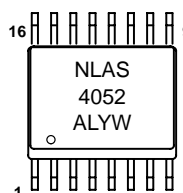
SO-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



QSOP-16
QS SUFFIX
CASE 492



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NLAS4052DR2	SO-16	2500 Units/Reel
NLAS4052DTR2	TSSOP-16	2500 Units/Reel
NLAS4052QSR	QSOP-16	2500 Units/Reel

NLAS4052

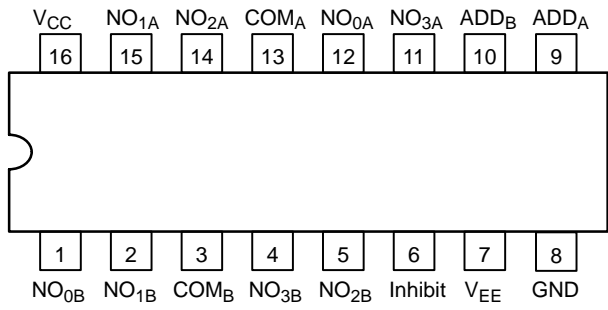


Figure 1. Pin Connection
(Top View)

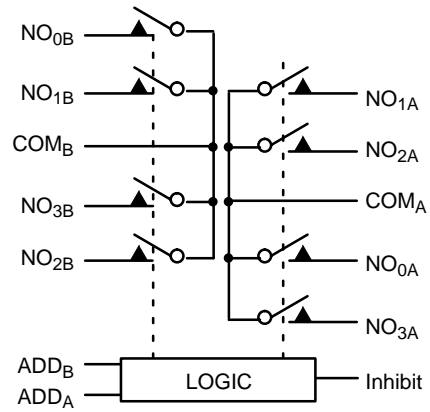


Figure 2. Logic Diagram

TRUTH TABLE

Inhibit	Address		ON SWITCHES*
	B	A	
1	X don't care	X don't care	All switches open
0	0	0	COM _A -NO _{0A} , COM _B -NO _{0B}
0	0	1	COM _A -NO _{1A} , COM _B -NO _{1B}
0	1	0	COM _A -NO _{2A} , COM _B -NO _{2B}
0	1	1	COM _A -NO _{3A} , COM _B -NO _{3B}

*NO and COM pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

NLAS4052

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit	
V _{EE}	Negative DC Supply Voltage (Referenced to GND)	-7.0 to +0.5	V	
V _{CC}	Positive DC Supply Voltage (Note 2) (Referenced to GND) (Referenced to V _{EE})	-0.5 to +7.0 -0.5 to +7.0	V	
V _{IS}	Analog Input Voltage	V _{EE} -0.5 to V _{CC} +0.5	V	
V _{IN}	Digital Input Voltage (Referenced to GND)	-0.5 to 7.0	V	
I	DC Current, Into or Out of Any Pin	± 50	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C	
T _J	Junction Temperature under Bias	+150	°C	
θ _{JA}	Thermal Resistance	SOIC TSSOP QSOP	143 164 164	°C/W
P _D	Power Dissipation in Still Air,	SOIC TSSOP QSOP	500 450 450	mW
MSL	Moisture Sensitivity	Level 1		
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in		
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 200 > 1000	V	
I _{LATCH-UP}	Latch-Up Performance Above V _{CC} and Below GND at 125°C (Note 6)	± 300	mA	

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. The absolute value of V_{CC} ± |V_{EE}| ≤ 7.0.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{EE}	Negative DC Supply Voltage (Referenced to GND)	-5.5	GND	V
V _{CC}	Positive DC Supply Voltage (Referenced to GND) (Referenced to V _{EE})	2.5 2.5	5.5 6.6	V
V _{IS}	Analog Input Voltage	V _{EE}	V _{CC}	V
V _{IN}	Digital Input Voltage (Note 7) (Referenced to GND)	0	5.5	V
T _A	Operating Temperature Range, All Package Types	-55	125	°C
t _r , t _f	Input Rise/Fall Time (Channel Select or Enable Inputs) V _{CC} = 3.0 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

7. Unused digital inputs may not be left open. All digital inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

NLAS4052

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V _{CC}	Guaranteed Max Limit			Unit
				-55 to 25°C	<85°C	<125°C	
V _{IH}	Minimum High-Level Input Voltage, Enable Inputs		2.5	1.75	1.75	1.75	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			5.5	3.85	3.85	3.85	
V _{IL}	Maximum Low-Level Input Voltage, Enable Inputs		2.5	0.45	0.45	0.45	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			5.5	1.65	1.65	1.65	
I _{IN}	Maximum Input Leakage Current, Address or Inhibit Inputs	V _{IN} = 6.0 or GND	0 V to 6.0 V	±0.1	±1.0	±1.0	µA
I _{CC}	Maximum Quiescent Supply Current (per Package)	Address, Inhibit and V _{IS} = V _{CC} or GND	6.0	4.0	40	80	µA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit			Unit
					-55 to 25°C	≤ 85°C	≤ 125°C	
R _{ON}	Maximum "ON" Resistance (Note 8)	V _{IN} = V _{IL} or V _{IH} V _{IS} = V _{EE} to V _{CC} I _S = 10 mA (Figures 4 thru 9)	3.0	0	86	108	120	Ω
			4.5	0	37	46	55	
			3.0	-3.0	26	33	37	
ΔR _{ON}	Maximum Difference in "ON" Resistance Between Any Two Channels in the Same Package	V _{IN} = V _{IL} or V _{IH} , V _{IS} = 2.0 V V _{IS} = 3.5 V I _S = 10 mA, V _{IS} = 2.0 V	3.0	0	15	20	20	Ω
			4.5	0	13	18	18	
			3.0	-3.0	10	15	15	
R _{flat(ON)}	ON Resistance Flatness	I _S = 10 mA V _{com} 1, 2, 3.5 V V _{com} -2, 0, 2 V	4.5	0	4	4	5	Ω
			3.0	-3.0	2	2	3	
I _{NC(OFF)} I _{NO(OFF)}	Maximum Off-Channel Leakage Current	Switch Off V _{IN} = V _{IL} or V _{IH} V _{IO} = V _{CC} -1.0 V or V _{EE} +1.0 V (Figure 17)	6.0	0	0.1	5.0	100	nA
			3.0	-3.0	0.1	5.0	100	
I _{COM(ON)}	Maximum On-Channel Leakage Current, Channel-to-Channel	Switch On V _{IO} = V _{CC} -1.0 V or V _{EE} +1.0 V (Figure 17)	6.0	0	0.1	5.0	100	nA
			3.0	-3.0	0.1	5.0	100	

8. At supply voltage (V_{CC}) approaching 2.5 V the analog switch on-resistance becomes extremely non-linear. Therefore, for low voltage operation it is recommended that these devices only be used to control digital signals.

NLAS4052

AC CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Conditions	V _{CC} V	V _{EE} V	Guaranteed Limit				Unit
					-55 to 25°C		≤ 85°C	≤ 125°C	
					Min	Typ*			
t _{BBM}	Minimum Break-Before-Make Time	V _{IN} = V _{IL} or V _{IH} V _{IS} = V _{CC} R _L = 300 Ω, C _L = 35 pF (Figure 19)	3.0	0.0	1.0	6.5	–	–	ns
			4.5	0.0	1.0	5.0	–	–	
			3.0	–3.0	1.0	3.5	–	–	

*Typical Characteristics are at 25°C.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f = 3$ ns)

Symbol	Parameter	V _{CC} V	V _{EE} V	Guaranteed Limit						Unit	
				-55 to 25°C			≤ 85°C		≤ 125°C		
				Min	Typ	Max	Min	Max	Min		Max
t _{TRANS}	Transition Time (Address Selection Time) (Figure 18)	2.5	0		22	40		45		50	ns
		3.0	0		20	28		30		35	
		4.5	0		16	23		25		30	
		3.0	–3.0		16	23		25		28	
t _{ON}	Turn-on Time (Figures 14, 15, 20, and 21) Inhibit to N _O or N _C	2.5	0		22	40		45		50	ns
		3.0	0		20	28		30		35	
		4.5	0		16	23		25		30	
		3.0	–3.0		16	23		25		28	
t _{OFF}	Turn-off Time (Figures 14, 15, 20, and 21) Inhibit to N _O or N _C	2.5	0		22	40		45		50	ns
		3.0	0		20	28		30		35	
		4.5	0		16	23		25		30	
		3.0	–3.0		16	23		25		28	

		Typical @ 25°C, V _{CC} = 5.0 V		
C _{IN}	Maximum Input Capacitance, Select Inputs	8		pF
C _{NO} or C _{NC}	Analog I/O	10		
C _{COM}	Common I/O	10		
C _(ON)	Feedthrough	1.0		

NLAS4052

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V _{CC} V	V _{EE} V	Typ	Unit
					25°C	
BW	Maximum On-Channel Bandwidth or Minimum Frequency Response	V _{IS} = ½ (V _{CC} - V _{EE}) Source Amplitude = 0 dBm (Figures 10 and 22)	3.0	0.0	110	MHz
			4.5	0.0	130	
			6.0	0.0	140	
			3.0	-3.0	140	
V _{ISO}	Off-Channel Feedthrough Isolation	f = 100 kHz; V _{IS} = ½ (V _{CC} - V _{EE}) Source = 0 dBm (Figures 12 and 22)	3.0	0.0	-93	dB
			4.5	0.0	-93	
			6.0	0.0	-93	
			3.0	-3.0	-93	
V _{ONL}	Maximum Feedthrough On Loss	V _{IS} = ½ (V _{CC} - V _{EE}) Source = 0 dBm (Figures 10 and 22)	3.0	0.0	-2	dB
			4.5	0.0	-2	
			6.0	0.0	-2	
			3.0	-3.0	-2	
Q	Charge Injection	V _{IN} = V _{CC} to V _{EE} , f _{IS} = 1 kHz, t _r = t _f = 3 ns R _{IS} = 0 Ω, C _L = 1000 pF, Q = C _L * ΔV _{OUT} (Figures 16 and 23)	5.0	0.0	9.0	pC
			3.0	-3.0	12	
THD	Total Harmonic Distortion THD + Noise	f _{IS} = 1 MHz, R _L = 10 KΩ, C _L = 50 pF, V _{IS} = 5.0 V _{PP} sine wave V _{IS} = 6.0 V _{PP} sine wave (Figure 13)	6.0	0.0	0.10	%
			3.0	-3.0	0.05	

NLAS4052

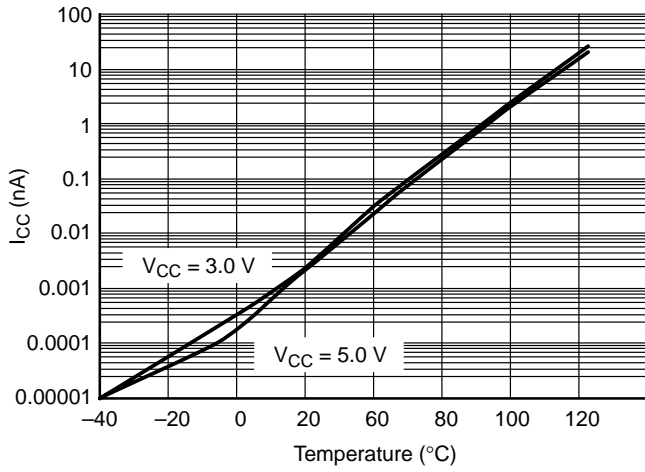


Figure 3. I_{CC} versus Temp, $V_{CC} = 3\text{ V}$ and 5 V

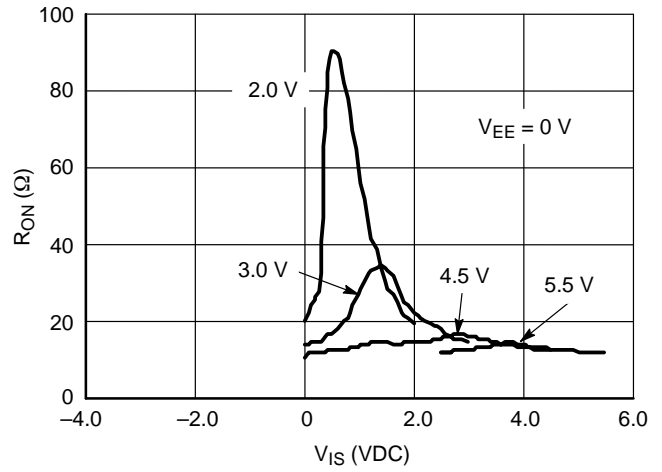


Figure 4. R_{ON} versus V_{CC} , Temp = 25°C

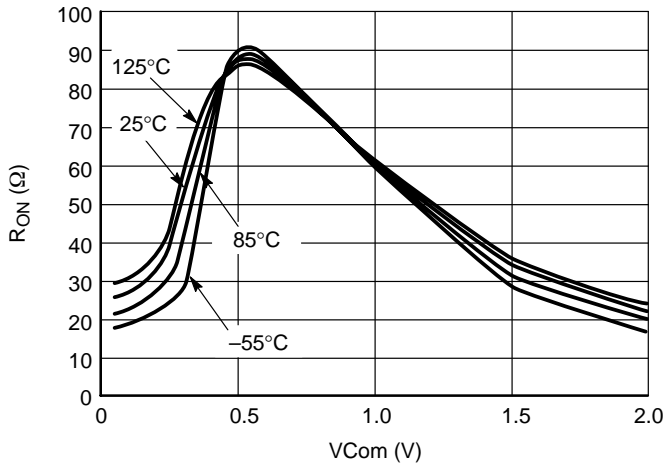


Figure 5. Typical On Resistance
 $V_{CC} = 2.0\text{ V}$, $V_{EE} = 0\text{ V}$

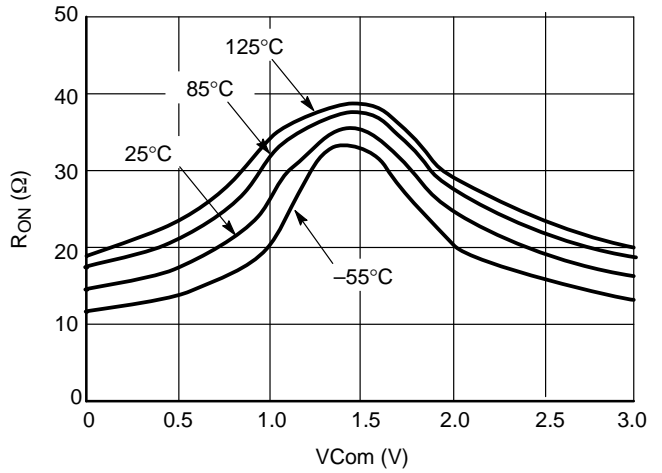


Figure 6. Typical On Resistance
 $V_{CC} = 3.0\text{ V}$, $V_{EE} = 0\text{ V}$

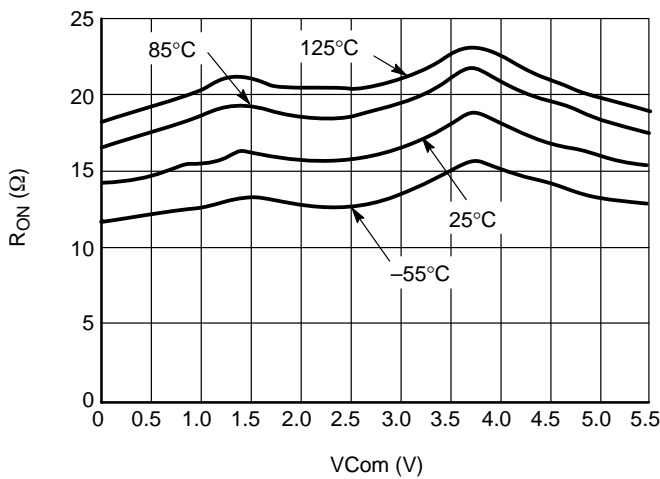


Figure 7. Typical On Resistance
 $V_{CC} = 4.5\text{ V}$, $V_{EE} = 0\text{ V}$

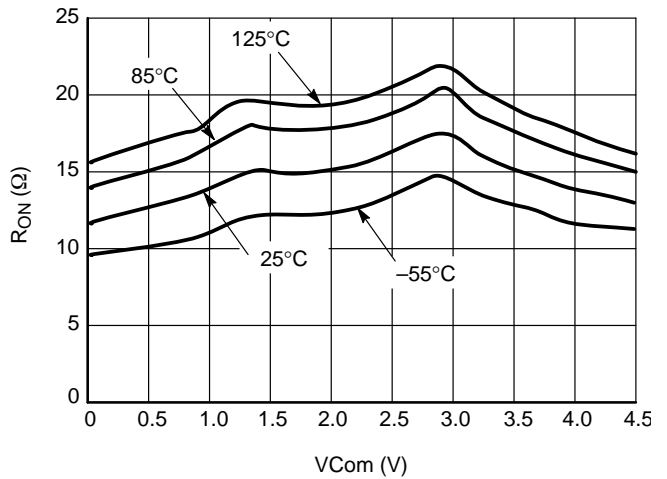


Figure 8. Typical On Resistance
 $V_{CC} = 5.5\text{ V}$, $V_{EE} = 0\text{ V}$

NLAS4052

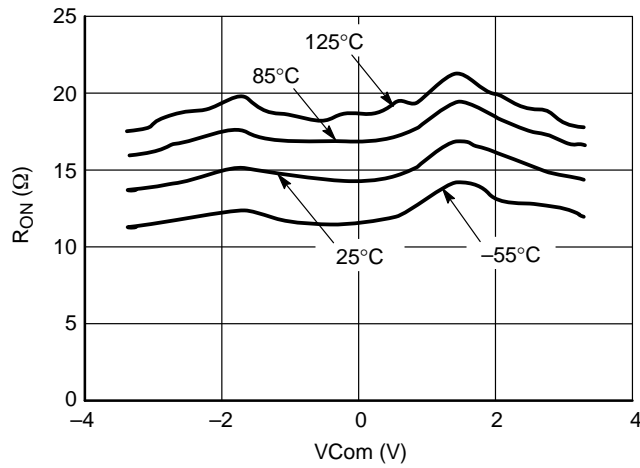


Figure 9. Typical On Resistance
 $V_{CC} = 3.3\text{ V}, V_{EE} = -3.3\text{ V}$

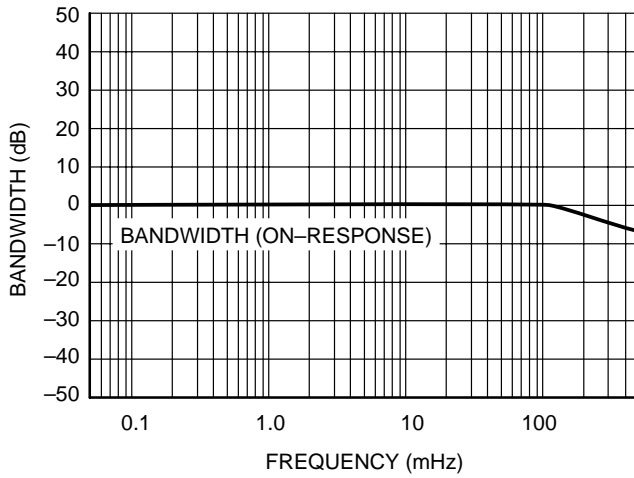


Figure 10. Bandwidth, $V_{CC} = 5.0\text{ V}$

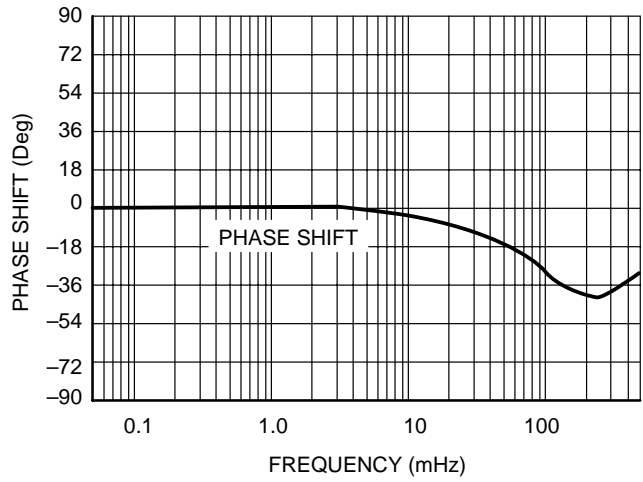


Figure 11. Phase Shift, $V_{CC} = 5.0\text{ V}$

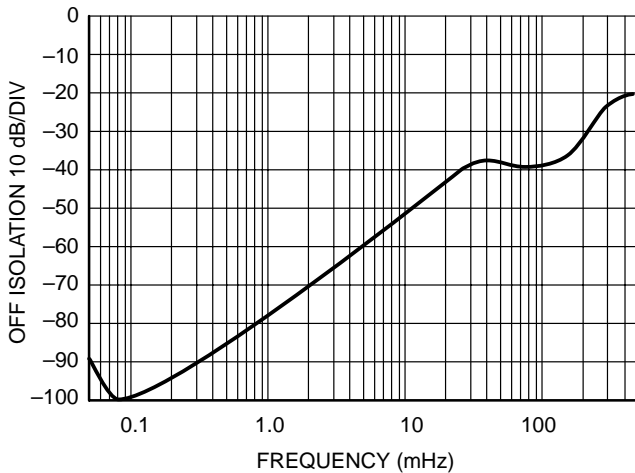


Figure 12. Off Isolation, $V_{CC} = 5.0\text{ V}$

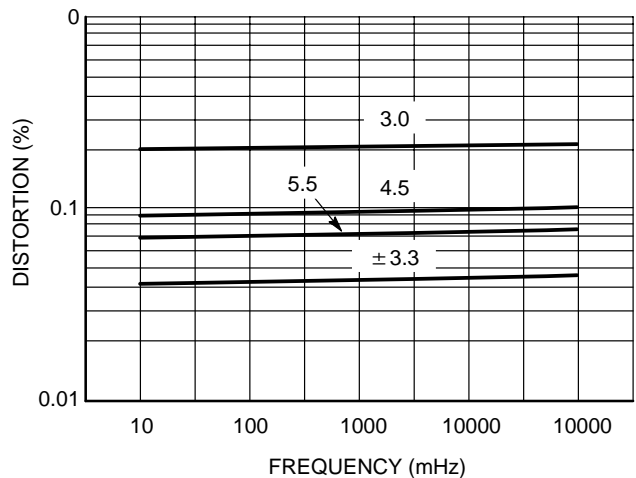


Figure 13. Total Harmonic Distortion

NLAS4052

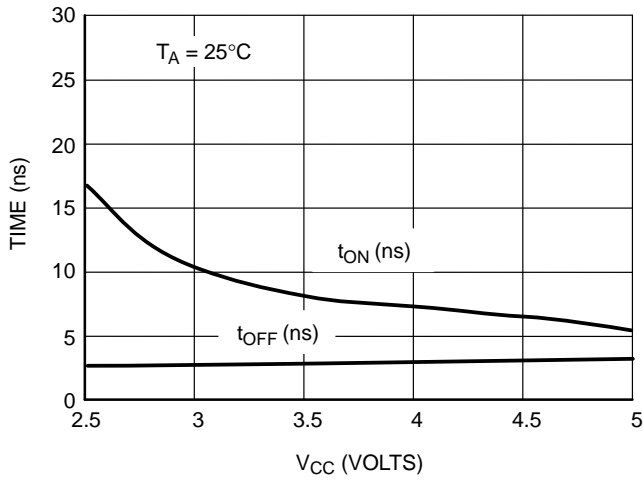


Figure 14. t_{ON} and t_{OFF} versus V_{CC}

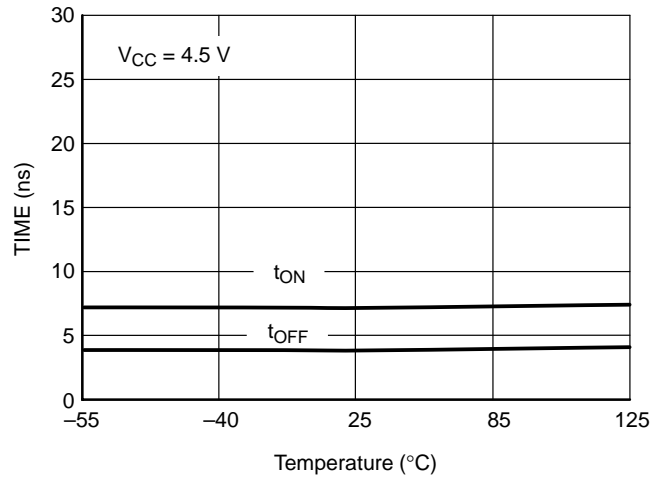


Figure 15. t_{ON} and t_{OFF} versus Temp

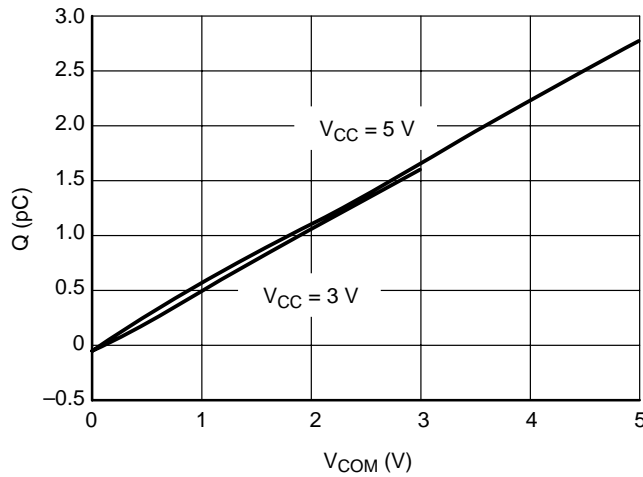


Figure 16. Charge Injection versus COM Voltage

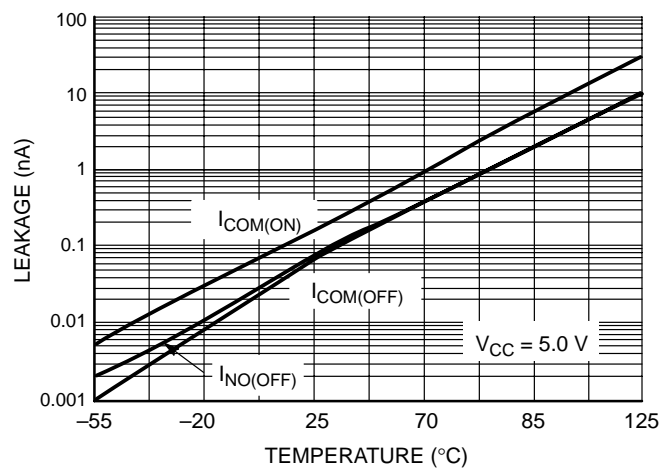


Figure 17. Switch Leakage versus Temperature

NLAS4052

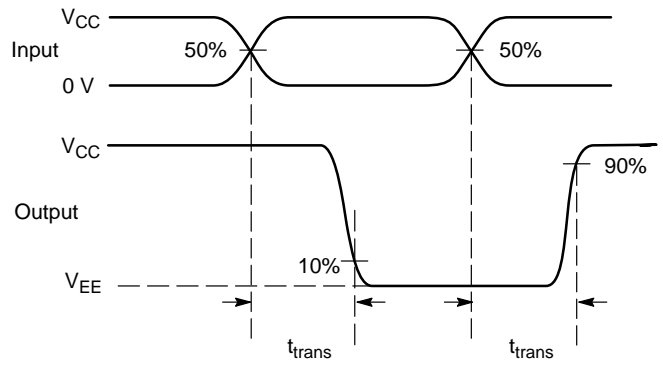
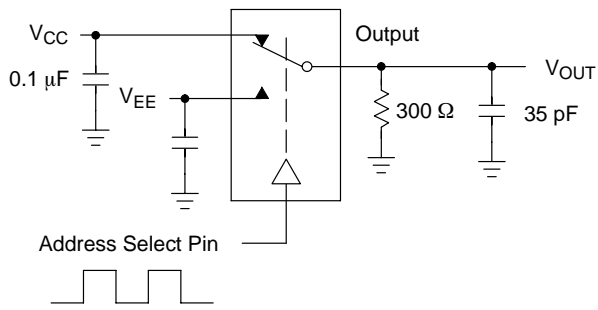


Figure 18. Channel Selection Propagation Delay

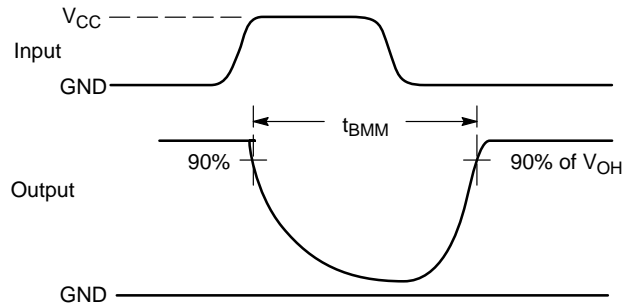
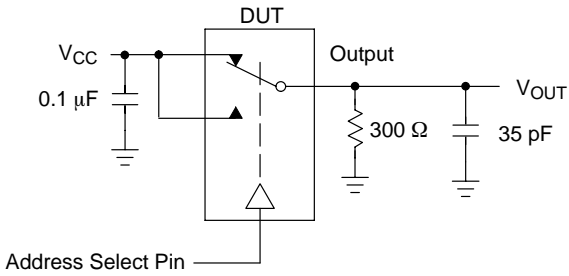


Figure 19. t_{BMM} (Time Break-Before-Make)

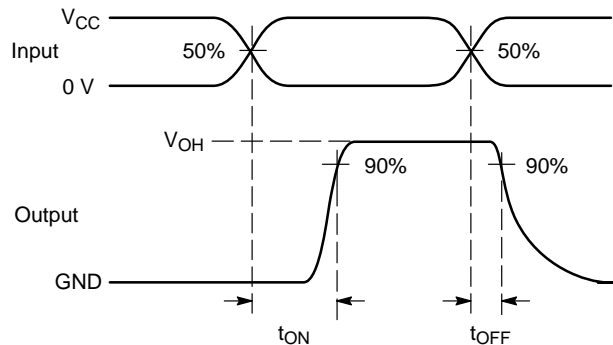
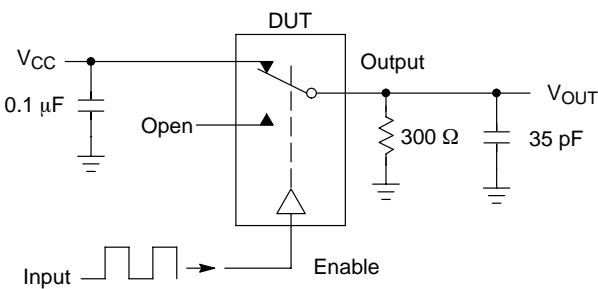


Figure 20. $t_{\text{ON}}/t_{\text{OFF}}$

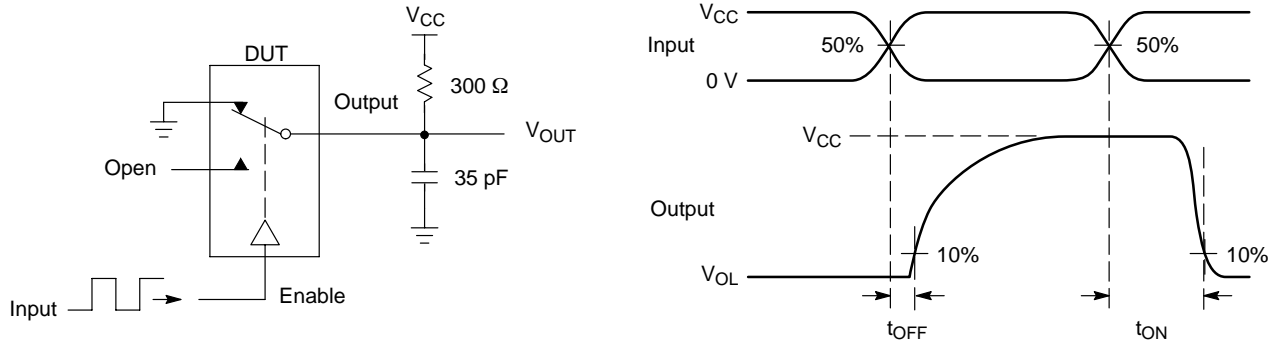
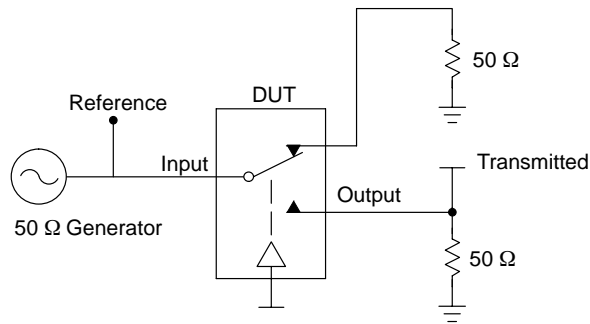


Figure 21. t_{ON}/t_{OFF}



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 22. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

NLAS4052

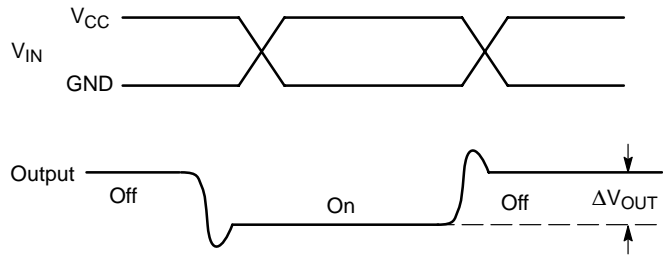
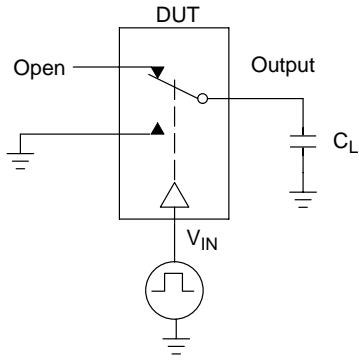


Figure 23. Charge Injection: (Q)

TYPICAL OPERATION

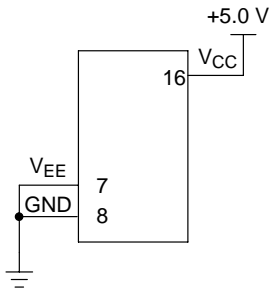


Figure 24. 5.0 Volts Single Supply
 $V_{CC} = 5.0\text{ V}$, $V_{EE} = 0$

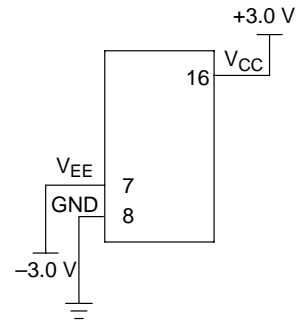


Figure 25. Dual Supply
 $V_{CC} = 3.0\text{ V}$, $V_{EE} = -3.0\text{ V}$

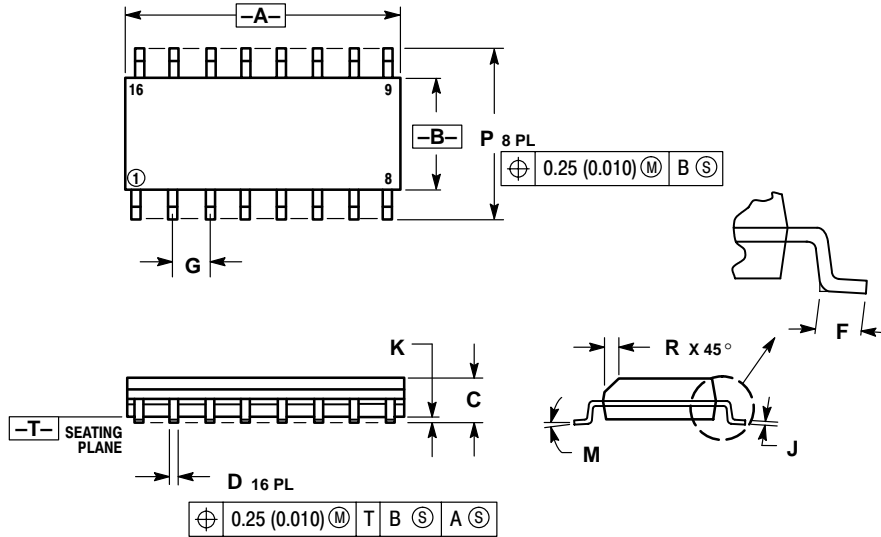
DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature					Package Type	Tape & Reel Size
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAS4052DR2	NL	AS	4052	D	R2	SO	2500 Unit Reel
NLAS4052DTR2	NL	AS	4052	DT	R2	TSSOP	2500 Unit Reel
NLAS4052QSR	NL	AS	4052	QS	R	QSOP	2500 Unit Reel

NLAS4052

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE J



NOTES:

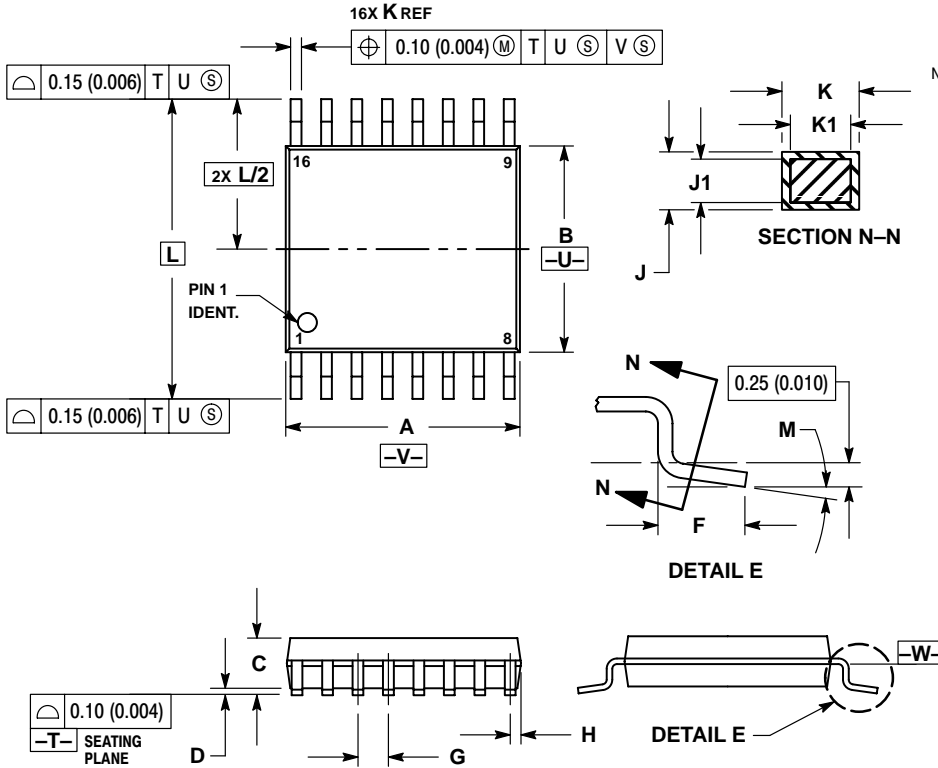
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NLAS4052

PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE O



NOTES:

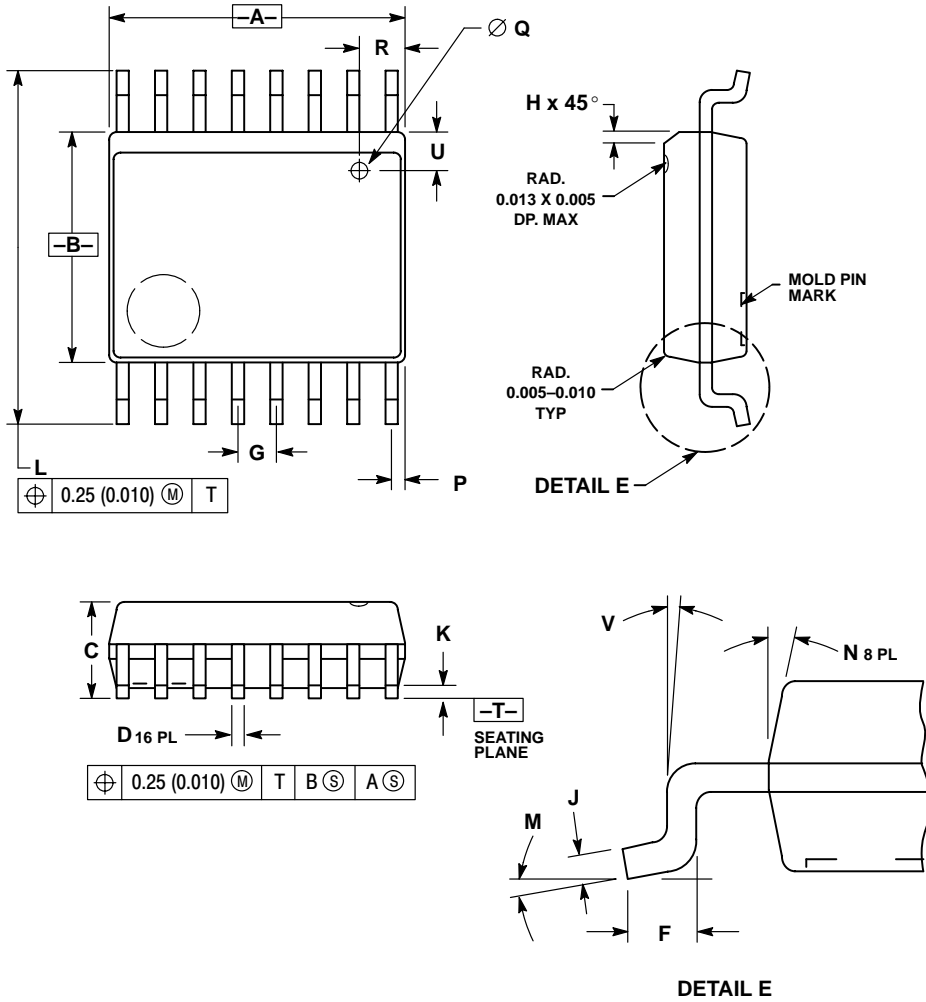
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

NLAS4052


PACKAGE DIMENSIONS

QSOP-16
 QS SUFFIX
 CASE 492-01
 ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
 4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
 5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
V	0°	8°	0°	8°

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.