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FAIRCHILD SEMICONDUCTOR®

May 2007

74VHC4316
Quad Analog Switch with Level Translator

Features

- Typical switch enable time: 20ns
- Wide analog input voltage range: ±6V
- Low "ON" resistance: 50 Typ. (V_{CC}–V_{EE} = 4.5V)
  30 Typ. (V_{CC}–V_{EE} = 9V)
- Low quiescent current: 80μA maximum (74VHC)
- Matched switch characteristics
- Individual switch controls plus a common enable
- Pin functional compatible with 74HC4316

General Description

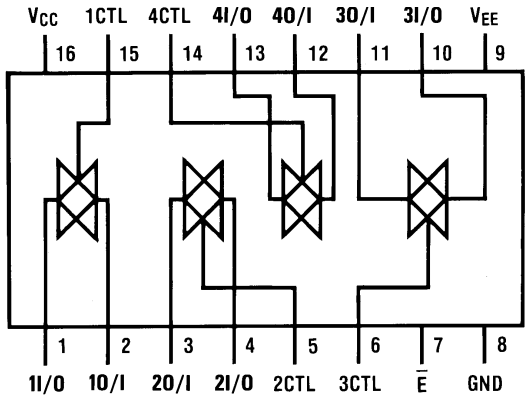
These devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the 4316 to implement a level translator which enables this circuit to operate with 0V–6V logic levels and up to ±6V analog switch levels. The 4316 also has a common enable input in addition to each switch's control which when HIGH will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Ordering Information

Order Number	Package Number	Package Description
74VHC4316M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC4316WM	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC4316MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering number.

Connection Diagram

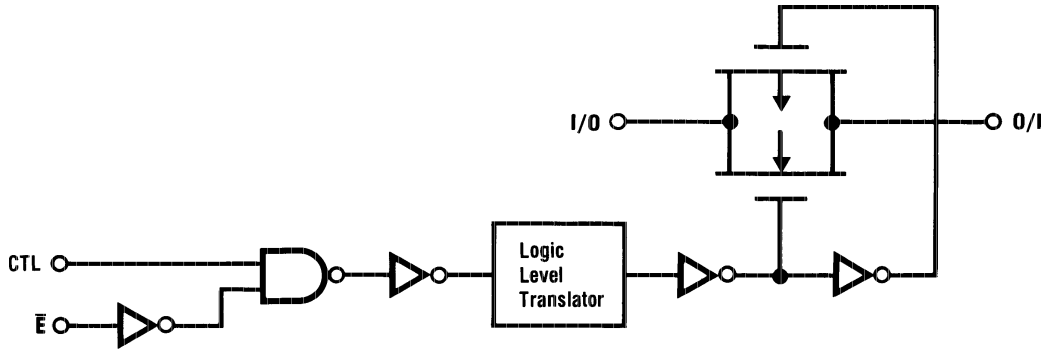


Top View

Truth Table

Inputs		Switch
$\overline{E}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Logic Diagram



Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.5V
V_{EE}	Supply Voltage	+0.5 to –7.5V
V_{IN}	DC Control Input Voltage	–1.5 to V_{CC}+1.5V
V_{IO}	DC Switch I/O Voltage	V_{EE}–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation S.O. Package only	600mW 500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Note:

1. Unless otherwise specified all voltages are referenced to ground.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{EE}	Supply Voltage	0	–6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0V V_{CC} = 4.5V V_{CC} = 6.0V V_{CC} = 12.0V		 1000 500 400 250	 ns

DC Electrical Characteristics[2]

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	T_A = –40°C to +85°C		Units
					Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage			2.0V		1.5	1.5	V
				4.5V		3.15	3.15	
				6.0V		4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage			2.0V		0.5	0.5	V
				4.5V		1.35	1.35	
				6.0V		1.8	1.8	
R_{ON}	Minimum "ON" Resistance[3]	$V_{CTL} = V_{IH}$, I_S = 2.0mA, $V_{IS} = V_{CC}$ to V_{EE}, (Fig. 1)	GND	4.5V	100	170	200	Ω
			–4.5V	4.5V	40	85	105	
			–6.0V	6.0V	30	70	85	
		$V_{CTL} = V_{IH}$, I_S = 2.0mA, $V_{IS} = V_{CC}$ or V_{EE} (Fig. 1)	GND	2.0V	100	180	215	
			GND	4.5V	40	80	100	
			–4.5V	4.5V	50	60	75	
			–6.0V	6.0V	20	40	60	
R_{ON}	Maximum "ON" Resistance Matching	$V_{CTL} = V_{IH}$, $V_{IS} = V_{CC}$ to V_{EE}	GND	4.5V	10	15	20	Ω
			–4.5V	4.5V	5	10	15	
			–6.0V	6.0V	5	10	15	
I_{IN}	Maximum Control Input Current	$V_{IN} = V_{CC}$ or GND	GND	6.0V		±0.1	±1.0	µA
I_{IZ}	Maximum Switch "OFF" Leakage Current	$V_{OS} = V_{CC}$ or V_{EE}, $V_{IS} = V_{EE}$ or V_{CC}, $V_{CTL} = V_{IL}$ (Fig. 2)	GND	6.0V		±30	±300	nA
			–6.0V	6.0V		±50	±500	
I_{IZ}	Maximum Switch "ON" Leakage Current	$V_{IS} = V_{CC}$ to V_{EE}, $V_{CTL} = V_{IH}$, V_{OS} = OPEN (Fig. 3)	GND	6.0V		±20	±75	nA
			–6.0V	6.0V		±30	±150	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, I_{OUT} = 0 µA	GND	6.0V		1.0	10	µA
			–6.0V	6.0V		4.0	40	

Notes:

2. For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.
3. At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V – 6.0V, V_{EE} = 0V – 6V, C_L = 50 pF unless otherwise specified

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = +25°C		T_A = –40°C to +85°C	Units
					Typ.	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	3.3V	15	30	37	ns
			GND	4.5V	5	10	13	
			–4.5V	4.5V	4	8	12	
			–6.0V	6.0V	3	7	11	
t_{PZL}, t_{PZH}	Maximum Switch Turn “ON” Delay (Control)	R_L = 1kΩ	GND	3.3V	25	97	120	ns
			GND	4.5V	20	35	43	
			–4.5V	4.5V	15	32	39	
			–6.0V	6.0V	14	30	37	
t_{PHZ}, t_{PLZ}	Maximum Switch Turn “OFF” Delay (Control)	R_L = 1 kΩ	GND	3.3V	35	145	180	ns
			GND	4.5V	25	50	63	
			–4.5V	4.5V	20	44	55	
			–6.0V	6.0V	20	44	55	
t_{PZL}, t_{PZH}	Maximum Switch Turn “ON” Delay (Enable)		GND	3.3V	27	120	150	ns
			GND	4.5V	20	41	52	
			–4.5V	4.5V	19	38	48	
			–6.0V	6.0V	18	36	45	
t_{PLZ}, t_{PHZ}	Maximum Switch Turn “OFF” Delay (Enable)		GND	3.3V	42	155	190	ns
			GND	4.5V	28	53	67	
			–4.5V	4.5V	23	47	59	
			–6.0V	6.0V	21	47	59	
	Minimum Frequency Response (Fig. 7) 20 log (V_{OS}/V_{IS})= –3 dB	R_L = 600Ω, V_{IS} = $2V_{PP}$ at (V_{CC}–V_{EE}/2)[4][5]	0V	4.5	40			MHz
			–4.5V	4.5V	100			
	Control to Switch Feedthrough Noise (Fig. 8)	R_L = 600Ω, f = 1MHz C_L = 50pF[5][6]	0V	4.5V	100			mV
			–4.5V	4.5V	250			
	Crosstalk Between any Two Switches (Fig. 9)	R_L = 600Ω, f = 1MHz	0V	4.5V	–52			dB
			–4.5V	4.5V	–50			
	Switch OFF Signal Feedthrough Isolation (Fig. 10)	R_L = 600Ω, f = 1MHz, V_{CTL} = V_{IL}[5][6]	0V	4.5V	–42			dB
			–4.5V	4.5V	–44			
THD	Sinewave Harmonic Distortion	R_L = 10 KΩ, C_L = 50 pF, f = 1KHz V_{IS} = 4 V_{PP}	0V	4.5V	0.013			%
		V_{IS} = 8 V_{PP}	–4.5V	4.5V	0.008			
C_{IN}	Maximum Control Input Capacitance				5			pF
C_{IN}	Maximum Switch Input Capacitance				35			pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND			0.5			pF
C_{PD}	Power Dissipation Capacitance				15			pF

Notes:

4. Adjust 0 dBm for f = 1 kHz (Null R_L/Ron Attenuation).
5. V_{IS} is centered at V_{CC}–V_{EE}/2.
6. Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms

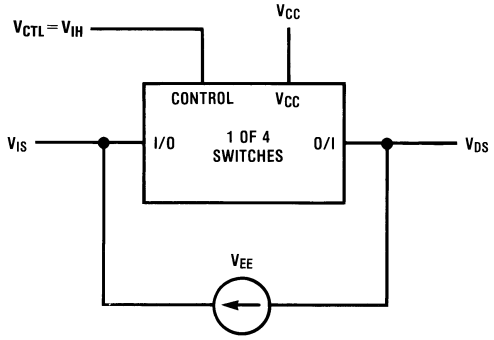


Figure 1. "ON" Resistance

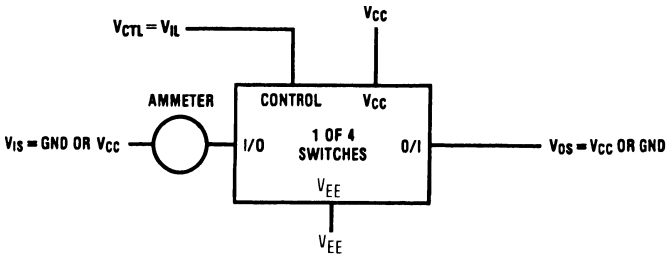


Figure 2. "OFF" Channel Leakage Current

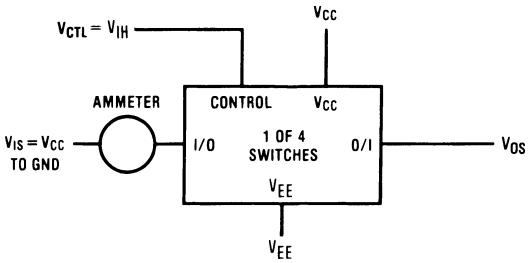


Figure 3. "ON" Channel Leakage Current

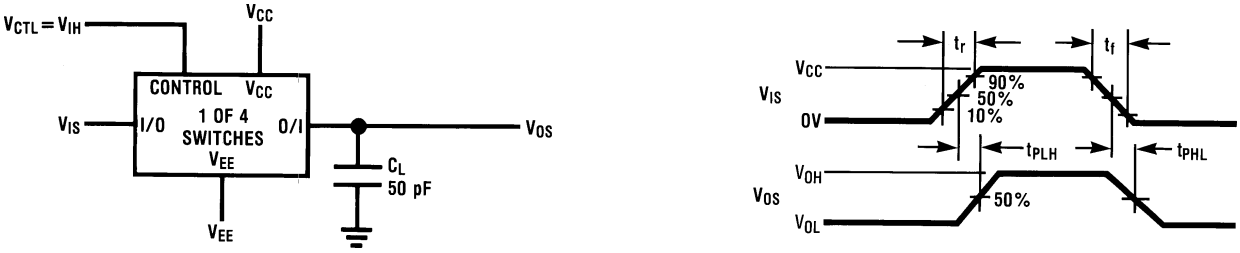


Figure 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

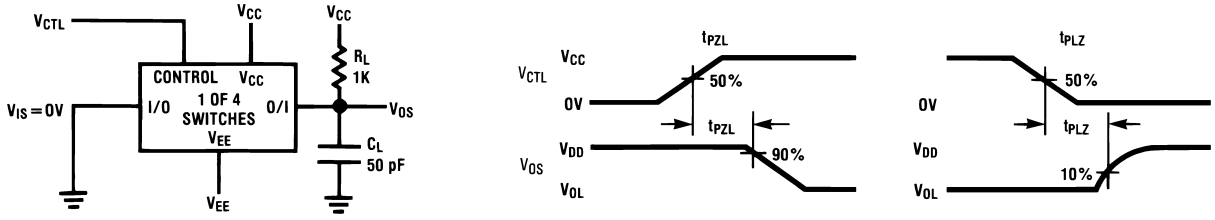


Figure 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

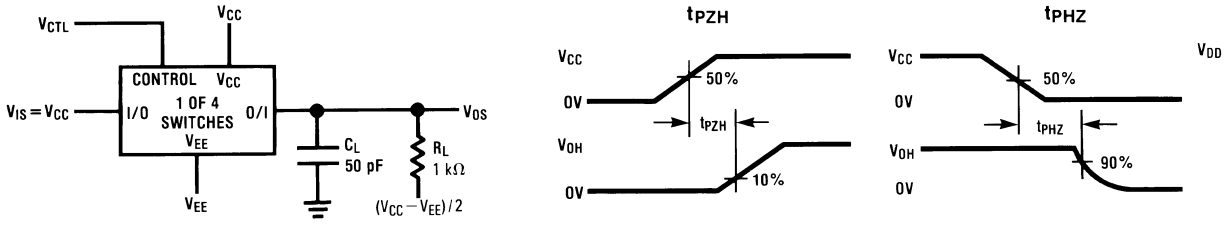


Figure 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

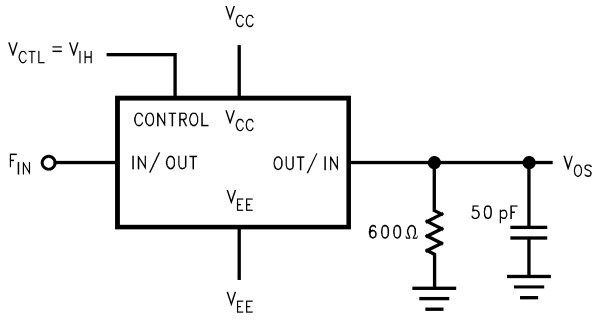


Figure 7. Frequency Response

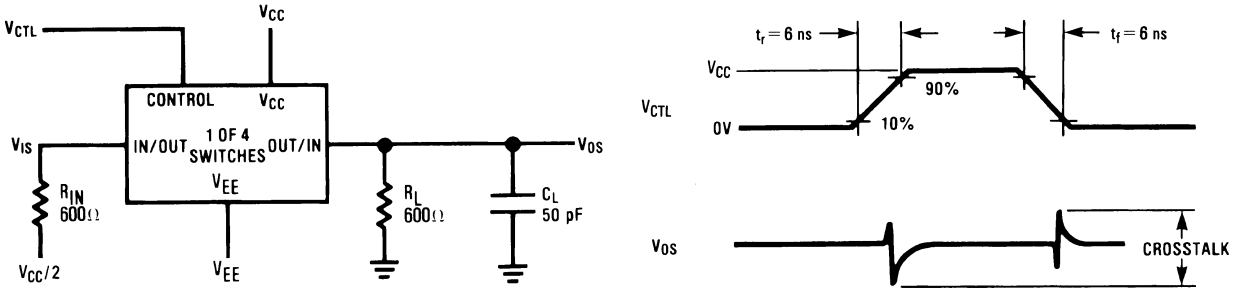


Figure 8. Crosstalk: Control Input to Signal Output

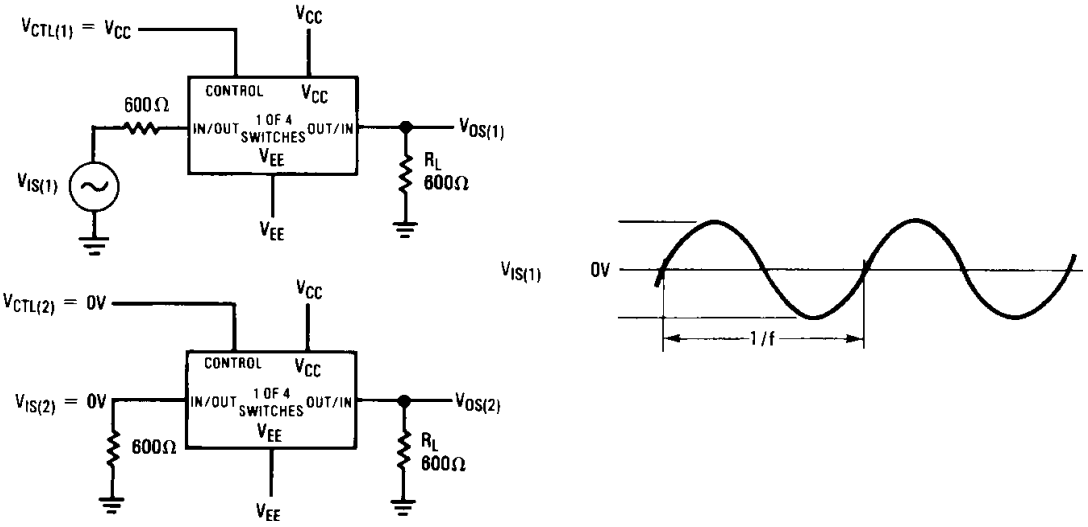


Figure 9. Crosstalk Between Any Two Switches

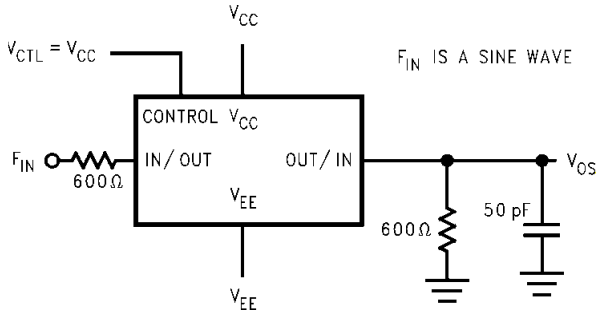


Figure 10. Switch OFF Signal Feedthrough Isolation

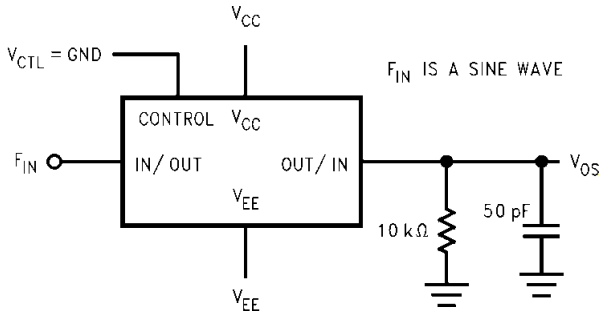
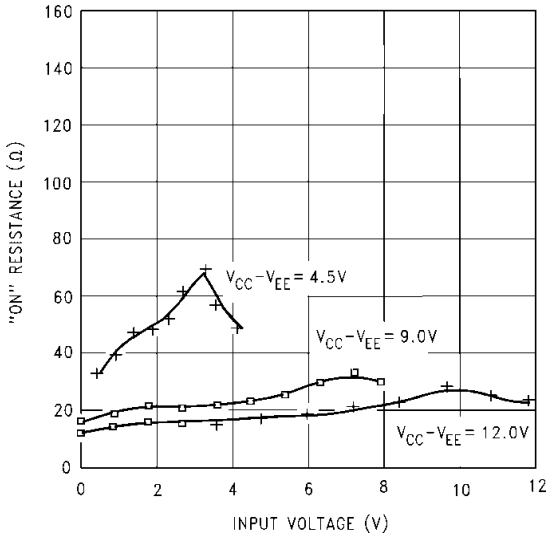


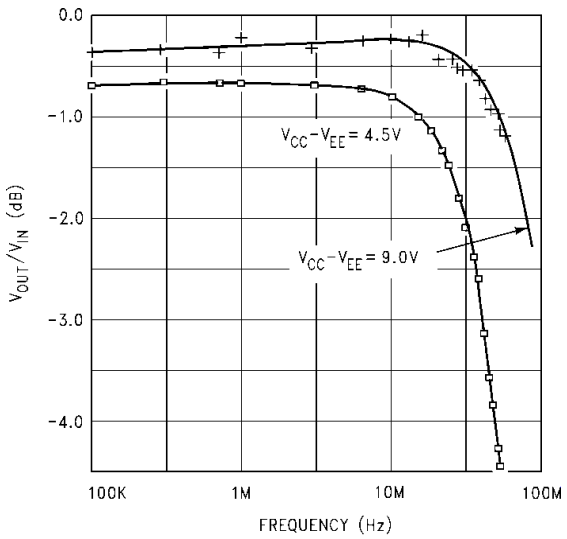
Figure 11. Sinewave Distortion

Typical Performance Characteristics

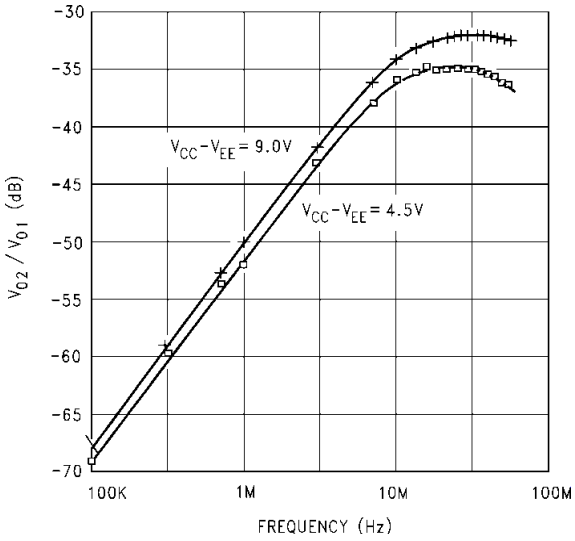
Typical "ON" Resistance



Typical Crosstalk Between Any Two Switches



Typical Frequency Response



Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

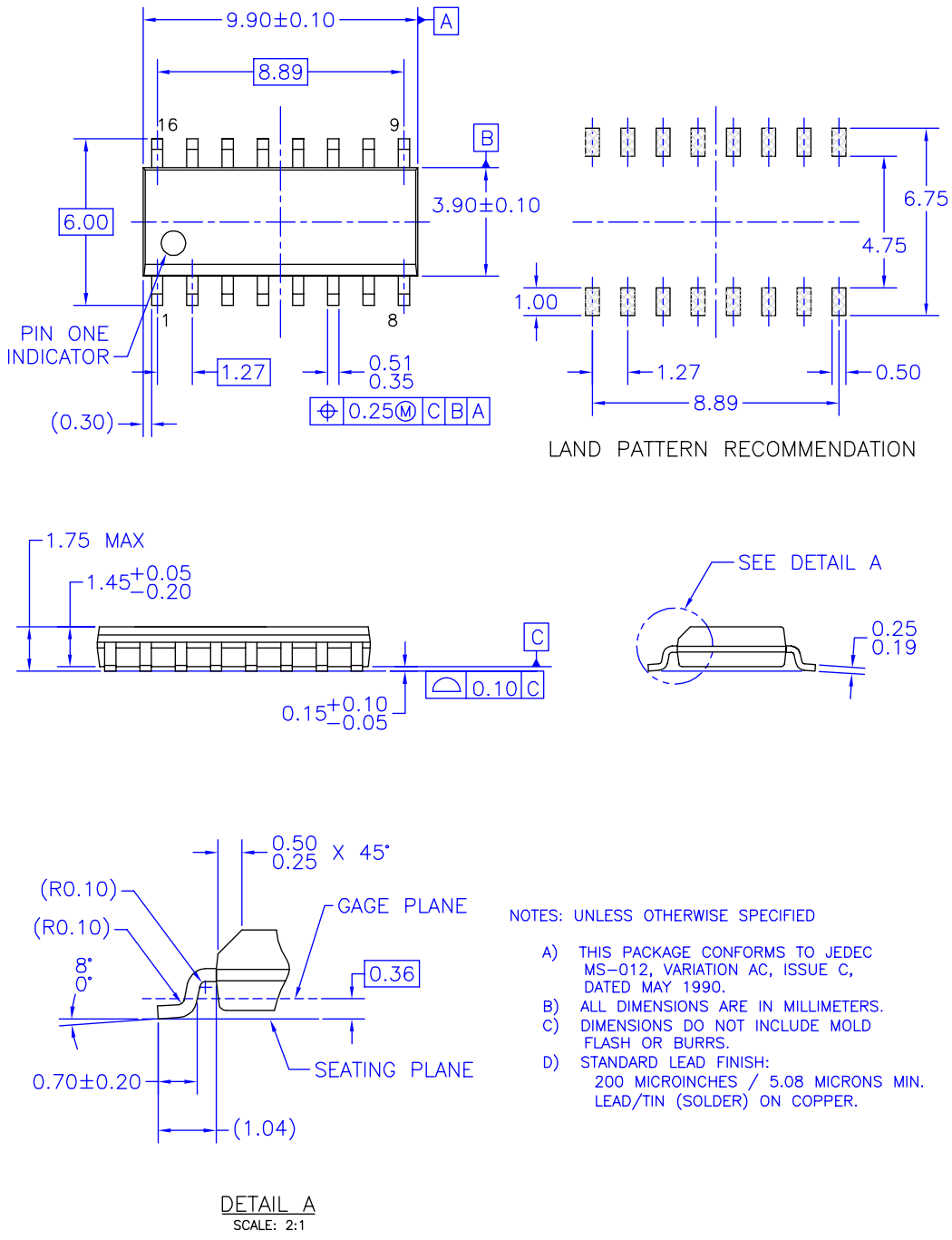


Figure 12. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

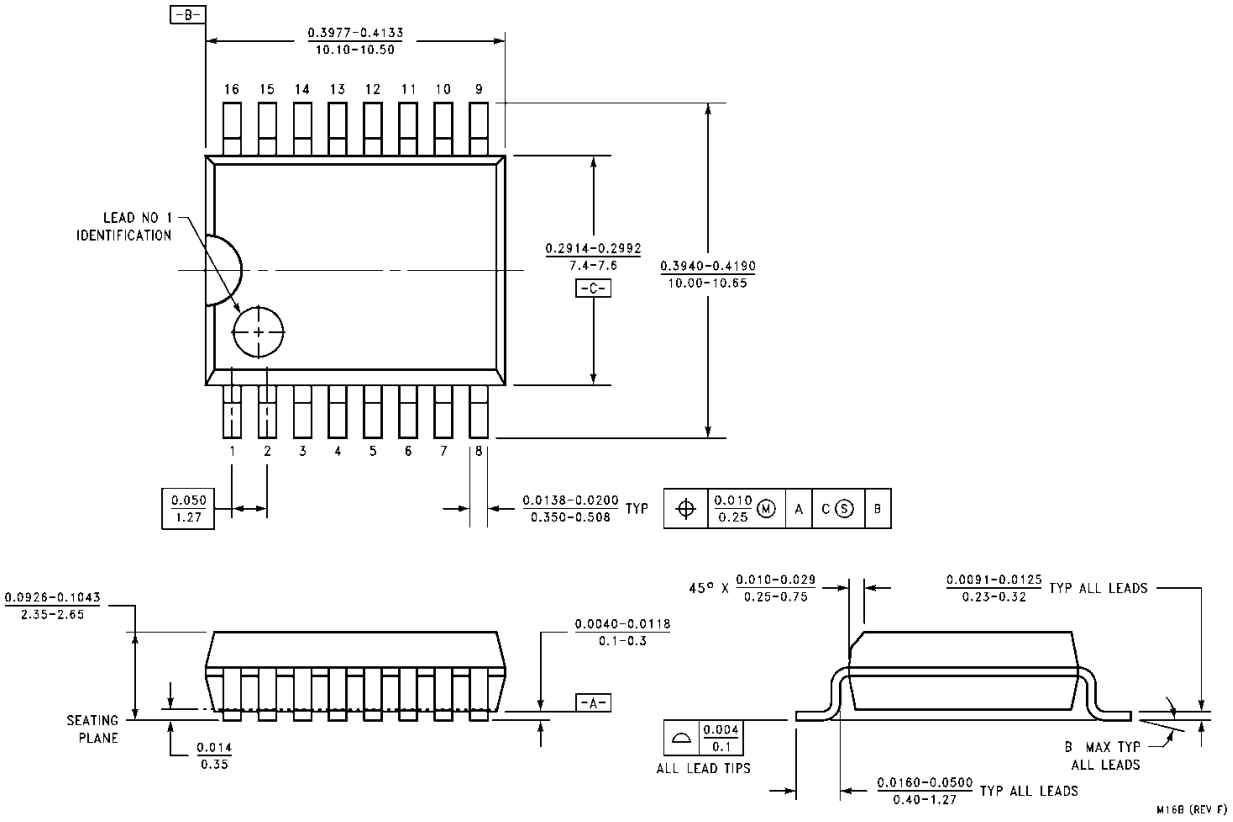
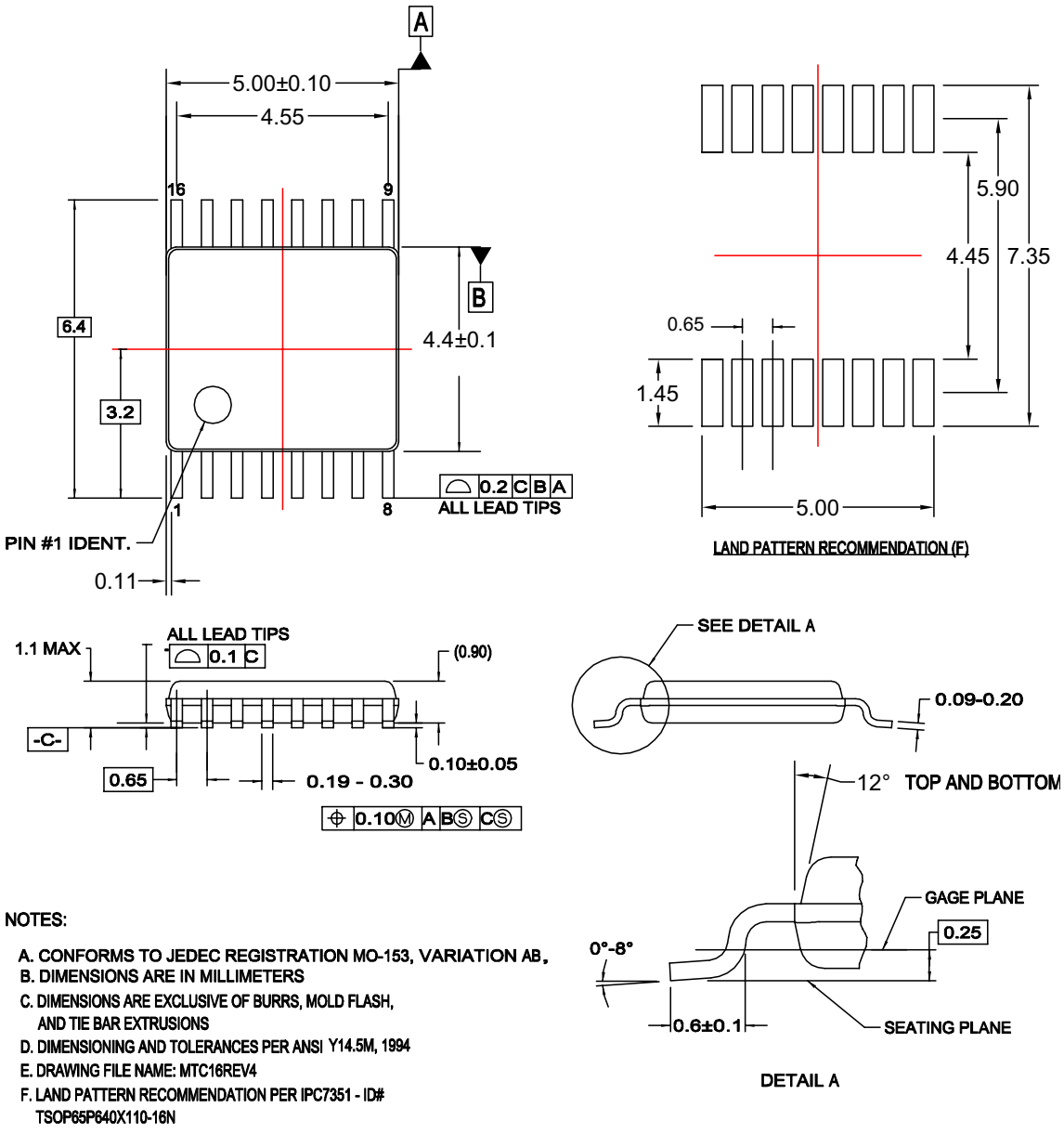


Figure 13. 16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M16B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB.
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 14. 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

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SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TCM™
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