

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

## 74VHC4066 Quad Analog Switch

### General Description

These devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the 4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The 4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to  $V_{CC}$  and ground.

### Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80  $\mu$ A maximum (74VHC)
- Matched switch characteristics
- Individual switch controls
- Pin and function compatible with the 74HC4066

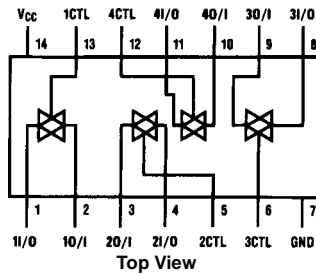
### Ordering Code:

| Order Number                 | Package Number | Package Description  |
|------------------------------|----------------|--|
| 74VHC4066M                   | M14A           | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow         |
| 74VHC4066MX_NL<br>(Note 1)   | M14A           | Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74VHC4066MTC                 | MTC14          | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide          |
| 74VHC4066MTCX_NL<br>(Note 1) | MTC14          | Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  |
| 74VHC4066N                   | N14A           | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide               |

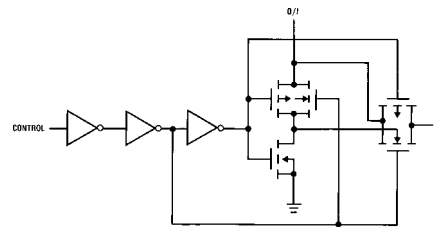
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC S-STD-020B). Device available in Tape and Reel only.

### Connection Diagram



### Schematic Diagram



### Truth Table

| Input | Switch  |
|-------|---------|
| CTL   | I/O–O/I |
| L     | "OFF"   |
| H     | "ON"    |

**Absolute Maximum Ratings** (Note 2)

(Note 3)

|  |                                   |
|--|-----------------------------------|
| Supply Voltage ( $V_{CC}$ )                          | -0.5 to +15V                      |
| DC Control Input Voltage ( $V_{IN}$ )                | -1.5 to $V_{CC} + 1.5V$           |
| DC Switch I/O Voltage ( $V_{IO}$ )                   | $V_{EE} - 0.5$ to $V_{CC} + 0.5V$ |
| Clamp Diode Current ( $I_{IK}, I_{OK}$ )             | $\pm 20$ mA                       |
| DC Output Current, per pin ( $I_{OUT}$ )             | $\pm 25$ mA                       |
| DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )     | $\pm 50$ mA                       |
| Storage Temperature Range ( $T_{STG}$ )              | -65°C to +150°C                   |
| Power Dissipation ( $P_D$ ) (Note 4)                 | 600 mW                            |
| S.O. Package only                                    | 500 mW                            |
| Lead Temperature ( $T_L$ )<br>(Soldering 10 seconds) | 260°C                             |

**Recommended Operating Conditions**

|   | Min | Max      | Units |
|---|-----|----------|-------|
| Supply Voltage ( $V_{CC}$ )                         | 2   | 12       | V     |
| DC Input or Output Voltage<br>( $V_{IN}, V_{OUT}$ ) | 0   | $V_{CC}$ | V     |
| Operating Temperature Range ( $T_A$ )               | -40 | +85      | °C    |
| Input Rise or Fall Times ( $t_r, t_f$ )             |     |          |       |
| $V_{CC} = 2.0V$                                     |     | 1000     | ns    |
| $V_{CC} = 4.5V$                                     |     | 500      | ns    |
| $V_{CC} = 9.0V$                                     |     | 400      | ns    |

**Note 2:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 3:** Unless otherwise specified all voltages are referenced to ground.

**Note 4:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

**DC Electrical Characteristics** (Note 5)

| Symbol   | Parameter                               | Conditions   | $V_{CC}$ | $T_A = 25^\circ\text{C}$ |                   | $T_A = -40$ to $85^\circ\text{C}$ |               | Units |
|----------|---|--|----------|--------------------------|-------------------|-----------------------------------|---------------|-------|
|          |   |  |          | Typ                      | Guaranteed Limits |                                   |               |       |
| $V_{IH}$ | Minimum HIGH Level<br>Input Voltage     |  | 2.0V     |                          | 1.5               | 1.5                               | V             |       |
|          |   |  | 4.5V     |                          | 3.15              | 3.15                              | V             |       |
|          |   |  | 9.0V     |                          | 6.3               | 5.3                               | V             |       |
|          |   |  | 12.0V    |                          | 8.4               | 8.4                               | V             |       |
| $V_{IL}$ | Maximum LOW Level<br>Input Voltage      |  | 2.0V     |                          | 0.5               | 0.5                               | V             |       |
|          |   |  | 4.5V     |                          | 1.35              | 1.35                              | V             |       |
|          |   |  | 9.0V     |                          | 2.7               | 2.7                               | V             |       |
|          |   |  | 12.0V    |                          | 3.6               | 3.6                               | V             |       |
| $R_{ON}$ | Maximum "ON" Resistance<br>See (Note 6) | $V_{CTL} = V_{IH}, I_S = 2.0$ mA<br>$V_{IS} = V_{CC}$ to GND<br>(Figure 1)                     | 4.5V     | 100                      | 170               | 200                               | $\Omega$      |       |
|          |   |  | 9.0V     | 50                       | 85                | 105                               | $\Omega$      |       |
|          |   |  | 12.0V    | 30                       | 70                | 85                                | $\Omega$      |       |
|          |   | $V_{CTL} = V_{IH}, I_S = 2.0$ mA<br>$V_{IS} = V_{CC}$ or GND<br>(Figure 1)                     | 2.0V     | 120                      | 180               | 215                               | $\Omega$      |       |
|          |   |  | 4.5V     | 50                       | 80                | 100                               | $\Omega$      |       |
|          |   |  | 9.0V     | 35                       | 60                | 75                                | $\Omega$      |       |
| 12.0V    | 20                                      | 40   | 60       | $\Omega$                 |                   |                                   |               |       |
| $R_{ON}$ | Maximum "ON" Resistance<br>Matching     | $V_{CTL} = V_{IH}$<br>$V_{IS} = V_{CC}$ to GND   | 4.5V     | 10                       | 15                | 20                                | $\Omega$      |       |
|          |   |  | 9.0V     | 5                        | 10                | 15                                | $\Omega$      |       |
|          |   |  | 12.0V    | 5                        | 10                | 15                                | $\Omega$      |       |
| $I_{IN}$ | Maximum Control<br>Input Current        | $V_{IN} = V_{CC}$ or GND<br>$V_{CC} = 2 - 6V$  |          |                          | $\pm 0.05$        | $\pm 0.5$                         | $\mu\text{A}$ |       |
| $I_{IZ}$ | Maximum Switch "OFF"<br>Leakage Current | $V_{OS} = V_{CC}$ or GND<br>$V_{IS} = \text{GND}$ or $V_{CC}$<br>$V_{CTL} = V_{IL}$ (Figure 2) | 6.0V     | 10                       | $\pm 60$          | $\pm 600$                         | nA            |       |
|          |   |  | 9.0V     | 15                       | $\pm 80$          | $\pm 800$                         | nA            |       |
|          |   |  | 12.0V    | 20                       | $\pm 100$         | $\pm 1000$                        | nA            |       |
| $I_{IZ}$ | Maximum Switch "ON"<br>Leakage Current  | $V_{IS} = V_{CC}$ to GND<br>$V_{CTL} = V_{IH}$<br>$V_{OS} = \text{OPEN}$ (Figure 3)            | 6.0V     | 10                       | $\pm 40$          | $\pm 150$                         | nA            |       |
|          |   |  | 9.0V     | 15                       | $\pm 50$          | $\pm 200$                         | nA            |       |
|          |   |  | 12.0V    | 20                       | $\pm 60$          | $\pm 300$                         | nA            |       |
| $I_{CC}$ | Maximum Quiescent<br>Supply Current     | $V_{IN} = V_{CC}$ or GND<br>$I_{OUT} = 0$ $\mu\text{A}$  | 6.0V     |                          | 1.0               | 10                                | $\mu\text{A}$ |       |
|          |   |  | 9.0V     |                          | 2.0               | 20                                | $\mu\text{A}$ |       |
|          |   |  | 12.0V    |                          | 4.0               | 40                                | $\mu\text{A}$ |       |

**Note 5:** For a power supply of  $5V \pm 10\%$  the worst case on resistance ( $R_{ON}$ ) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

**Note 6:** At supply voltages ( $V_{CC} - \text{GND}$ ) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

| AC Electrical Characteristics   |  |   |          |                    |                   |                             |       |
|---|--|---|----------|--------------------|-------------------|-----------------------------|-------|
| $V_{CC} = 2.0V-6.0V$ $V_{EE} = 0V-12V$ , $C_L = 50$ pF (unless otherwise specified)   |  |   |          |                    |                   |                             |       |
| Symbol  | Parameter  | Conditions  | $V_{CC}$ | $T_A = 25^\circ C$ |                   | $T_A = -40$ to $85^\circ C$ | Units |
|   |  |   |          | Typ                | Guaranteed Limits |                             |       |
| $t_{PHL}$ , $t_{PLH}$   | Maximum Propagation Delay Switch In to Out                           |   | 3.3V     | 25                 | 30                | 20                          | ns    |
|   |  |   | 4.5V     | 5                  | 10                | 13                          | ns    |
|   |  |   | 9.0V     | 4                  | 8                 | 10                          | ns    |
|   |  |   | 12.0V    | 3                  | 7                 | 11                          | ns    |
| $t_{PZL}$ , $t_{PZH}$   | Maximum Switch Turn "ON" Delay                                       | $R_L = 1$ k $\Omega$  | 3.3V     | 30                 | 58                | 73                          | ns    |
|   |  |   | 4.5V     | 12                 | 20                | 25                          | ns    |
|   |  |   | 9.0V     | 6                  | 12                | 15                          | ns    |
|   |  |   | 12.0V    | 5                  | 10                | 13                          | ns    |
| $t_{PHZ}$ , $t_{PLZ}$   | Maximum Switch Turn "OFF" Delay                                      | $R_L = 1$ k $\Omega$  | 3.3V     | 60                 | 100               | 125                         | ns    |
|   |  |   | 4.5V     | 25                 | 36                | 45                          | ns    |
|   |  |   | 9.0V     | 20                 | 32                | 40                          | ns    |
|   |  |   | 12.0V    | 15                 | 30                | 38                          | ns    |
|   | Minimum Frequency Response (Figure 7)<br>$20 \log (V_O/V_I) = -3$ dB | $R_L = 600\Omega$<br>$V_{IS} = 2 V_{PP}$ at $(V_{CC}/2)$<br>(Note 7)(Note 8)                        | 4.5V     | 40                 |                   |                             | MHz   |
|   |  |   | 9.0V     | 100                |                   |                             | MHz   |
|   | Crosstalk Between any Two Switches (Figure 8)                        | $R_L = 600\Omega$ , $F = 1$ MHz<br>(Note 8)(Note 9)   | 4.5V     | -52                |                   |                             | dB    |
|   |  |   | 9.0V     | -50                |                   |                             | dB    |
|   | Peak Control to Switch Feedthrough Noise (Figure 9)                  | $R_L = 600\Omega$ , $F = 1$ MHz<br>$C_L = 50$ pF  | 4.5V     | 100                |                   |                             | mV    |
|   |  |   | 9.0V     | 250                |                   |                             | mV    |
|   | Switch OFF Signal Feedthrough Isolation (Figure 10)                  | $R_L = 600\Omega$ , $F = 1$ MHz<br>$V_{(CT)} V_{IL}$<br>(Note 8)(Note 9)                            | 4.5V     | -42                |                   |                             | dB    |
|   |  |   | 9.0V     | -44                |                   |                             | dB    |
| THD   | Total Harmonic Distortion (Figure 11)                                | $R_L = 10$ k $\Omega$ , $C_L = 50$ pF,<br>$F = 1$ kHz<br>$V_{IS} = 4 V_{PP}$<br>$V_{IS} = 8 V_{PP}$ | 4.5V     | .013               |                   |                             | %     |
|   |  |   | 9.0V     | .008               |                   |                             | %     |
|   |  |   |          |                    |                   |                             |       |
| $C_{IN}$  | Maximum Control Input Capacitance                                    |   |          | 5                  | 10                | 10                          | pF    |
| $C_{IN}$  | Maximum Switch Input Capacitance                                     |   |          | 20                 |                   |                             | pF    |
| $C_{IN}$  | Maximum Feedthrough Capacitance                                      | $V_{CTL} = GND$   |          | 0.5                |                   |                             | pF    |
| $C_{PD}$  | Power Dissipation Capacitance  |   |          | 15                 |                   |                             | pF    |
| <p><b>Note 7:</b> Adjust 0 dBm for <math>F = 1</math> kHz (Null <math>R_L/R_{ON}</math> Attenuation).</p> <p><b>Note 8:</b> <math>V_{IS}</math> is centered at <math>V_{CC}/2</math>.</p> <p><b>Note 9:</b> Adjust input for 0 dBm.</p> |  |   |          |                    |                   |                             |       |

AC Test Circuits and Switching Time Waveforms

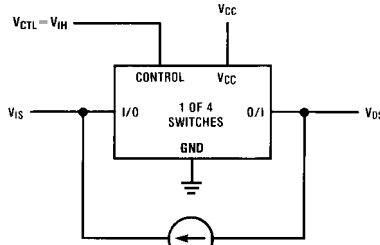


FIGURE 1. "ON" Resistance

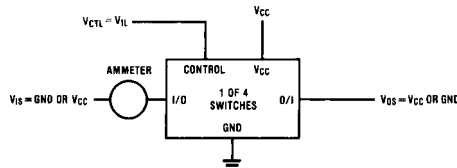


FIGURE 2. "OFF" Channel Leakage Current

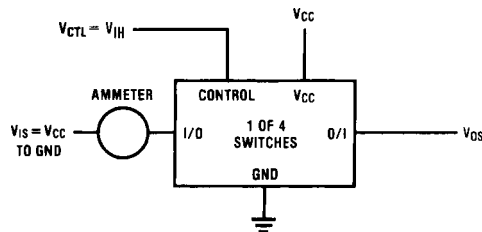


FIGURE 3. "ON" Channel Leakage Current

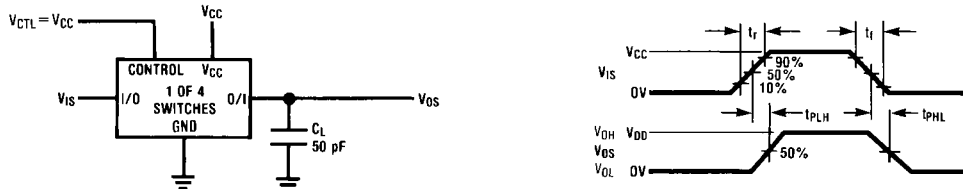


FIGURE 4.  $t_{PHL}$ ,  $t_{PLH}$  Propagation Delay Time Signal Input to Signal Output

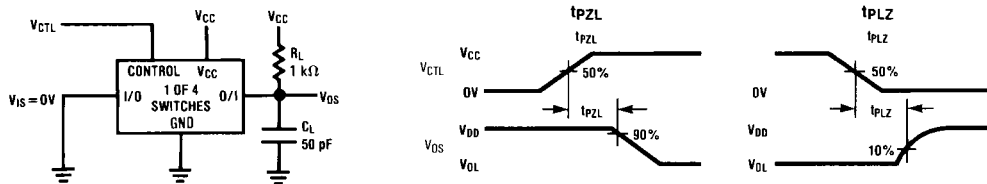


FIGURE 5.  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal Output

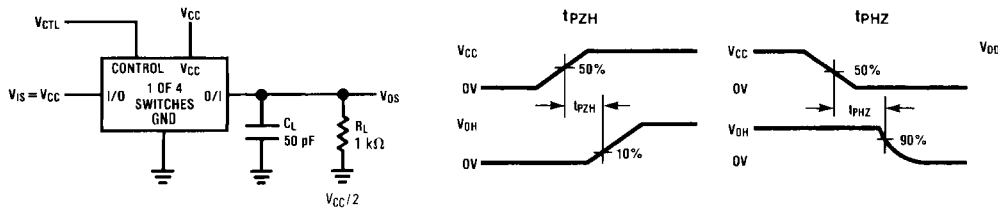


FIGURE 6.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

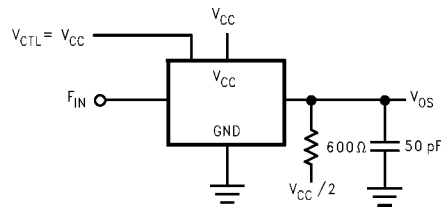


FIGURE 7. Frequency Response

Crosstalk and Distortion Test Circuits

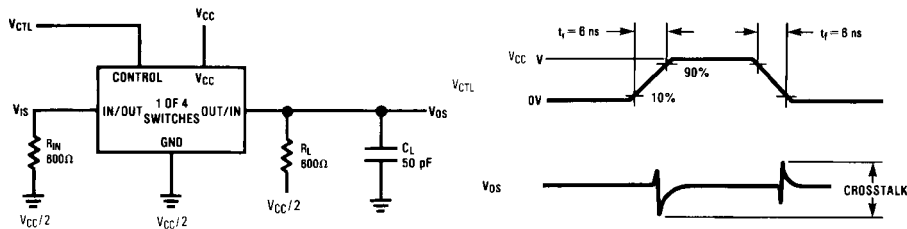


FIGURE 8. Crosstalk: Control Input to Signal Output

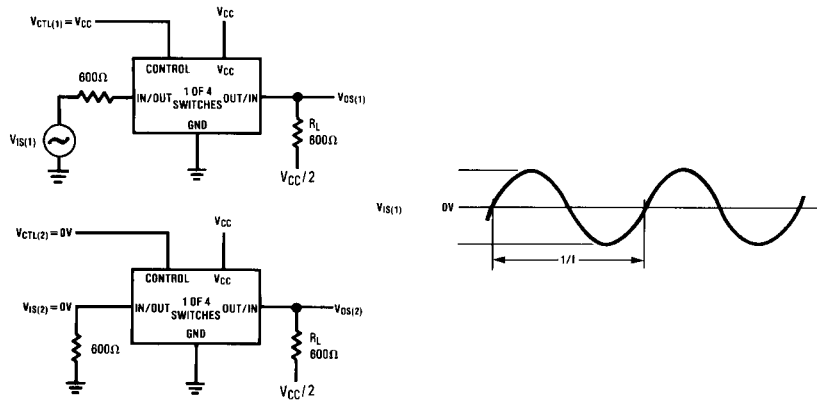
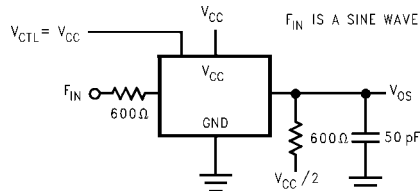
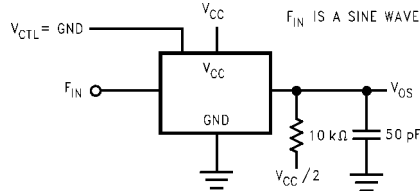


FIGURE 9. Crosstalk Between Any Two Switches

**Crosstalk and Distortion Test Circuits** (Continued)

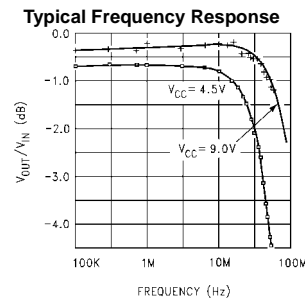
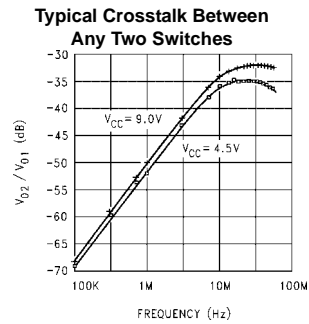
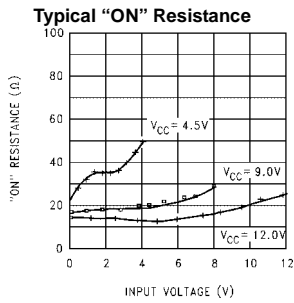


**FIGURE 10. Switch OFF Signal Feedthrough Isolation**



**FIGURE 11. Sinewave Distortion**

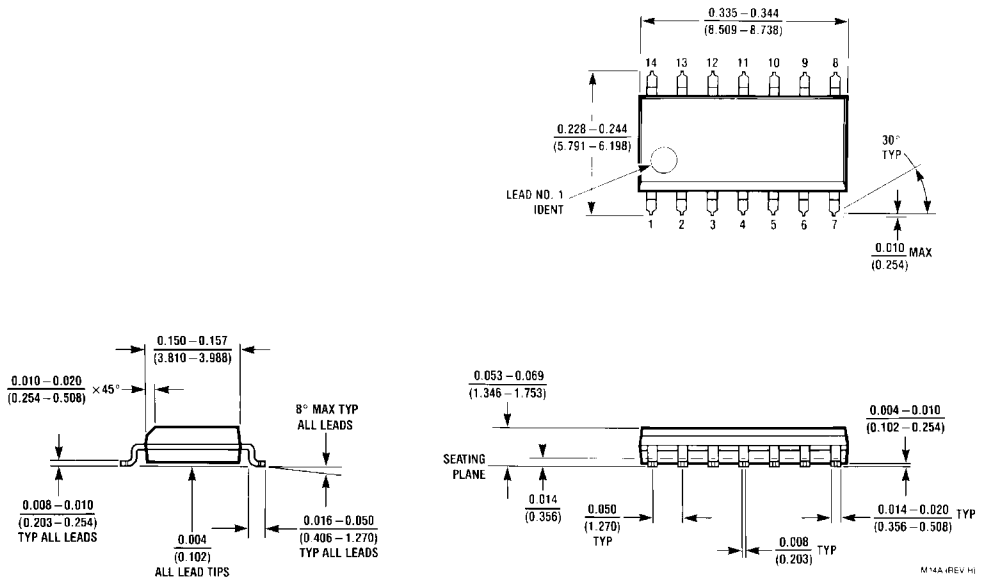
**Typical Performance Characteristics**



**Special Considerations**

In certain applications the external load-resistor current may include both  $V_{CC}$  and signal line components. To avoid drawing  $V_{CC}$  current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON Resistance).

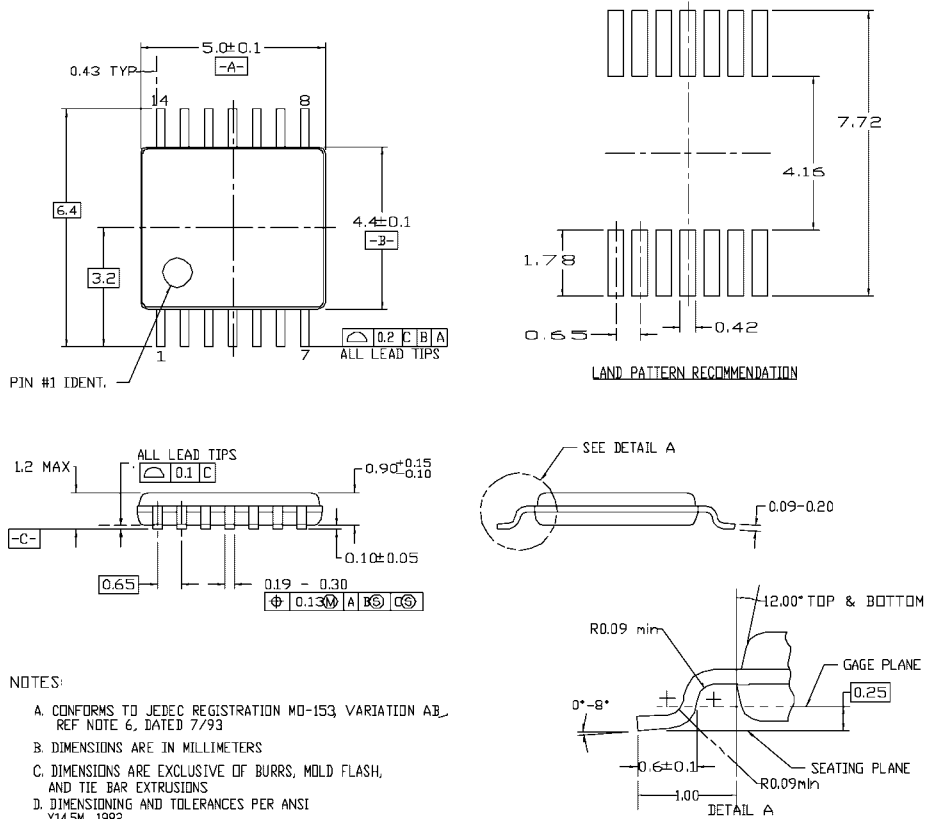
**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

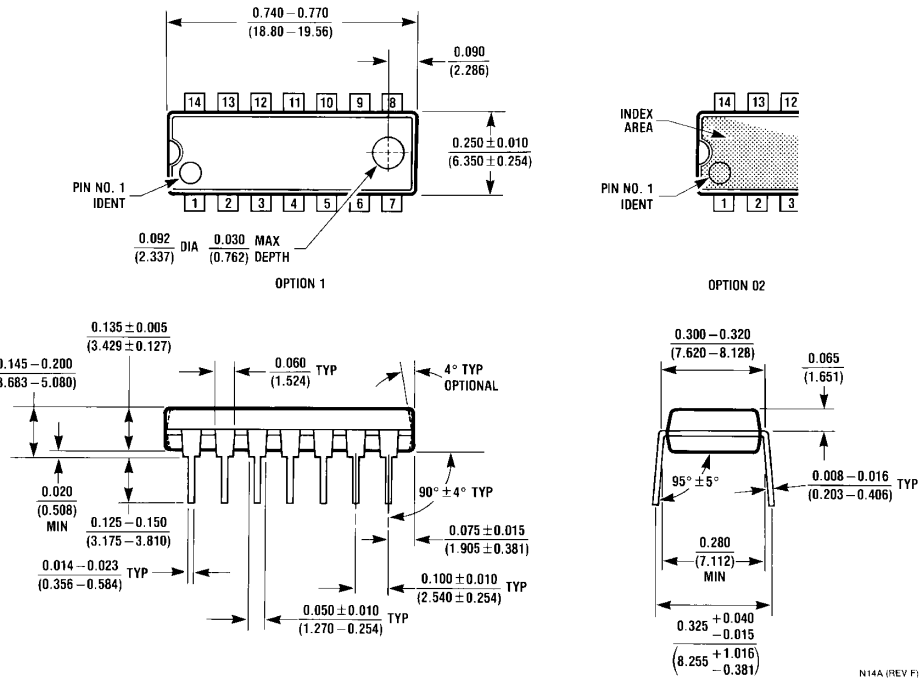


- NOTES:
- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
  - B. DIMENSIONS ARE IN MILLIMETERS
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
  - D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

N14A (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)