

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

AS1751, AS1752, AS1753

High-Speed, Low-Voltage, Single-Supply, 0.9Ω, Quad SPST Analog Switches

1 General Description

The AS1751/AS1752/AS1753 are high-speed, low-voltage, quad single-pole/single-throw (SPST) analog switches.

Fast switching speeds, low ON-resistance, and low power consumption make these devices ideal for single-cell battery powered applications.

These highly-reliable devices operate from a single +1.6 to +3.6V supply, and are differentiated by the type and number of switches:

- AS1751 – Four normally open (NO) switches
- AS1752 – Four normally closed (NC) switches
- AS1753 – Two NO switches and Two NC switches

The AS1753 supports break-before-make switching.

With very low ON-resistance (RON), RON matching and RON flatness, the devices can accurately switch signals for sample and hold circuits, digital filters, and op-amp gain switching networks.

The AS1751/AS1752/AS1753 digital logic input is 1.8V CMOS-compatible when using a +3V supply, and all devices can handle Rail-to-Rail signals.

The devices are available in a 3mm x 3mm 16-pin TQFN package and a 14-pin TSSOP package.

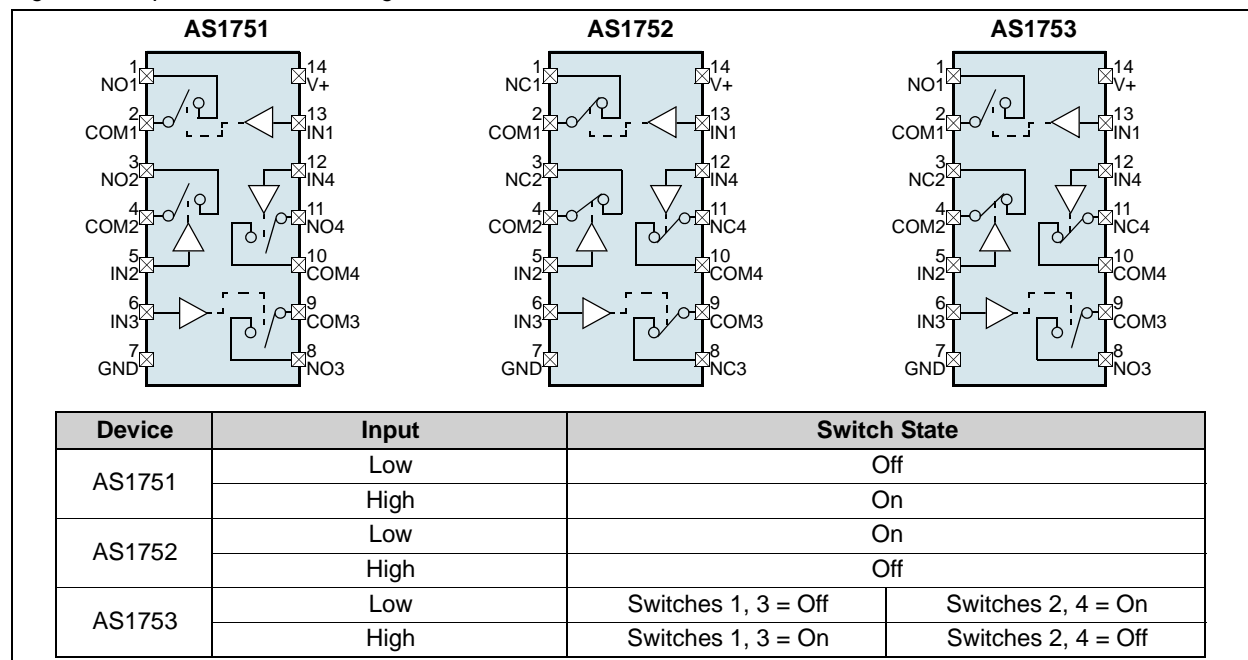
2 Key Features

- ON-Resistance:
 - 0.9Ω (+3V supply)
 - 2.5Ω (+1.8V supply)
- RON Matching:
 - 0.12Ω (+3V supply)
 - 0.25Ω (+1.8V supply)
- RON Flatness: 0.1Ω (+3V Supply)
- Supply Voltage Range: +1.6 to +3.6V
- Switching Speed: tON = 22ns, tOFF = 14ns
- Current-Handling: 250mA Continuous
- Break-Before-Make Switching (AS1753)
- Rail-to-Rail Signal Handling
- 1.8V CMOS Logic Compatible (+3V Supply)
- Operating Temperature Range: -40 to +85°C
- Package Types:
 - 16-pin TQFN (3mm x 3mm)
 - 14-pin TSSOP

3 Applications

The devices are ideal for use in power routing systems, cordless and mobile phones, MP3 players, CD and DVD players, PDAs, handheld computers, digital cameras, hard drives, and any other application where high-speed signal switching is required.

Figure 1. 14-pin TSSOP Block Diagrams



4 Pinout

Pin Assignments

Figure 2. TQFN Pin Assignments (Top View)

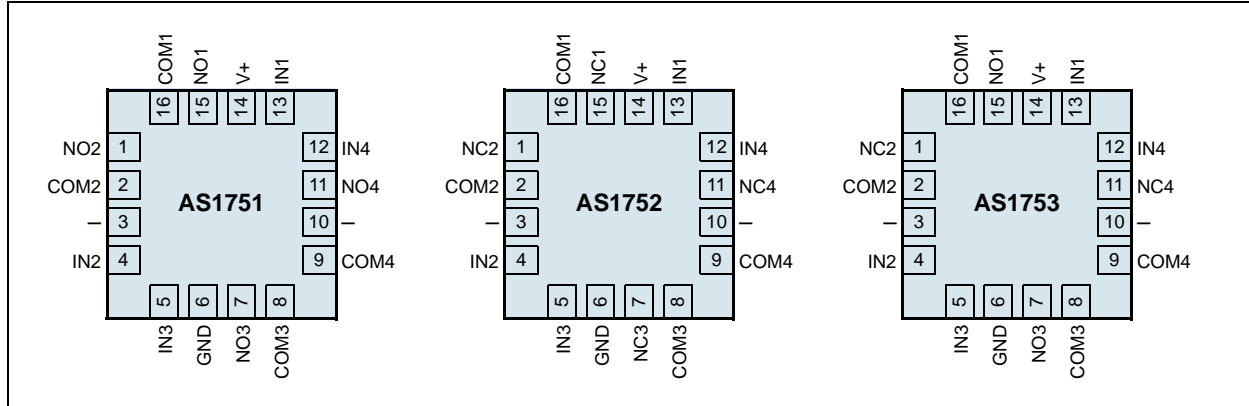
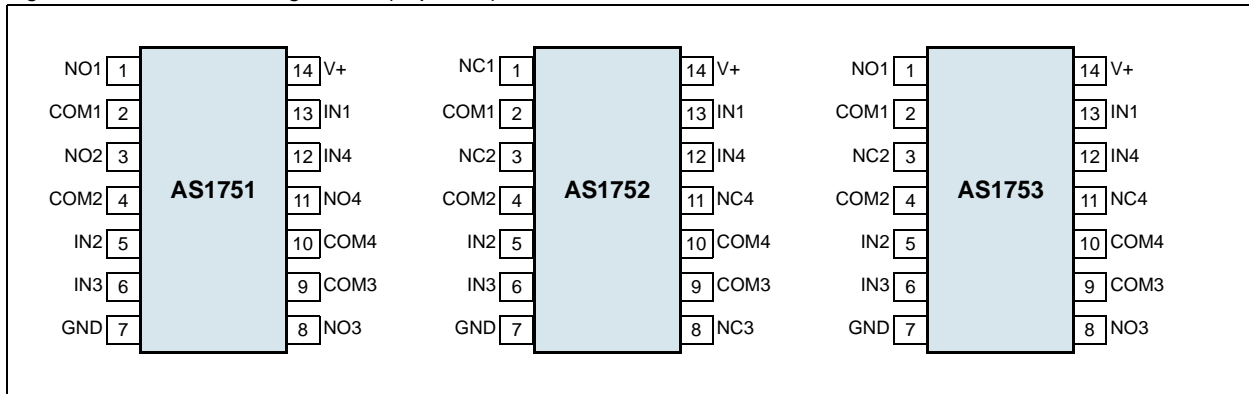


Figure 3. TSSOP Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
(see Figure 2 and Figure 3)	COM1:COM4	Analog Switch 1, 2, 3, 4 Common
	GND	Ground
	IN1:IN4	Analog Switch 1, 2, 3, 4 Logic Control Input
	NC1:NC4	Analog Switch 1, 2, 3, 4 Normally Closed Terminal
	NO1:NO4	Analog Switch 1, 2, 3, 4 Normally Open Terminal
	V+	Input Supply Voltage. +1.6 to +3.6V

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V+, INx to GND	-0.3	+5	V	
COMx, NOx, NCx to GND †	-0.3	V+ + 0.3	V	
COMx, NOx, NCx Continuous Current	-250	+250	mA	
COMx, NOx, NCx Peak Current	-350	+350	mA	Pulsed at 1ms 10% duty cycle
Continuous Power Dissipation (T _{AMB} = +70°C)	16-pin TQFN	727	mW	Derate at 9.1W/°C above +70°C
	14-pin TSSOP	1349		Derate at 16.9W/°C above +70°C
Operating Temperature Range	-40	+85	°C	
Electro-Static Discharge		2500	V	HBM Mil-Std883E 3015.7 methods
Latch Up Immunity		250	mA	Norm: JEDEC 17
Junction Temperature		+150	°C	
Storage Temperature Range	-65	+150	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"

† Signals on pins COM1, COM3, NO1, NO2, NC1, or NC2 that exceed V+ or GND are clamped by internal diodes. Forward-diode current should be limited to the maximum current rating.

6 Electrical Characteristics

Table 3. Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V+	Power Supply Range	T _{AMB} = T _{MIN} to T _{MAX}	1.6		3.6	V
I+	Positive Supply Current	V+ = 3.6V, V _{INx} = 0 or V+, T _{AMB} = +25°C			0.1	μA

V+ = +2.7 to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values @ V+ = +3.0V, T_{AMB} = +25°C.

Table 4. +3V Supply Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog Switch						
V _{COMx} , V _{NOx} , V _{NCx}	Analog Signal Range		0		V+	V
R _{ON}	ON-Resistance	V+ = 2.7V, I _{COMx} = 100mA, V _{NOx} or V _{NCx} = 1.5V	T _{AMB} = +25°C	0.4	0.9	Ω
			T _{AMB} = T _{MIN} to T _{MAX}		1	
ΔR _{ON}	ON-Resistance Match Between Channels ¹	V+ = 2.7V, I _{COMx} = 100mA, V _{NOx} or V _{NCx} = 1.5V	T _{AMB} = +25°C	0.03	0.12	Ω
			T _{AMB} = T _{MIN} to T _{MAX}		0.15	
R _{FLAT(ON)}	ON-Resistance Flatness ²	V+ = 2.7V, I _{COMx} = 100mA, V _{NOx} or V _{NCx} = 1, 1.5, or 2V	T _{AMB} = +25°C	0.02	0.1	Ω
			T _{AMB} = T _{MIN} to T _{MAX}		0.12	
I _{NOx(OFF)} , I _{NCx(OFF)}	NO _x or NC _x Off-Leakage Current	V+ = 3.6V, V _{COMx} = 0.3 or 3.6V, V _{NOx} or V _{NCx} = 3.6 or 0.3V	T _{AMB} = +25°C	-2.5	+2.5	nA
			T _{AMB} = T _{MIN} to T _{MAX}	-10	+10	
I _{COMx(OFF)}	COM _x Off-Leakage Current	V+ = 3.6V, V _{COMx} = 0.3 or 3.6V, V _{NOx} or V _{NCx} = 3.6 or 0.3V	T _{AMB} = +25°C	-2.5	+2.5	nA
			T _{AMB} = T _{MIN} to T _{MAX}	-10	+10	
I _{COMx(ON)}	COM _x On-Leakage Current	V+ = 3.6V, V _{COMx} = 0.3 or 3.6V, V _{NOx} or V _{NCx} = 0.3 or 3.6V	T _{AMB} = +25°C	-2.5	+2.5	nA
			T _{AMB} = T _{MIN} to T _{MAX}	-10	+10	
Switch Dynamic Characteristics						
t _{ON}	Turn On Time ³	V _{NOx} or V _{NCx} = 1.5V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figures 13, 14	T _{AMB} = +25°C	16	22	ns
			T _{AMB} = T _{MIN} to T _{MAX}		24	
t _{OFF}	Turn Off Time ³	V _{NOx} or V _{NCx} = 1.5V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figures 13, 14	T _{AMB} = +25°C	5	14	ns
			T _{AMB} = T _{MIN} to T _{MAX}		15	
t _{BBM}	Break-Before-Make ³	V _{NOx} or V _{NCx} = 1.5V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figure 15 (AS1753)	T _{AMB} = +25°C	11		ns
			T _{AMB} = T _{MIN} to T _{MAX}	2		
Q	Charge Injection	V _{GEN} = V+, R _{GEN} = 0, C _{LOAD} = 1.0nF, Figure 16		2		pC
C _{OFF}	NO _x , NC _x Off-Capacitance	f = 1MHz, Figure 17		45		pF
C _{COMx(OFF)}	COM _x Off-Capacitance	f = 1MHz, Figure 17		49		pF
C _{COMx(ON)}	COM _x On-Capacitance	f = 1MHz, Figure 17		85		pF

Table 4. +3V Supply Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Viso	Off-Isolation ⁴	f = 10MHz, R _{LOAD} = 50Ω, C _{LOAD} = 5pF, Figure 18		-40		dB
		f = 1MHz, R _{LOAD} = 50Ω, C _{LOAD} = 5pF, Figure 18		-55		
	Crosstalk ⁵	f = 10MHz, R _{LOAD} = 50Ω, C _{LOAD} = 5pF, Figure 18		-70		dB
		f = 1MHz, R _{LOAD} = 50Ω, C _{LOAD} = 5pF, Figure 18		-80		
THD	Total Harmonic Distortion	f = 20Hz to 20kHz, V _{COMx} = 2Vp-p, R _{LOAD} = 32Ω		0.033		%
Logic Input						
V _{IH}	Input Logic High		1.4			V
V _{IL}	Input Logic Low				0.5	V
I _{IN}	Input Leakage Current	V _{INx} = 0 or V+	-1	0.0001	+1	μA

V₊ = +1.8V, V_{IH} = +1.0V, V_{IL} = 0.4V, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values @ T_{AMB} = +25°C.

Table 5. +1.8V Supply Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog Switch						
V _{COMx} , V _{NOx} , V _{NCx}	Analog Signal Range		0		V+	V
R _{ON}	ON-Resistance	V ₊ = 1.8V, I _{COMx} = 10mA, V _{NOx} or V _{NCx} = 0.9V	T _{AMB} = +25°C	0.9	2.5	Ω
			T _{AMB} = T _{MIN} to T _{MAX}		3	
ΔR _{ON}	ON-Resistance Match Between Channels ¹	V ₊ = 1.8V, I _{COMx} = 10mA, V _{NOx} or V _{NCx} = 0.9V	T _{AMB} = +25°C	0.05	0.25	Ω
			T _{AMB} = T _{MIN} to T _{MAX}		0.25	
Switch Dynamic Characteristics						
t _{ON}	Turn On Time ³	V _{NOx} or V _{NCx} = 1.0V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figures 13, 14	T _{AMB} = +25°C	22	30	ns
			T _{AMB} = T _{MIN} to T _{MAX}		35	
t _{OFF}	Turn Off Time ³	V _{NOx} or V _{NCx} = 1.0V, R _{LOAD} = 50Ω, C _{LOAD} = 35pF, Figures 13, 14	T _{AMB} = +25°C	12	20	ns
			T _{AMB} = T _{MIN} to T _{MAX}		25	
Q	Charge Injection	V _{GEN} = V+, R _{GEN} = 0, C _{LOAD} = 1.0nF, Figure 16		1		pC
Logic Input						
V _{IH}	Input Logic High		1.0			V
V _{IL}	Input Logic Low				0.4	V
I _{IN}	Input Leakage Current	V _{INx} = 0 or V+	-1	0.0001	+1	μA

1. ΔR_{ON} = R_{ON(MAX)} - R_{ON(MIN)}.

2. Flatness is defined as the difference between the maximum and the minimum value of ON-resistance as measured over the specified analog signal ranges.

3. Guaranteed by design.

4. Off-Isolation = 20log₁₀(V_{COMx}/V_{NOx}), V_{COMx} = output, V_{NOx} = input to off switch.

5. Between two switches.

7 Typical Operating Characteristics

Figure 4. Frequency Response

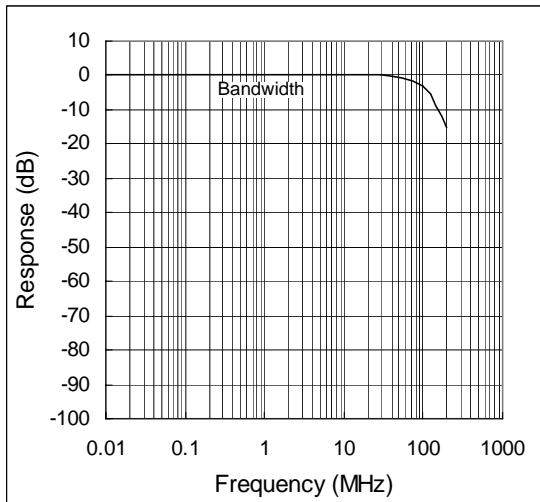


Figure 5. Total Harmonic Distortion vs. Frequency

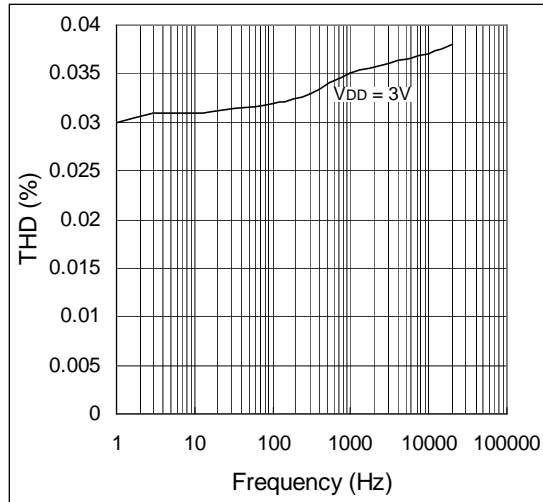


Figure 6. Turn On/Turn Off Time vs. Temperature

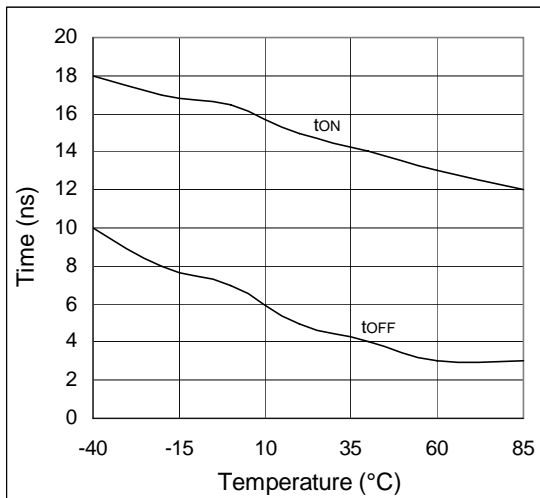


Figure 7. Turn On/Off Time vs. Supply Voltage

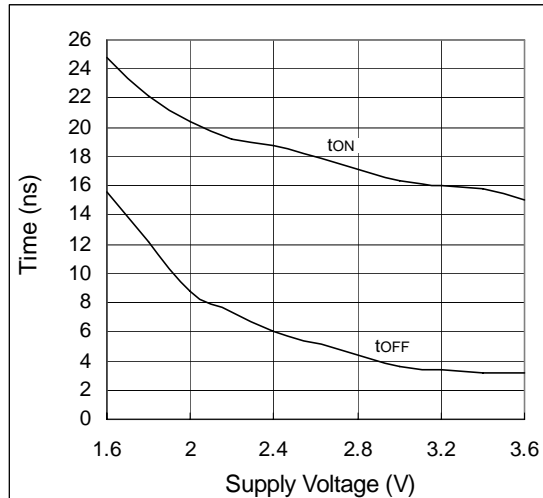


Figure 8. R_{ON} vs. V_{COM} and Temperature; $V_{DD} = 2.7V$

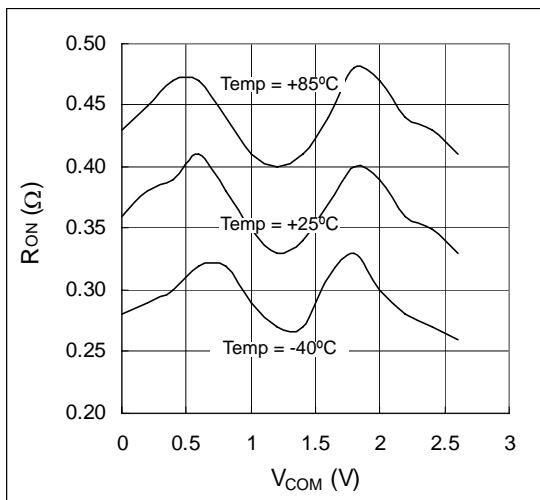


Figure 9. R_{ON} vs. V_{COM}

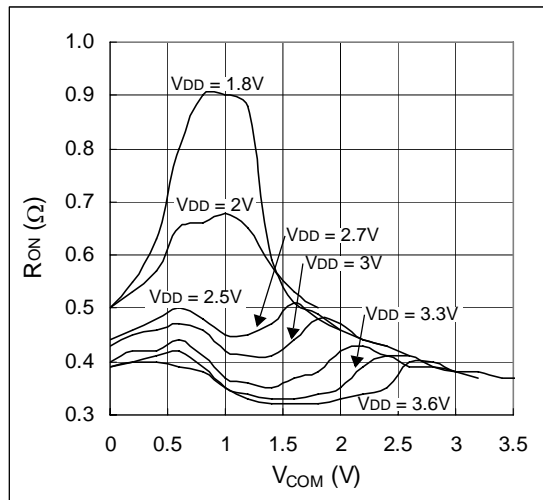
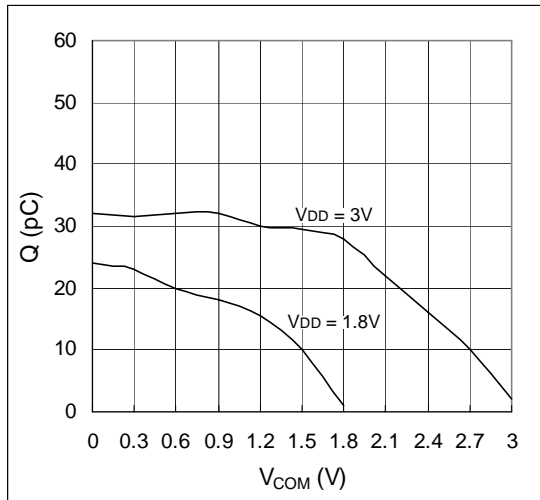


Figure 10. Charge Injection vs. V_{COM}



8 Detailed Description

The AS1751/AS1752/AS1753 are low ON-resistance, low-voltage, quad analog SPST switches that operate from a single +1.6 to +3.6V supply.

CMOS process technology allows switching of analog signals that are within the supply voltage range (GND to V+).

Figure 11. 16-pin TQFN Block Diagrams

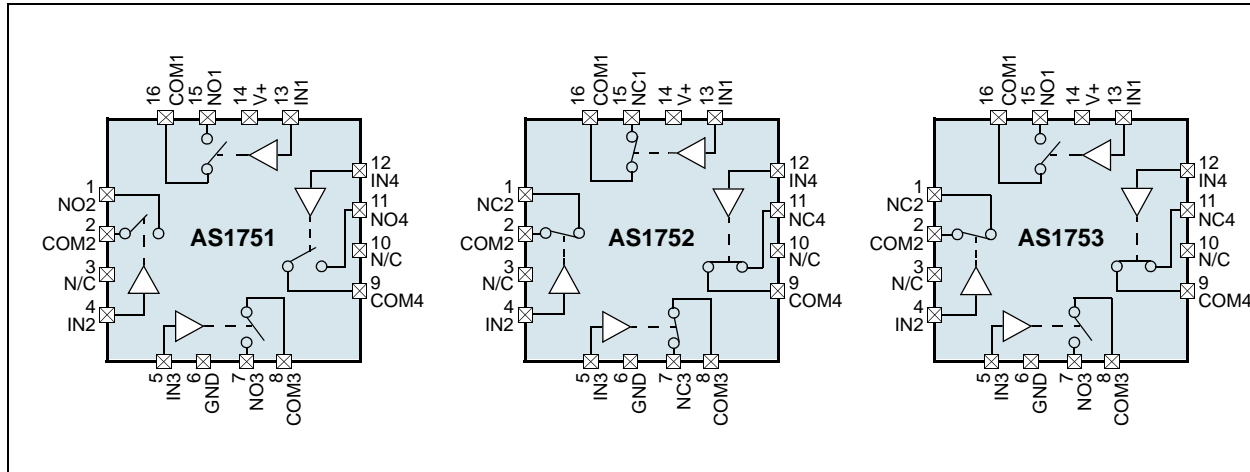


Table 6. Truth Tables

Device	Input	Switch State	
AS1751	Low	Off	
	High	On	
AS1752	Low	On	
	High	Off	
AS1753	Low	Switches 1, 3 = Off	Switches 2, 4 = On
	High	Switches 1, 3 = On	Switches 2, 4 = Off

ON-Resistance

When powered from a +3V supply, the low (0.9Ω, max) ON-resistance allows high-speed, continuous signals to be switched in a variety of applications.

Bi-Directional Switching

Pins NOx, NCx, and COMx are bi-directional, thus they can be used as inputs to- or outputs from other components.

Analog Signal Levels

Analog signals ranging over the entire supply voltage range (V+ to GND) can be switched with very little change in ON-resistance (see [Typical Operating Characteristics on page 6](#)).

Logic Inputs

The devices' logic inputs can be driven up to +3.6V regardless of the supply voltage value. For example, with a +1.8V supply, INx may be driven low to GND and high to +3.6V. This allows the devices to interface with +3V systems using a supply of less than 3V.

9 Application Information

Power Supply Sequencing

Proper power-supply sequencing is critical for proper switch operation. The power supplies should be started up in the following sequence:

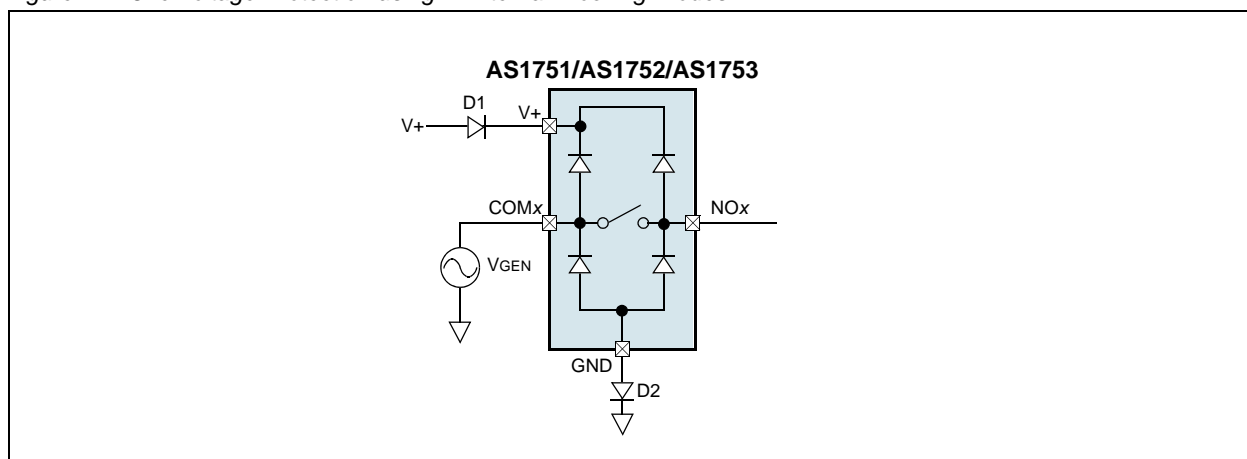
1. V+
2. NO_x, NC_x, COM_x

Note: Do not exceed the absolute maximum ratings (see page 2).

Overvoltage Protection

ON-resistance increases slightly at lower supply voltages.

Figure 12. Overvoltage Protection using 2 External Blocking Diodes



Adding diode D2 to the circuit shown in Figure 12 causes the logic threshold to be shifted relative to GND. Diodes D1 and D2 also protect against overvoltage conditions.

For example, in the circuit shown in Figure 12, if the supply voltage goes below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Power Supply Bypass

Power supply connections to the devices must maintain a low impedance to ground. This can be done using a bypass capacitor, which will also improve noise margin and prevent switching noise propagation from the V+ supply to other components.

A 0.1 μ F bypass capacitor, connected from V+ to GND (see Figure 18 on page 11), is adequate for most applications.

Logic Inputs

Driving IN_x Rail-to-Rail will help minimize power consumption.

Layout Considerations

High-speed switches require proper layout and design procedures for optimum performance.

- Short, wide traces should be used to reduce stray inductance and capacitance.
- Bypass capacitors should be as close to the device as possible.
- Large ground planes should be used wherever possible.

Timing Diagrams and Test Setups

Figure 13. AS1751/AS1753 Test Circuit and Timing Diagram

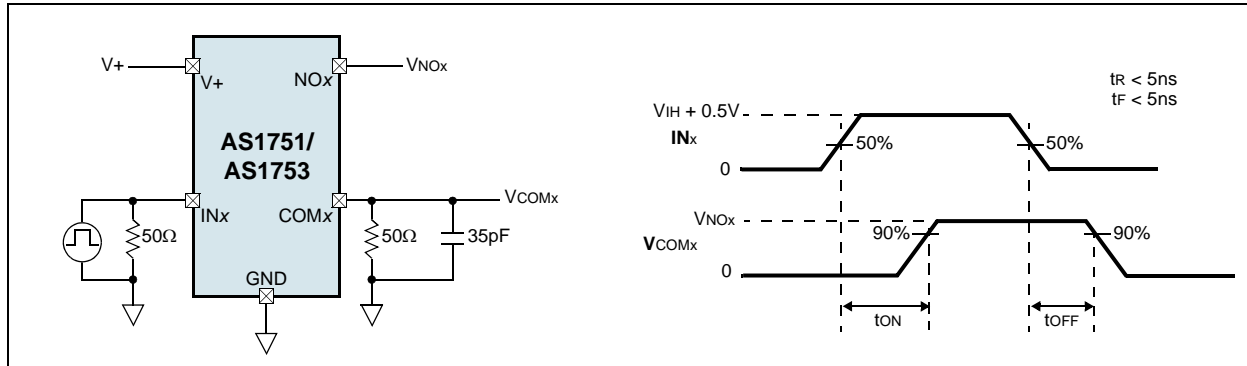


Figure 14. AS1752/AS1753 Test Circuit and Timing Diagram

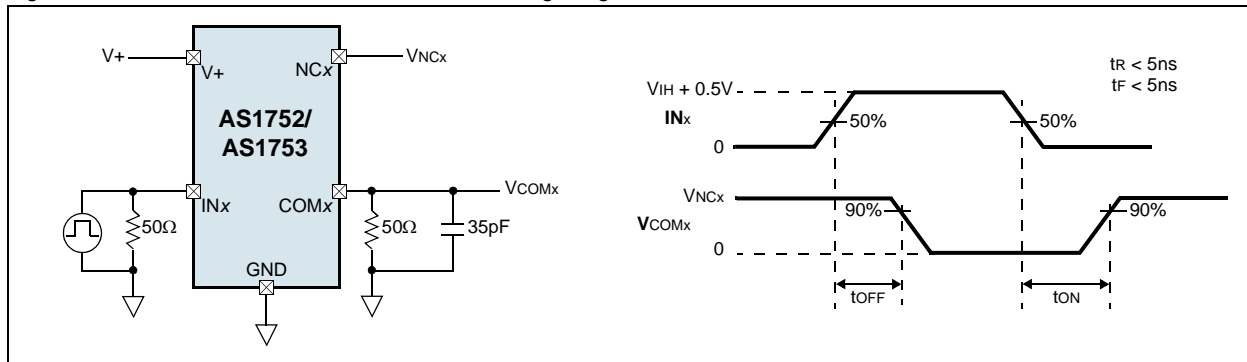


Figure 15. AS1753 Test Circuit and Timing Diagram

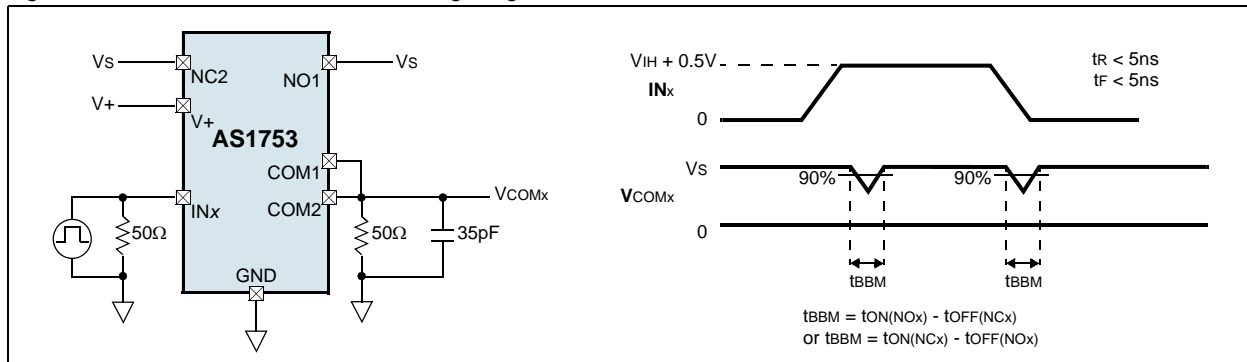


Figure 16. Charge Injection

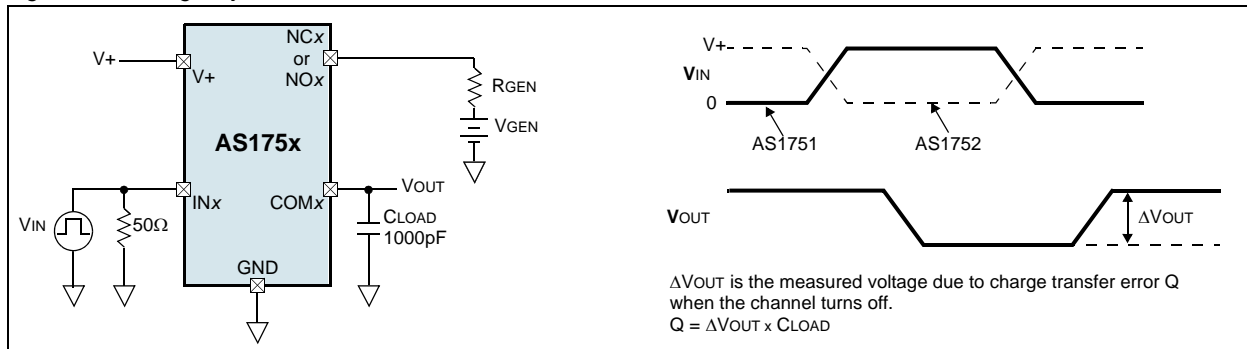


Figure 17. NO_x, NC_x, and COM_x Capacitance

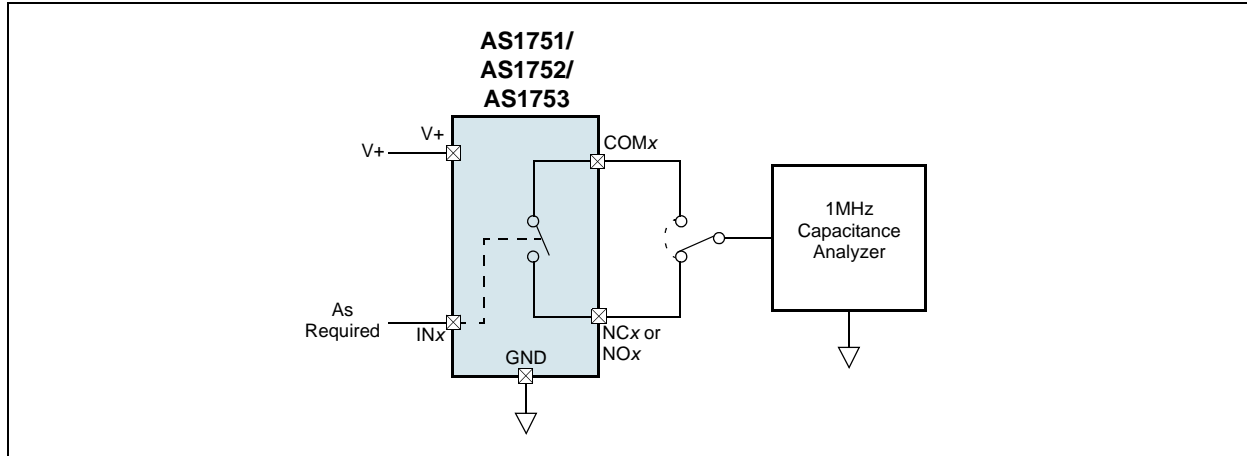
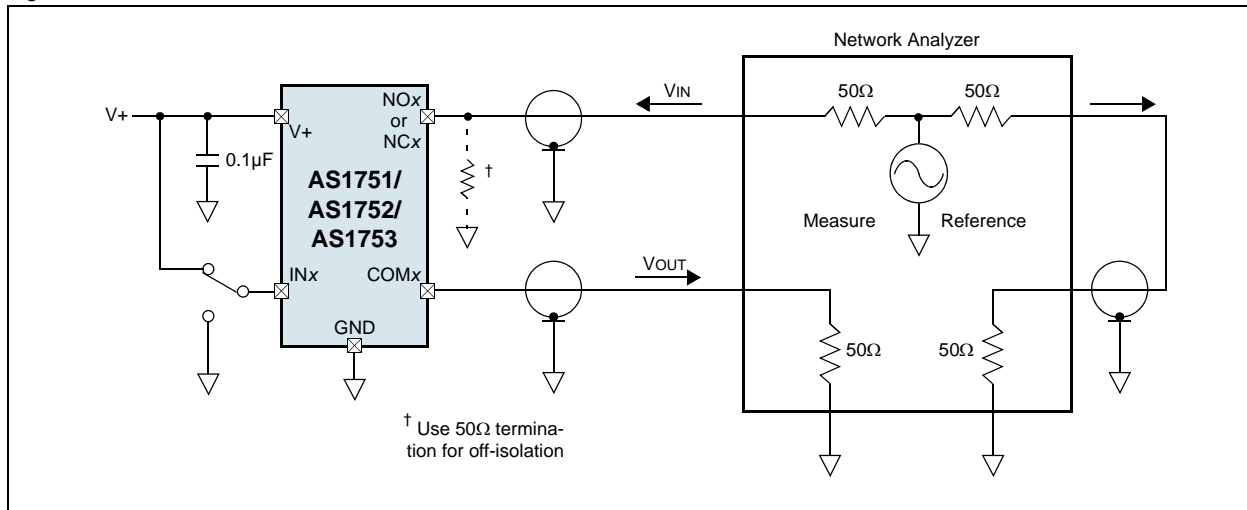


Figure 18. Off-Isolation, On-Loss, and Crosstalk



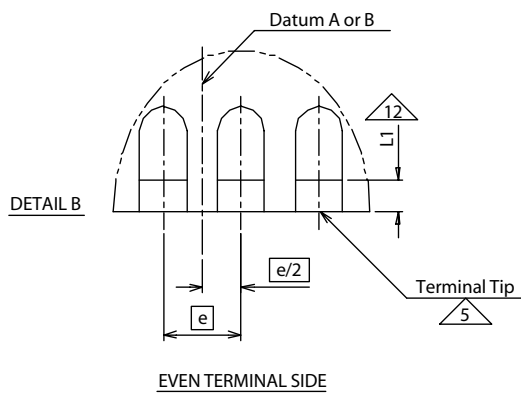
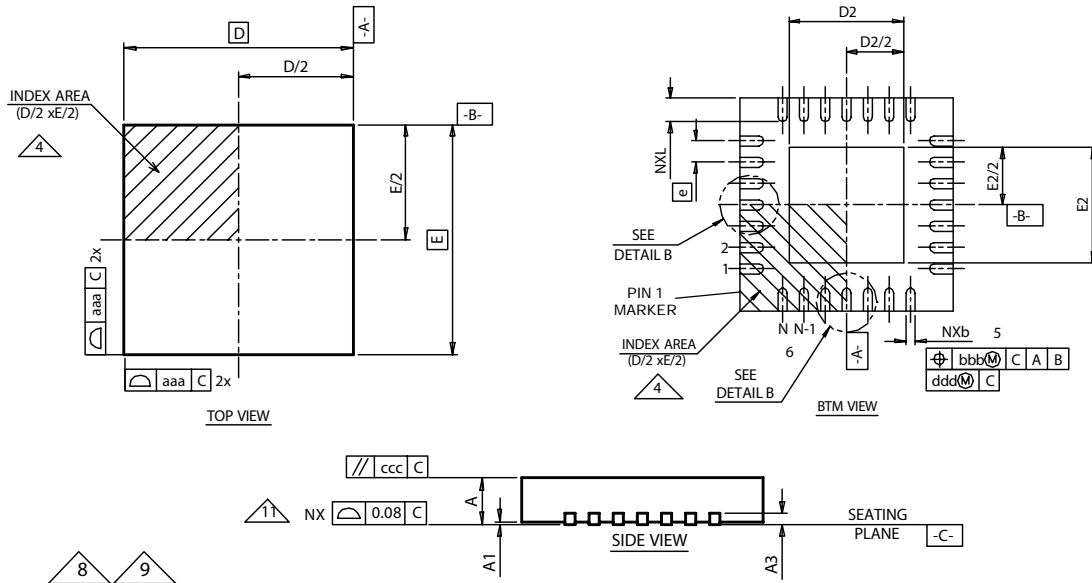
Notes:

1. Measurements are standardized against short-circuit at socket terminals.
2. Off-isolation is measured between COM_x and the off NC_x/NO_x terminal on each switch. Off-isolation = $20\log(V_{OUT}/V_{IN})$.
3. On-loss is measured between COM_x and the on NC_x/NO_x terminal on each switch. On-loss = $20\log(V_{OUT}/V_{IN})$.
4. Signal direction through the switch is reversed; worst values are recorded.

Package Drawings and Markings

The devices are available in an 16-pin TQFN package and an 14-pin TSSOP package.

Figure 19. 16-pin TQFN Package

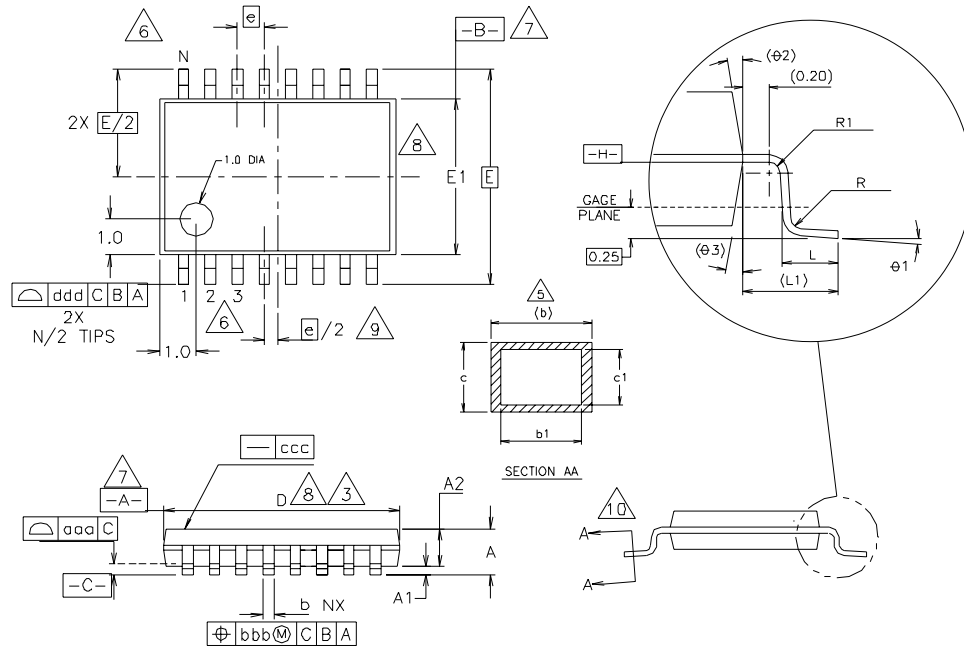


Common Dimensions				
Symbol	Min	Nom	Max	Notes
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
L1	0.03		0.15	
D BSC		3.00		1, 2, 10
E BSC		3.00		1, 2, 10
D2	1.30	1.45	1.55	1, 2, 10
E2	1.30	1.45	1.55	1, 2, 10
L	0.30	0.40	0.50	1, 2, 10
N		16		1, 2, 10
ND		4		1, 2, 10
NE		4		1, 2, 10

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters; angles in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95 SPP-012*. Details of terminal #1 identifier are optional but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip. If one end of the terminal has the optional radius, the b dimension should not be measured in that radius area.
6. Dimensions ND and NE refer to the number of terminals on each D and E side, respectively.
7. Depopulation is possible in a symmetrical fashion.
8. [Figure 19](#) is shown for illustration only and does not represent any specific variation.
9. All variations may be constructed per [Figure 19](#), however variations may alternately be constructed between square or rectangle shape per dimensions D and E.
10. Refer to the Dimensions Table for a complete set of dimensions.
11. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
12. Depending on the method of lead termination at the edge of the package, pullback (L1) may be present. L minus L1 to be $\geq 0.33\text{mm}$.
13. For variations with more than one lead count for a given body size and terminal pitch, each lead count for that variation is denoted by a dash number (e.g., -1 or -2).
14. NJR designates non-JEDEC registered package.

Figure 20. 14-pin TSSOP Package



Symbol	0.65mm Lead Pitch ^{1, 2}			Note	Symbol	0.65mm Lead Pitch ^{1, 2}			Note
	Min	Nom	Max			Min	Nom	Max	
A	-	-	1.10		θ1	0°	-	8°	
A1	0.05	-	0.15		L1	1.0 Ref			
A2	0.85	0.90	0.95		aaa	0.10			
L	0.50	0.60	0.75		bbb	0.10			
R	0.09	-	-		ccc	0.05			
R1	0.09	-	-		ddd	0.20			
b	0.19	-	0.30	5	e	0.65 BSC			
b1	0.19	0.22	0.25		θ2	12° Ref			
c	0.09	-	0.20		θ3	12° Ref			
c1	0.09	-	0.16						
Variations									
D	4.90	5.00	5.10	3, 8	e	0.65 BSC			
E1	4.30	4.40	4.50	4, 8	N	14			6
E	6.4 BSC								

Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensions and tolerancing per *ASME Y14.5M-1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of dimension b at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm for 0.5mm pitch packages.
6. Terminal numbers shown are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per package, the center lead must be coincident with the package centerline, datum A.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

10 Ordering Information

The devices are available as the standard products shown in [Table 7](#).

Table 7. Ordering Information

Model	Description	Delivery Form	Package
AS1751S	SPST Switch	Tube	14-TSSOP
AS1751S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1751V [†]	Quad SPST Switch	Tray	16-TQFN 3mmx3mm
AS1751V-T [†]	Quad SPST Switch	Tape and Reel	16-TQFN 3mmx3mm
AS1752S	Quad SPST Switch	Tube	14-TSSOP
AS1752S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1752V [†]	Quad SPST Switch	Tray	16-TQFN 3mmx3mm
AS1752V-T [†]	Quad SPST Switch	Tape and Reel	16-TQFN 3mmx3mm
AS1753S	Quad SPST Switch	Tube	14-TSSOP
AS1753S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1753V [†]	Quad SPST Switch	Tray	16-TQFN 3mmx3mm
AS1753V-T [†]	Quad SPST Switch	Tape and Reel	16-TQFN 3mmx3mm

[†] Future Product

Copyrights

Copyright © 1997-2007, austriamicrosystems AG, Schloss Premstaetten, 8141 Unterpremstaetten, Austria-Europe. Trademarks Registered ®. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

All products and companies mentioned are trademarks or registered trademarks of their respective companies.

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.



Contact Information

Headquarters

austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

<http://www.austriamicrosystems.com/contact>