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IC DESIGN SPECIFICATION
1.3-V microPower™ DSP/μC VOICE BAND AUDIO CODEC

FEATURES

- **Single Channel Codec**
- **Noise Shaped Delta Sigma ADC and DAC Technology**
- **Low Supply Voltage and Current:**
  - **1.3-V Typical Power Supply**
  - **350-μA Typical Supply Current Drain**
- **Power Supply Up Monitor and Low Battery Monitor That Also Automatically Shuts Off H-Bridge Output When Battery Decays Below 1.05 V in a Nontransient Manner**
- **Typical 2.4-μVrms Input Referred Noise With 0.01% Total Harmonic Distortion for Front End and 108-dB Dynamic Range**
- **ADC Has 87-dB Dynamic Range With 73-dB Total Harmonic Distortion 100 Hz–10 kHz, 40-kHz Sampling Rate**
- **Typical 55-dB PSRR 100 Hz to 10 kHz for Analog Front End**
- **Low Noise Programmable Gain Amplifier/Compressor Front End With Programmable Fast and Slow Attack and Decay Rates With Dual or Single Attack and Decay Rate Option**
- **Typical Output Noise of 12 μVrms With 0.05% Total Harmonic Distortion for Delta Sigma DAC and H-Bridge Output Driver**
- **Low Jitter Oscillator That Generates all Internal Clocks and Generates 5-MHz Output DSP/μC Clock**
- **Regulated Bandgap Voltage Reference**
- **Programmable Functionality via Digital Serial Interface**
  - **McBSP Interface, DSP Protocol**
  - **TI TMS320VC54x™, TMS320VC55x™ DSPs**
  - **SPI Interface, Microcontroller Protocol**
  - **TI MSP430xx**
- **External Chip Power Down and Reset**
- **Available in:**
  - **32-Pin QFN 5×5-mm Plastic Package**
  - **32-Pad Bumped Die in Waffle Pack (wafer scale packaging), or Tape and Reel, (Preview, Available 3rd Quarter 2003)**

APPLICATIONS

- **Hearing Instruments**
- **Personal Medical Devices**
- **Hearing Protection**
- **Aural Processing**
- **Low-Power Headsets**

DESCRIPTION

The AIC111 IC design specification serves to provide product development teams with a guideline for how the AIC111 IC is specified and programmable options that are available. The document outlines a top-level block description of the IC along with system specifications and functions. Individual block descriptions and target specifications are also outlined.

The Texas Instruments AIC111 is a TI μPower DSP compatible, or microcontroller compatible audio codec product, or analog interface circuit. The AIC111 is part of a comprehensive family of DSP/μC based high-performance analog interface solutions. The AIC111 is targeted primarily at personal medical devices, such as hearing instruments, aural preprocessing applications, and low-power headset applications. The AIC111 is used in any design requiring a programmable time constant PGA/compressor interface, high dynamic range analog-to-digital converter, an external DSP/μC handling signal processing, or a low distortion digital-to-analog converter with a balanced H-Bridge speaker driver. It supports a CMOS digital interface tailored for TI DSPs with the McBSP protocol such as TMS320VC54x™ DSP family and SPI-based controllers such as TI MSP430x family of microcontrollers. The AIC111 also has an external microphone or sensor supply and bias and power supply up low-battery monitor indicator.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

The AIC111 comes in a 32-pin QFN 5×5-mm package. A 32-pad solder ball bumped flip chip die that comes in waffle packs or tape and reel is in preview and will be available 3rd quarter 2003.

AVAILABLE OPTIONS

PART NUMBER	PACKAGE
AIC111RHB	32-pin QFN (5 mm x 5 mm), in tube.
AIC111RHBR	32-pin QFN (5 mm x 5 mm), tape and reel
AIC111YE	32-pad waffle scale chip package, bumped die in waffle pack (contact the factory for availability) – Preview, available 3rd quarter 2003
AIC111YER	32-pad (WSCP) bumped die in tape and reel (contact the factory for availability) – Preview, available 3rd quarter 2003

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

		UNIT
Input voltage	AI or DI pins	–0.3 V to 4 V
Power supply	VDD, power pins	–0.3 V to 4.5 V
Latch-up tolerance	JEDEC latch-up (EIA/JEDS78)	100 mA
Operating free-air temperature range, T_A		0°C to 70°C
Functional temperature range		–15°C to 85°C
Reflow temperature range (flip chip)		220°C to 230°C
Storage temperature range, T_{stg}		–40°C to 125°C
Storage humidity		65% R.H.

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Specifications are assured operating at maximum device limits for QFN package only, unless otherwise specified.

ELECTRICAL CHARACTERISTICS

INPUT/OUTPUT, OPERATING TEMPERATURE AT 25°C						
PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
Digital interface (see Notes 1 and 2)	BUF_DVDD (see Note 1)				3.6	V
V_{IH} High-level input voltage				BUF_DVDD–0.2		V
V_{IL} Low-level input voltage				BUF_DVSS+0.2		V
V_{OH} High-level output voltage				BUF_DVDD		V
V_{OL} Low-level output voltage				BUF_DVSS		V
Maximum allowed input voltage (AVIN)	Differential				450	mVpk
Input impedance (AVIN) (see Note 3)	Nominal gain = 50x			20		kΩ
Input capacitance (AVIN)				5		pF
Microphone bias voltage (MIC_VSUP)	20-μA maximum		0.87	0.94	0.99	V
Microphone bias resistor (MIC_BIAS)			27	29.1	31	kΩ
H-bridge amplifier output	DAC full scale output differential	Fixed Q		3/4 HB_VDD		V_{PP}
		Adaptive Q		HB_VDD		
Output resistance	Differential, HB – V_{DD} = 1.3 V			20 or 40		Ω

(1) DVDD, VDD_OSC, and AVDD should be within 50 mV, preferably connected together.
AVSS1, 2, DVSS, and VSS_OSC should be within 50 mV, preferably connected together.

(2) Maximum (0.9 V, DVDD –0.5 V) ≤ BUF_DVDD ≤3.6 V

(3) Driving single-ended: Rin = R × [(1+A)/(2+A)], A = PGAC Gain (linear), R = 20.4 kΩ for A ≥ 4 or 20.4 kΩ × (4/A) for A<4. Rin(min) = 17 kΩ (A=4), Rin(max) = 59.89 kΩ (A = 0.89), Rin(nom) = 20 kΩ (A = 50).

TERMINAL ASSIGNMENTS

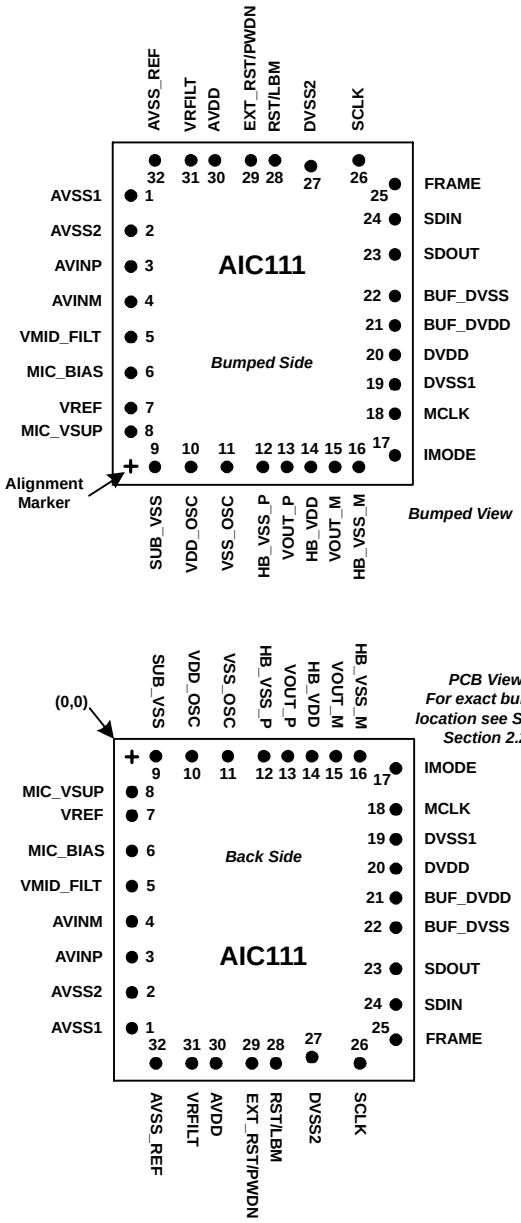


Figure 1. AIC111YE Bumped View and PCB Flipped Pin Placements

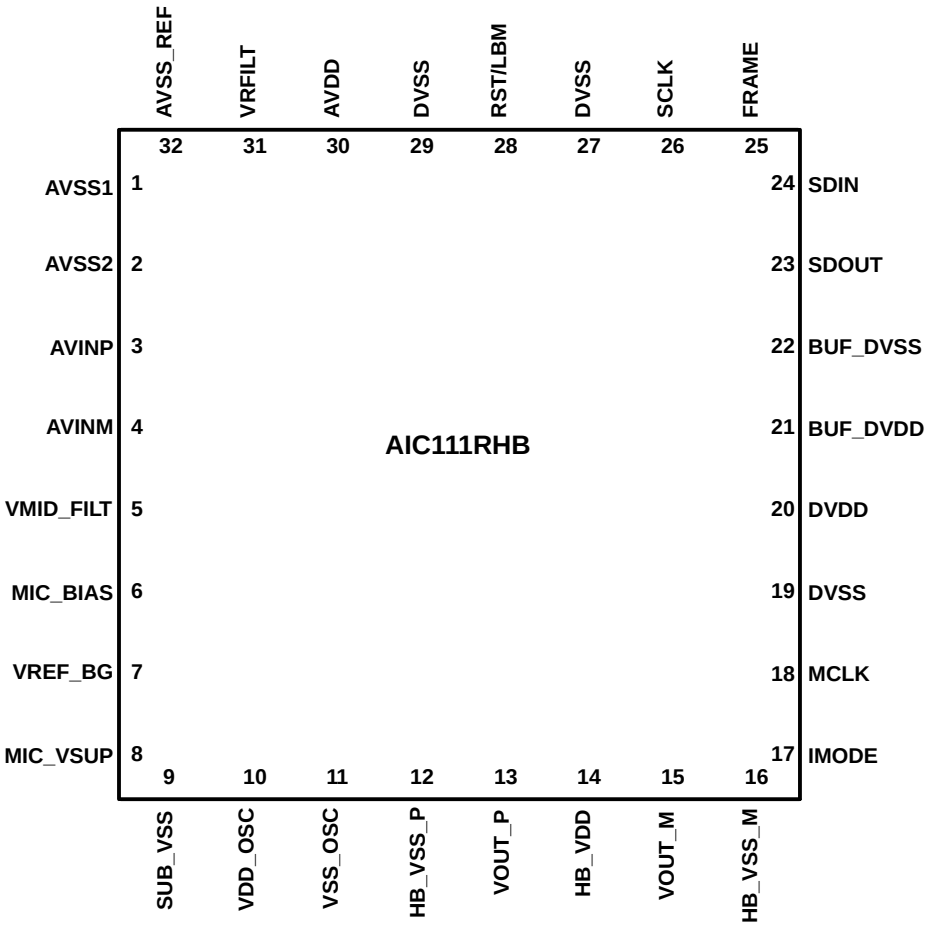
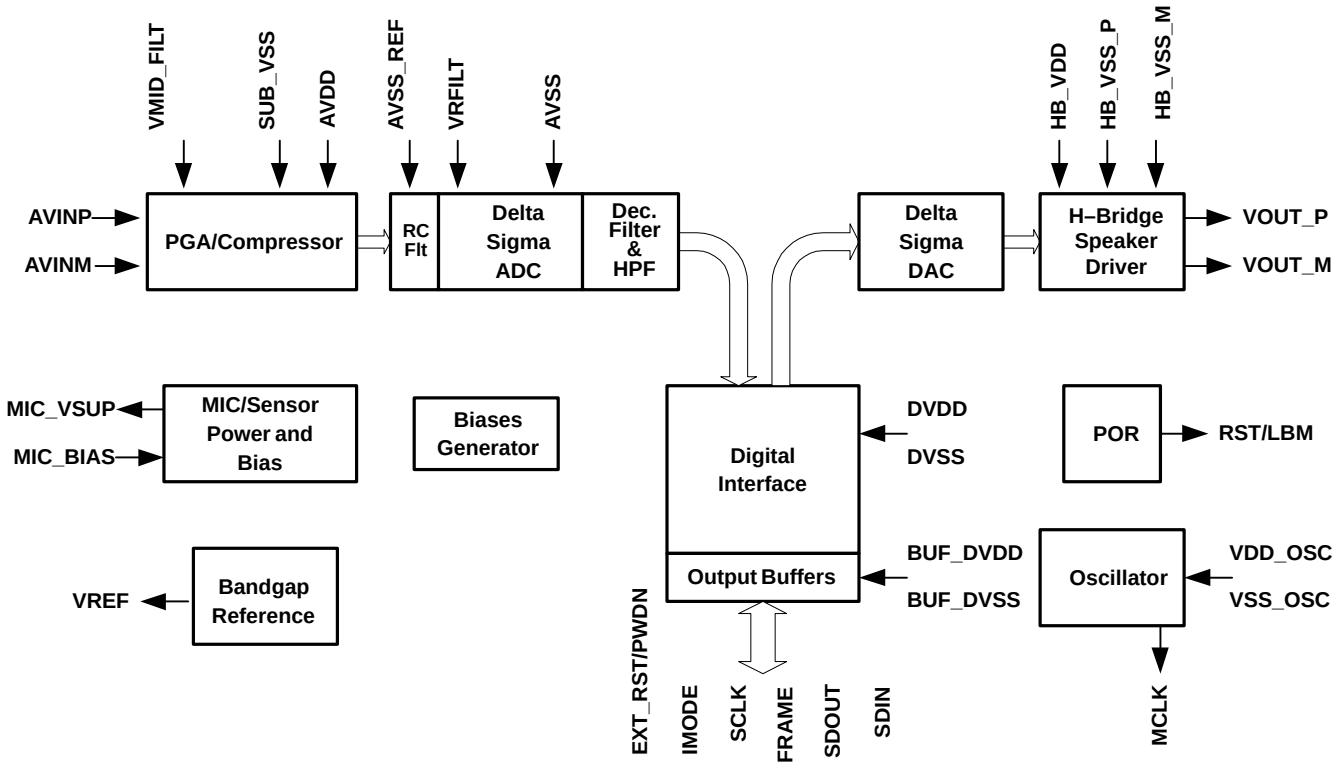


Figure 2. AIC111RHB 32-Pin QFN Pinout

Terminal Functions

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	AVSS1	GND	Ground return for ADC analog circuits
2	AVSS2	GND	Ground return for PGAC and MIC power analog circuits
3	AVINP	AI	Noninverting differential analog input coupled through an external 1-μF capacitor to external microphone output
4	AVINM	AI	Inverting differential analog signal input coupled through an external 1-μF capacitor to ground
5	VMID_FILT	AO	Midsupply ac ground reference filter pin bypassed by a 1-μF capacitor connected to ground
6	MIC_BIAS	AO	Source connection of external microphone source follower preamp. (Provides 29.1 kΩ to AVSS2)
7	VREF	AO	Bandgap reference output bypassed by external 1-μF VREF filter capacitor
8	MIC_VSUP	AO	Supply voltage for external microphone source follower preamp bypassed with an external 0.1-μF capacitor
9	SUB_VSS	GND	Isolated substrate VSS for analog circuits
10	VDD_OSC	VDD	Power pin for internal oscillator
11	VSS_OSC	GND	Ground return for internal oscillator
12	HB_VSS_P	GND	Ground return for noninverting stack of H-bridge amplifier
13	VOUT_P	AO	Noninverting H-bridge output voltage
14	HB_VDD	VDD	Power pin for H-bridge amplifier
15	VOUT_M	AO	Inverting H-bridge output voltage
16	HB_VSS_M	GND	Ground return for inverting stack of H-bridge amplifier
17	IMODE	DI	Digital interface format selection pin
18	MCLK	DO	5-MHz output clock for external DSP/μC
19	DVSS1	GND	Ground return for digital circuits
20	DVDD	VDD	Power pin for digital circuits
21	BUF_DVDD	VDD	Power pin for interface digital I/O circuits
22	BUF_DVSS	GND	Ground return for interface digital I/O circuits
23	SDOUT	DO	Digital interface serial data output pin
24	SDIN	DI	Digital interface serial data input pin
25	FRAME	DO	Digital interface serial data framer
26	SCLK	DO	Digital interface serial shift clock
27	DVSS2	GND	Ground return for digital circuits
28	RST/LBM	DO	Provides external reset and low battery monitor
29	EXT_RST/PWDN	DI	Powers down all analog blocks and holds digital outputs low until internal system is up
30	AVDD	VDD	VDD power pin for analog circuits
31	VRFILT	AO	Positive ADC reference pin bypassed with 1-μF capacitor to AVSS_REF
32	AVSS_REF	GND	Ground for ADC voltage reference

FUNCTIONAL BLOCK DIAGRAM



OPERATION

The power source may be a zinc-air battery operating at a typical voltage of 1.3 V. A single external de-coupling capacitor of 1 μF is recommended on the main power supply.

VOLTAGE and CURRENT, OPERATING TEMPERATURE AT 25°C					
PARAMETER	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
AVDD, DVDD (All pins of type AVDD, DVDD in pin-out table)	Steady-state battery supply	1.1	1.3	1.5	V
I_S (supply current)	• Unloaded: H-Bridge output open • Microphone resistor model connected (see Figure 6) • Power supplies = 1.3 V • No receiver attached		350		μA

FUNCTIONAL INPUT CHANNEL PERFORMANCE REQUIREMENTS

The front end is defined as the differential signal path from the PGA/compressor inputs, AVINP, and AVINM through the delta-sigma ADC and decimation filter.

Typical Conditions; deviations are noted in table.

- Operating Temperature Range: 0°C to 70°C. All specification are at 25°C and 1.3 V unless otherwise noted.
- AVDD, DVDD range: 1.1 V to 1.5 V
- AVINP, AVINM inputs: AC coupled, Frequency ranging from 100 Hz–10 kHz
- Measurement Bandwidth: 100 Hz–10 kHz A-weighted.
- Idle channel definition: AVINP and AVINM are both ac-coupled to AVSS.
- Typical PGAC gain range is –1 dB to 40 dB.
- Maximum input voltage: 450 mVpk.

PARAMETER	**TEST CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Broad-band noise	Input referred idle channel		2.4		μV RMS
THD (low level)	AVIN ≤ PGAC threshold (see Note 1)		0.01	0.2%	
DC Offset	Idle channel	–5	0	5	mV
Droop at 10 kHz	Referenced to amplitude at 1 kHz		1.2		dB

(1) PGAC threshold = PGAC threshold voltage/maximum gain of PGAC.

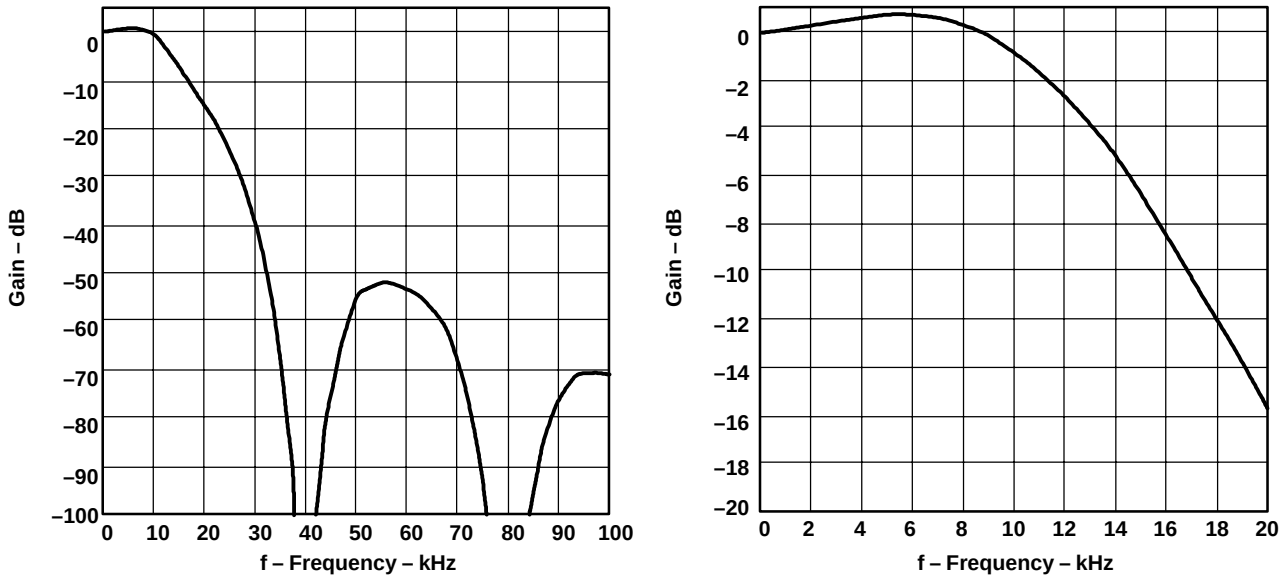


Figure 3. Input Channel Frequency Response With HPF Bypassed

Analog-to-Digital Converter Filtered Input Voltage Reference

Function – Filters analog supply AVDD for DS-ADC reference. With a recommended 0.1-μF external capacitor between pins VRFILT and AVSS_REF, the pole is set at approximately 72 Hz, with 1 μF, the pole is set at approximately 7 Hz.

Programmable Gain Amplifier and Compressor

Function: **T**he programmable gain amplifier and compressor (PGAC) amplifies the microphone or sensor output signal, provides an appropriate impedance to the microphone buffer or sensor, and provides input gain compression limiting depending on the input signal level if one is not using the fixed gain mode, where the PGAC gain is set by selected register bits. Input compression limiting is discrete automatic gain correction (AGC) based on detecting the peak input signal level using a peak detector circuit that has programmable time responses to provide AGC control, and is intended to prevent a steady state input level up to the defined PGAC limit from being clipped. The attack/release times of the PGAC are programmable by internal clock selection inside the PGAC digital level circuitry that affects the rate of gain changes.

The PGAC has four modes of operation: automatic dual-rate (default), automatic single-rate, fixed single-rate, and fixed immediate. Mode selection is controlled by bits 3 and 2 of the PDCREG register.

Automatic dual-rate mode (00, default):

In this mode of operation, the PGAC has two attack (gain decrease) rates and two release (gain increase) rates, which may be selected by programming the FASTARREG and FORMAT4 registers. Internally, two counters are used to control the compressor gain. The fast rate counter responds at the fast attack and release rates, and it counts down at the attack rate to decrease the PGAC gain if the output of the PGAC is instantaneously larger than a preset threshold (PGAC_THRES = 400-mV peak), or it counts up to increase the gain, up to the maximum allowed gain as set by the PGACREG register, if the output of the PGAC falls below a second threshold, which is 3 dB lower (283-mV peak), which provides hysteresis. Before the gain is allowed to increase, the signal at the output of the PGAC must be below the lower threshold for a period of time which is controlled by bit 4 of PDCREG, and can be 50 ms (0, default) or 25 ms (1). The slow-rate counter responds at the slow attack and release rates, and it attempts to track the state of the fast rate counter. The PGAC gain is determined by whichever counter is smaller. In this way, the PGAC can respond and recover rapidly to short signal bursts while responding more slowly to the signal average.

Automatic single-rate mode (01):

In this mode of operation, the PGAC has one attack rate and one release rate, which may be selected by programming the FASTARREG register. The operation of the PGAC is similar to the dual-rate mode, except that the slow-rate counter is disabled and the PGAC gain is solely determined by the fast-rate counter.

Fixed single-rate mode (10):

In this mode of operation, the PGAC gain tracks the value specified in the PGACREG register regardless of the signal amplitude, and changes in PGACREG cause the gain to decrease or increase at the corresponding fast attack or release rate specified in the FASTARREG register.

Fixed immediate mode (11):

In this mode of operation, the PGAC gain tracks the value specified in the PGACREG register regardless of the signal amplitude, and changes in PGACREG cause the gain to change immediately to the desired gain without stepping through the intermediate gain states.

Bit 7 of the PGACREG register controls the PGAC gain read mode. While this bit is low (default), reading PGACREG returns the contents of PGACREG. However, if this bit is set high, then any subsequent read(s) of PGACREG returns the actual, instantaneous PGAC gain. This information may be useful, for example, for dynamic range expansion, effectively undoing the compression effect in the automatic modes of operation.

Characteristics: Compression limits the PCAG output. PGACREG is a programmable register.

Specifications at 25°C, AVDD = 1.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Signal Parameters					
Maximum signal swing	Gain = –1 dB		900		mV_{PP}
Block Parameters					
Gain size step		0.3	0.5	0.7	dB

(1) Based on a system clock of 1.280 MHz.
(2) For fixed gain mode the rate is 80 KdB/s to new programmed value of gain. All intermediate 0.5 dB gain steps are passed through to reach new gain.

Delta Sigma A/D Converter/Anti-alias Filter

Function: Converts the PGAC differential output to a digital word with an equivalent dynamic range of approximately 14 bits.

Characteristics: The delta sigma ADC has a 64 oversampling ratio, a 1.28-MHz master clock, and a 40-kHz output data rate. Digital coding is 2s complement. Tones are at least 12 dB below broadband noise level. Full-scale signal range corresponds to $+2^{15} –1$, $–2^{15}$

Specifications at 25°C, AVDD = 1.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Block parameters					
Dynamic range	–3 dB rel. to reference		87		dB
Input sample rate			1.28		MHz
Output sample rate			40		kHz
THD	BW: 100 Hz–10 kHz		85		dB

Digital High-Pass Filter

Function: Provide a high-pass filter in ADC signal path. The high-pass filter (HPF first order) removes dc offsets introduced into the channel. FORMAT1 register selections for a 50 Hz, 100 Hz, or bypass are available.

Characteristics: Programmable selections for a 50 Hz, 100 Hz, or bypass are available. The default HPF pole is 50 Hz.

Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HPF corner frequency	–3 dB nom mode		50		Hz

Delta Sigma DAC

Function: Generates an over-sampled bit string to drive the H-bridge output amplifier such that when filtered reproduces the desired analog waveform.

Characteristics: A 32 times over-sampled modulator multi-bit design.

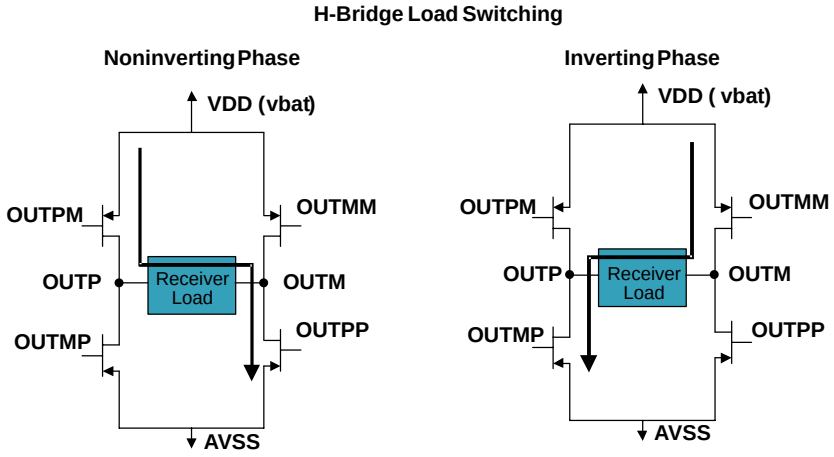
Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$fd_{(input\_data)}$	Signal; BW = 10 kHz		40		kHz
f_{clk}			640		kHz

H-bridge Output Driver

Function: An H-bridge output driver efficiently converts the delta sigma DAC modulator output signals. The external load provides the low-pass filtering that recovers the differential analog signal from the H-bridge.

Characteristics: Standard H-bridge configuration with transistors sized to differentially drive the load impedance. The load impedance is complex and a function of frequency.



NOTE: VDD does not necessarily have to be connected to the same potential as AVDD, it could be connected to a higher potential than AVDD, equal to AVDD, but not less than AVDD.

Figure 4. Definition of Phase and Output Switching Current Polarity

Specifications at 25°C, HB_VDD = 1.3 V

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Block Parameters						
DC offset	Idle channel; Differential across VOUT_P and VOUT_M		–5	0	5	mV
Broadband noise	Idle channel, measured at output of channel, BW = 100 Hz–10 kHz, HB_VDD = 1.3 V, A-weighted	Fixed Q		33		µVrms
		Adaptive Q		12		
THD	BW = 100 Hz–10 kHz			0.03%		
Switching frequency				640		kHz
Maximum output swing		Fixed Q		3/4 HB_VDD		V_{PP}
		Adaptive Q		HB_VDD		

Microphone Power Supply

Function: The microphone power supply circuit provides a constant power supply voltage and bias current for the microphone preamp or sensor bias, provides a low-noise voltage reference (ac ground) for the PGAC, provides regulated PGAC comparator threshold levels, provides bandgap regulated POR comparator trip voltage levels, and provides a bandgap regulated current for the biases generator circuit.

Characteristics: The low-dropout regulator configuration or single stage, single-pole amplifier drives an external 0.1-μF capacitor. The regulator does not oscillate under no-load or loaded conditions. The circuit supplies up to 50-μA of continuous current.

Specifications at 25°C, AVDD = 1.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MIC_VSUP	I_L = 20 μA	0.87	0.94	0.97	V
VMID_FILT	0.59 × AVDD		0.78		V
PSRR	0.1-μF external bypass cap from MIC_VSUP to AVSS2.		55		dB
Output impedance			1.5		kΩ

MCLK Output

Function: Provides a clock signal for external use.

Specifications at 25°C, VDD_OSC, DVDD, BUF_DVDD = 1.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency		4.7	5.12	5.5	MHz
Jitter	RMS jitter		150		ps
Duty cycle			50%		

Power-On Reset

Function: Provides a reset signal upon power up (stable voltage reference) that initializes the digital interface. It also provides a gating signal to the delta-sigma DAC modulator to prevent audible *pops* and *clicks* from erroneous data sent to the H-bridge circuit at power up and during periods when battery voltage has degraded below 1.05 V for an extended period of time (typically greater than 44 μs). The reset signal is asynchronous to MCLK. Digital interface does not start operating until after $t_{(VDD)_}$valid has transpired.

POR has to:

- Deal with system's on/off switch bounce lasting 100 ms or less.
- Detect when the power supply AVDD is ≥1.1 V to enable the H-bridge output.
- Provide kick-start to oscillator.
- Detect when VDD degrades below 1.05 V for a period of time that is nontransient, and gate H-bridge output.

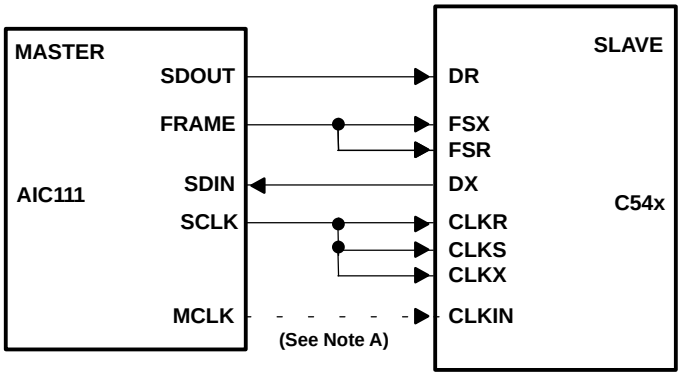
Specifications at 25°C, AVDD = 1.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(VDD)_}$valid: Time VDD considered valid at powerup after switch bounce has settled.	V_{DD} > 1.1 V		100		ms
Allowed transient spike below 1.05 V before H-bridge output and digital interface are not asserted.	V_{DD} < 1.05 V		44		μs
POR on			1.1		V
POR off			1.05		

DIGITAL INTERFACE

Function: The digital interface can be selected (IMODE=LOW) as a serial audio/control interface (SACI), which is the McBSP DSP-codec protocol, or (IMODE=HIGH), a serial peripheral interface (SPI). Either SACI or SPI sends out a 16-bit audio stream from the Δ–Σ ADC and receives a 20-bit audio stream going to the Δ–Σ DAC/H-Bridge. Several control functions, READ/WRITE to user registers, are also included totaling five 8-bit registers. Four pins, SCLK, FRAME, SDIN and SDOUT, are employed in SACI or SPI. An internal register map exists that contains read/write program registers for a variety of FORMAT (user) settings. The register bits that are designated *not used* will always read back zero or voltage level VSS regardless of what is written to them.

DIG INTERFACE PIN	I/O	DESCRIPTION
SCLK	Output	Bit shift clock. SCLK has an internal pull down.
FRAME	Output	Data frame sync: controls the separation of audio channels and provides a reset/synchronization to the interface's internal state machine. FRAME has an internal pull down.
SDIN	Input	Serial audio/control data input pin.
SDOUT	Input	Serial audio/control data output pin.
IMODE	Input	Interface protocol selection pin. LOW=SACI, HIGH=SPI.
MCLK	Output	Clock output pin.



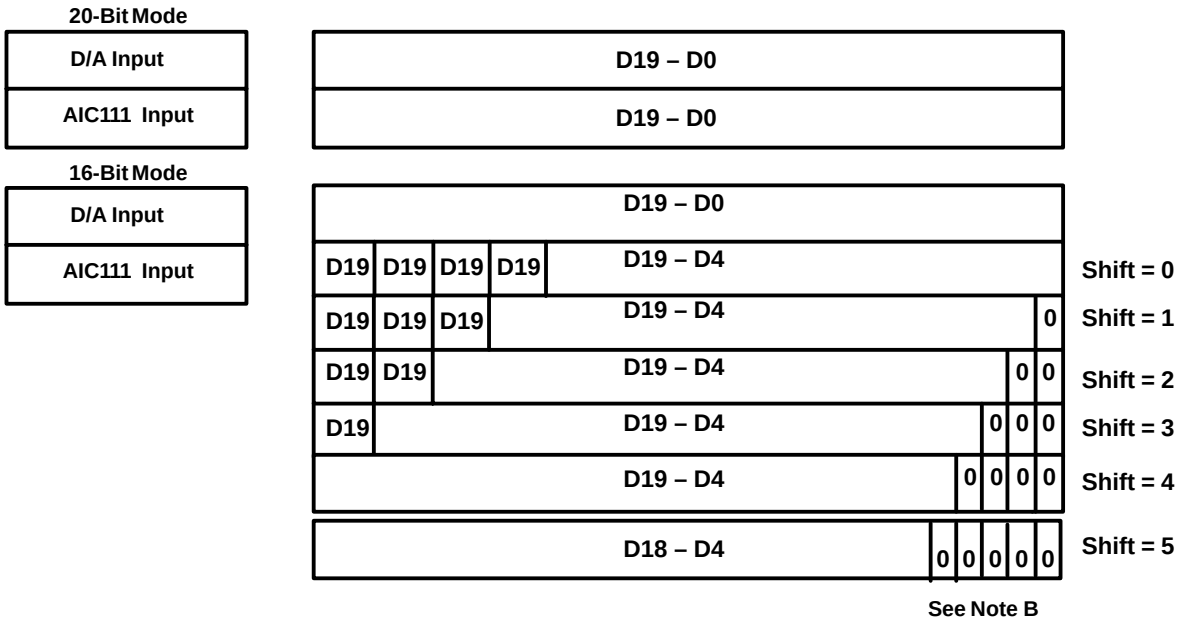
NOTE A: The dotted line indicates the connection is not essential for communication to work.

Figure 5. AIC111 McBSP DSP-Codec Interface

McBSP DSP-Codec (SACI) Protocol

Use this protocol when interfacing to TI DSPs.

- The SACI works in a master mode.
- SCLK = 1.28 MHz. FRAME (= 40 kHz) has a 50% duty cycle. FRAME is an output.
- 32-bit control/audio data, written on the SDIN pin, consist of a 20-bit audio word going to the Δ–Σ DAC, and a 12-bit control word.
- DAC input has two modes of operation, a 20-bit mode, and a 16-bit mode.
- The 12-bit control word consists of: a R/W bit, 3 address bits, and 8-bits of control register content. Note that the R/W bit is defined as 0=READ, and 1=WRITE.
- When the 3 address bits are all zeros, the control function of the SACI is disabled.
- 24-bit audio/control data, read from the SDOUT pin, consist of one 16-bit output from the Δ–Σ ADC followed by an 8-bit control word.
- All data/control words are formatted as the MSB first.



NOTE B: For 5-bit left shift, digital word is limited to 15 bits with sataration.

Figure 6. AIC111 Data Output

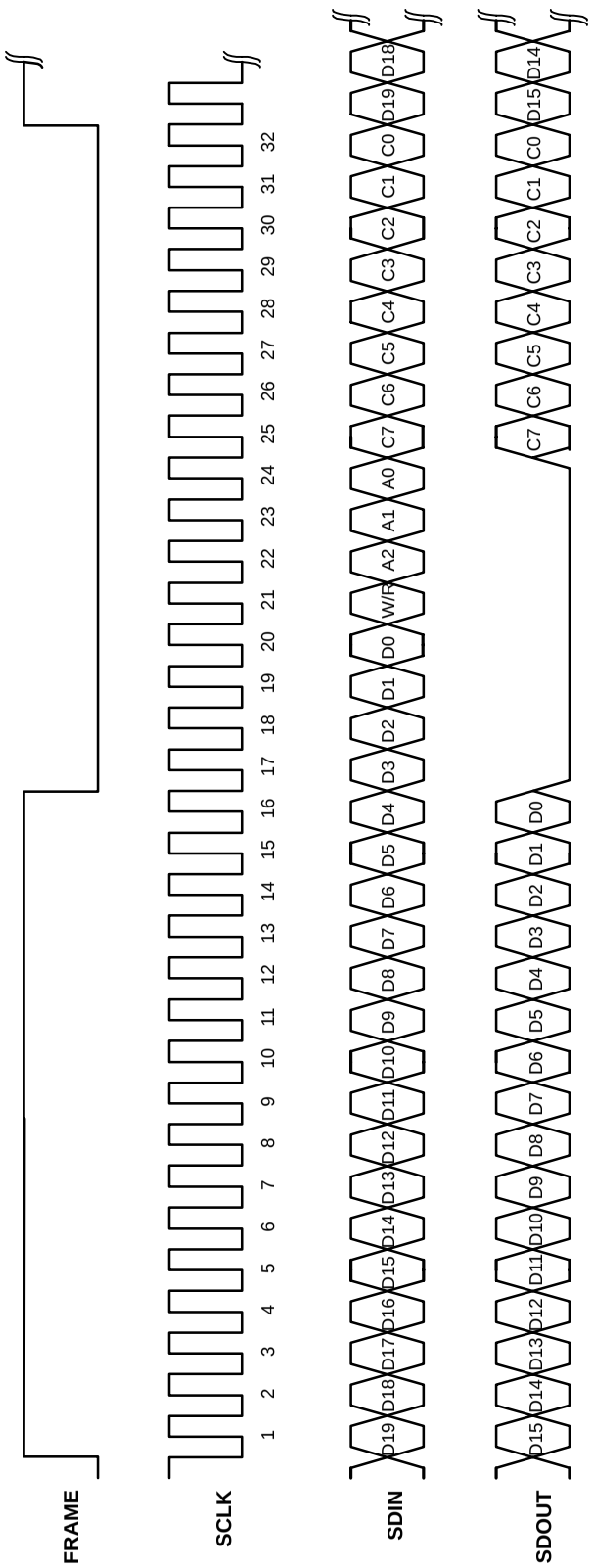


Figure 7. AIC111 DSP-Codec (SACI) Signals (Read = 0, Write = 1)

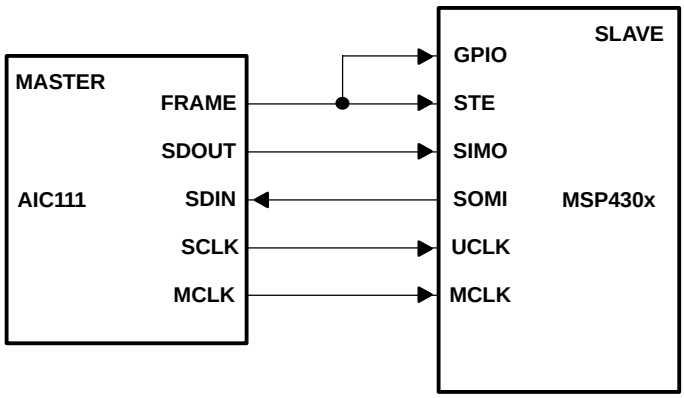
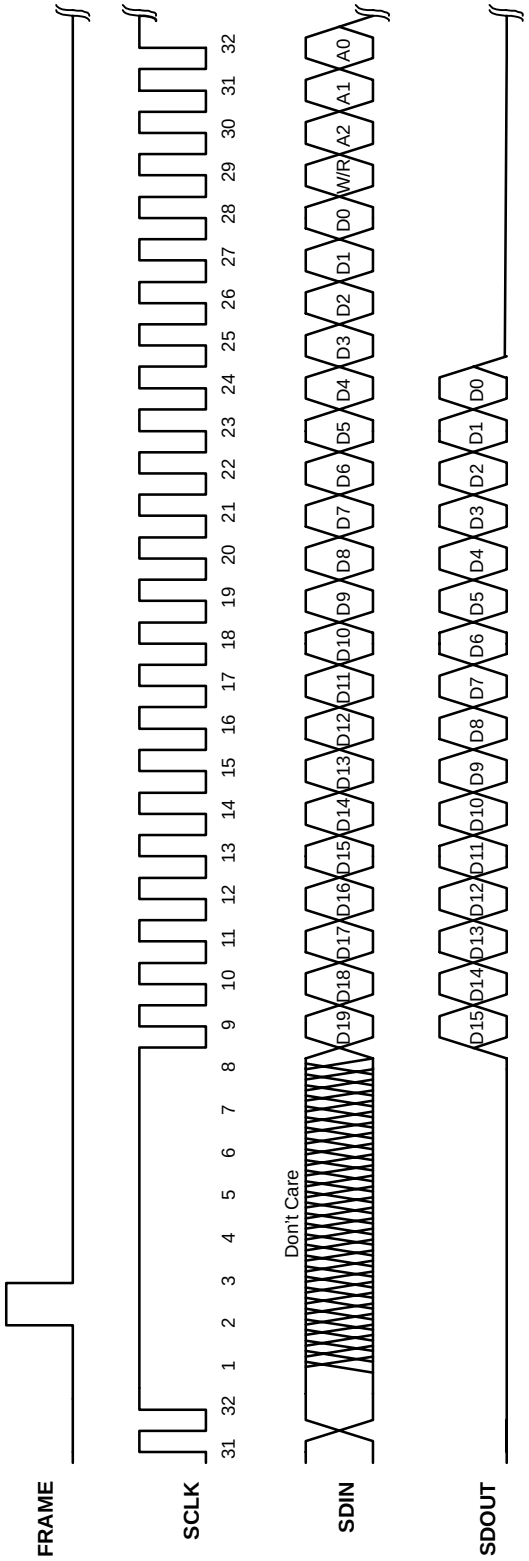


Figure 8. AIC111 SPI I/O Diagram

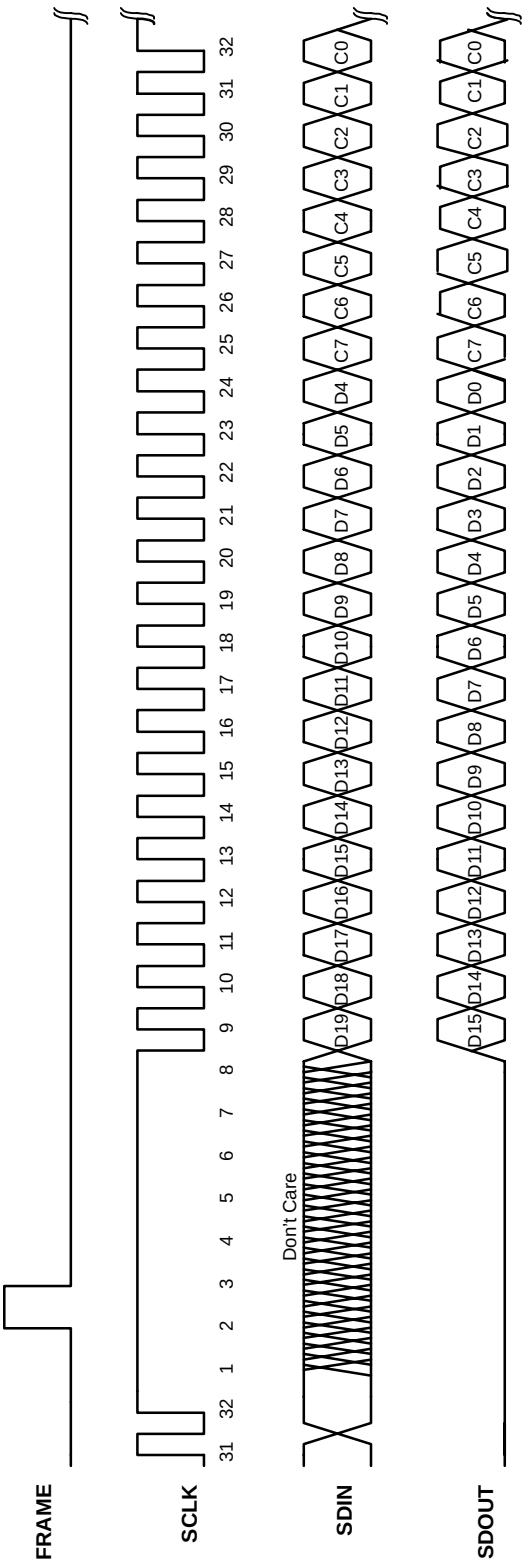
SPI Protocol

- AIC111 can also implement a master SPI protocol.
- SCLK supplies a bit shift clock of 1.28 MHz to the SPI port of a slave device.
- FRAME must be in the active *low* state prior to data transaction and must stay *low* for the duration of data transaction. Before communication, there are eight silent cycles on SCLK. During this period FRAME also sends a pulse to reset the slave device.
- When the control function is not required, the AIC111 transmits a 16-bit audio word to and receives a 20-bit audio word from the slave device in every FRAME cycle.
- A WRITE/READ of an 8-bit user register (address 0x01 to 0x07) takes two FRAME cycles.
- All data/control words are formatted as the MSB first.



NOTE: If A2, A1, and A0 = 0, one gets audio data only and W/R is a don't care. If in the previous frame A2, A1, and A0 = 0, then one gets both audio and control data depending on the W/R bit defined as Read = 0 and Write = 1.

Figure 9. AIC111 SPI Signals



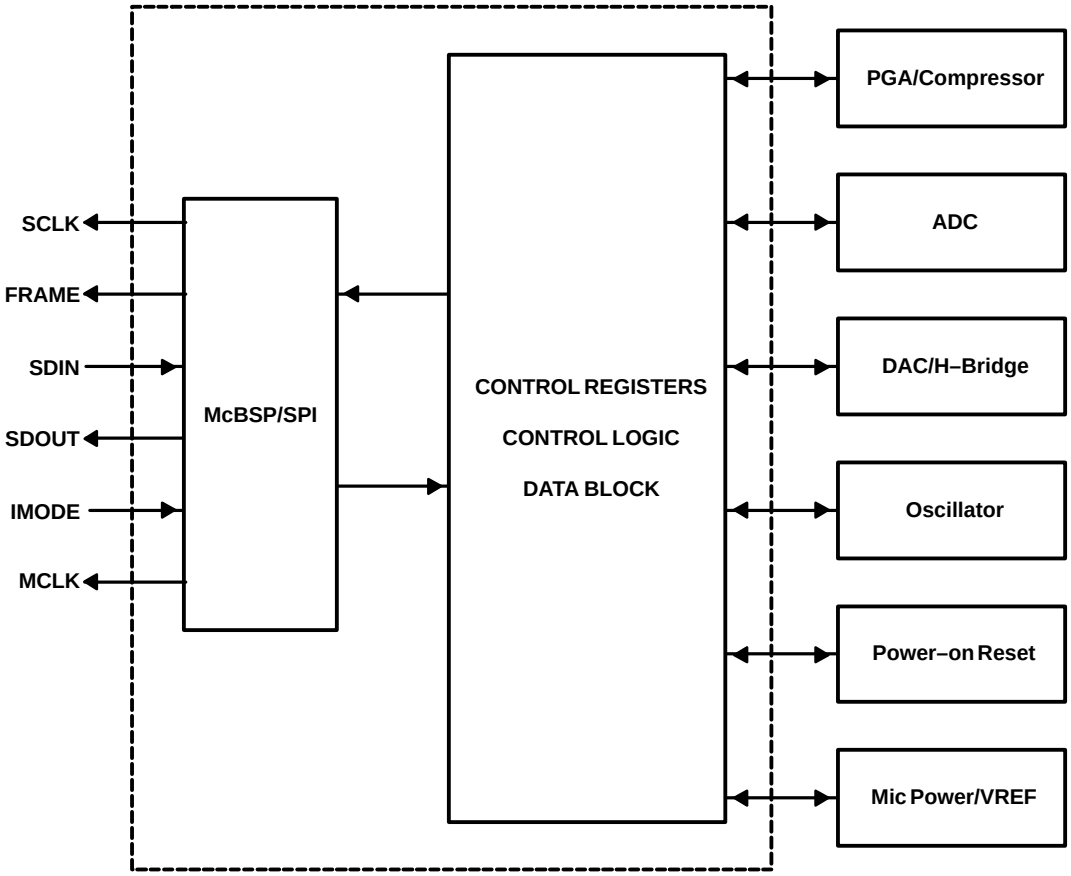
NOTE: SDIN shows writing to A2, A1, and A0 specified from the previous frame. SDOUT shows reading from A2, A1, and A0 specified from a different previous frame.

Figure 10. AIC111 SPI Signals

Digital Interface Timing

PARAMETER		MIN	TYP	MAX	UNIT
F_sclk	SCLK frequency		1.28		MHz
F_frame	FRAME frequency		F-sclk/32		MHz

Digital Interface Block Diagram



Register Map and Register Bit Definitions

ADDRESS	REGISTER NAME	DETAILED DESCRIPTION
0x00	Reserved	Reserved for future use
0x01	PGACREG	PGAC gain register
0x02	HPFSFTREG	HPF and shift control register
0x03	PDCREG	Power-down control register
0x04	FASTARREG	Fast attack/release rate control register
0x05	SLOWARREG	Slow attack/release rate control register
0x06–07	Reserved	Reserved for future use

NOTE: Do not write to the reserved registers.

PGACREG

BIT	NAME	FUNCTION DEFAULT=0x46
7	PGAC_READ_MODE	Select register contents or actual gain to read 0: Read FORMAT0 register contents (default) 1: Read actual PGAC gain
6:0	PGAC_GAIN [6:0]	PGAC gain adjustment (0.5 dB steps). A full table is found in the *Appendix Section* of this data sheet. 0x52 = +40.0 dB 0x51 = +39.5 dB 0x50 = +39.0 dB … 0x46 =+34.0 dB (default) …. 0x01 = –0.5 dB 0x00 = –1.0 dB

HPFSFTREG

BIT	NAME	FUNCTION DEFAULT=0x11
7	DBUFF_EN	Enable weak (1/2 strength) dig I/O buffer
6:5	HPF_CTL [1:0]	Control bits for high-pass filter 00: normal mode 01: HPF bypass 10: 100 Hz corner frequency 11: Not used
4:2	SHIFT [2:0]	Select shift bits when ADC 16-b output is used as DAC 20-b input. 000: no shift –24 db gain 001: 1b left shift –18 dB gain 010: 2b left shift –12 dB gain 011: 3b left shift –6 dB gain 100: 4b left shift (default) 0 dB gain 101: 5b left shift +6 dB gain 11X: 5b left shift
1:0	DAC_MODE	Select DAC mode of operation. 00: DAC off, powered down 01: 16-bit input goes through shifter (default) 10: 20-bit input bypasses shifter 11: ADC→DAC digital loopback

PDCREG

BIT	NAME	FUNCTION DEFAULT=0x00
7	DAC_ADAPTIVE_Q	0 = fixed quantization, 1 = adaptive quantization
6	HB_OUT_EN	H-bridge output enable
5	HB_DRIVE	H-bridge drive strength, 0 = 40 Ω, 1 = 20 Ω
4	HIST_TIMEOUT_SEL	PGAC hysteresis timeout select 0: 50 ms (default) 1: 25 ms
3:2	PGAC_GAIN_MODE	Set gain mode of PGAC 00: Automatic, dual rate (default) 01: Automatic, single rate 10: Fixed, single rate 11: Fixed, immediate
1	MIC_VSUP_PD	Power down MIC_VSUP
0	FRONTEND_PD	Power down PGAC+ADC

FASTARREG PGAC Fast Rates

BIT	NAME	FUNCTION	DEFAULT=0xF7
7:4	ATTACK<7:4>	1111: Attack rate = 80000 dB/s 1110: Attack rate = 40000 dB/s 1101: Attack rate = 20000 dB/s 1100: Attack rate = 10000 dB/s 1011: Attack rate = 5000 dB/s 1010: Attack rate = 2500 dB/s 1001: Attack rate = 1250 dB/s 1000: Attack rate = 625 dB/s 0111: Attack rate = 312.5 dB/s 0110: Attack rate = 156.25 dB/s 0101: Attack rate = 78.13 dB/s 0100: Attack rate = 39.1 dB/s 0011: Attack rate = 19.53 dB/s 0010: Attack rate = 9.77 dB/s 0001: Attack rate = 4.88 dB/s 0000: Attack rate = 2.44 dB/s	
3:0	RELEASE<3:0>	1111: Release rate = 80000 dB/s 1110: Release rate = 40000 dB/s … 0001: Release rate = 4.88 dB/s 0000: Release rate = 2.44 dB/s	

SLOWARREG PGAC Slow Rates (Dual Rate Mode Only)

BIT	NAME	FUNCTION	DEFAULT=0x42
7:4	ATTACK<7:4>	1111: Attack rate = 80000 dB/s 1110: Attack rate = 40000 dB/s … 0001: Attack rate = 4.88 dB/s 0000: Attack rate = 2.44 dB/s	
3:0	RELEASE<3:0>	1111: Release rate = 80000 dB/s 1110: Release rate = 40000 dB/s … 0001: Release rate = 4.88 dB/s 0000: Release rate = 2.44 dB/s	

APPENDIX

PGAC GAIN

PGAC GAIN VALUES				
	BUS NAME	**HEX VALUE**	**BINARY**	**GAIN (DB)**
PGAC	PGAC_GAIN<6:0>	0x52	1010010	40
		0x51	1010001	39.5
		0x50	1010000	39
		0x4F	1001111	38.5
		0x4E	1001110	38
		0x4D	1001101	37.5
		0x4C	1001100	37
		0x4B	1001011	36.5
		0x4A	1001010	36
		0x49	1001001	35.5
		0x48	1001000	35
		0x47	1000111	34.5
		0x46	1000110	34
		0x45	1000101	33.5
		0x44	1000100	33
		0x43	1000011	32.5
		0x42	1000010	32
		0x41	1000001	31.5
		0x40	1000000	31
		0x3F	0111111	30.5
		0x3E	0111110	30
		0x3D	0111101	29.5
		0x3C	0111100	29
		0x3B	0111011	28.5
		0x3A	0111010	28
		0x39	0111001	27.5
PGAC	PGAC_GAIN<6:0>	0x38	0111000	27
		0x37	0110111	26.5
		0x36	0110110	26
		0x35	0110101	25.5
		0x34	0110100	25
		0x33	0110011	24.5
		0x32	0110010	24
		0x31	0110001	23.5
		0x30	0110000	23
		0x2F	0101111	22.5
		0x2E	0101110	22
		0x2D	0101101	21.5
		0x2C	0101100	21
		0x2B	0101011	20.5
		0x2A	0101010	20
		0x29	0101001	19.5
		0x28	0101000	19
		0x27	0100111	18.5
		0x26	0100110	18
		0x25	0100101	17.5
		0x24	0100100	17
		0x23	0100011	16.5

PGAC GAIN VALUES				
	BUS NAME	**HEX VALUE**	**BINARY**	**GAIN (DB)**
PGAC (Continued)	PGAC_GAIN<6:0>	0x22	0100010	16
		0x21	0100001	15.5
		0x20	0100000	15
		0x1F	0011111	14.5
		0x1E	0011110	14
		0x1D	0011101	13.5
		0x1C	0011100	13
		0x1B	0011011	12.5
		0x1A	0011010	12
		0x19	0011001	11.5
		0x18	0011000	11
		0x17	0010111	10.5
		0x16	0010110	10
		0x15	0010101	9.5
		0x14	0010100	9
		0x13	0010011	8.5
		0x12	0010010	8
		0x11	0010001	7.5
		0x10	0010000	7
		0x0F	0001111	6.5
		0x0E	0001110	6
		0x0D	0001101	5.5
		0x0C	0001100	5
		0x0B	0001011	4.5
		0x0A	0001010	4
		0x09	0001001	3.5
		0x08	0001000	3
		0x07	0000111	2.5
		0x06	0000110	2
PGAC	PGAC_GAIN<6:0>	0x05	0000101	1.5
		0x04	0000100	1
		0x03	0000011	0.5
		0x02	0000010	0
		0x01	0000001	–0.5
	Default	0x00	0000000	–1

TI TMS320C54xx APPLICATION CIRCUIT

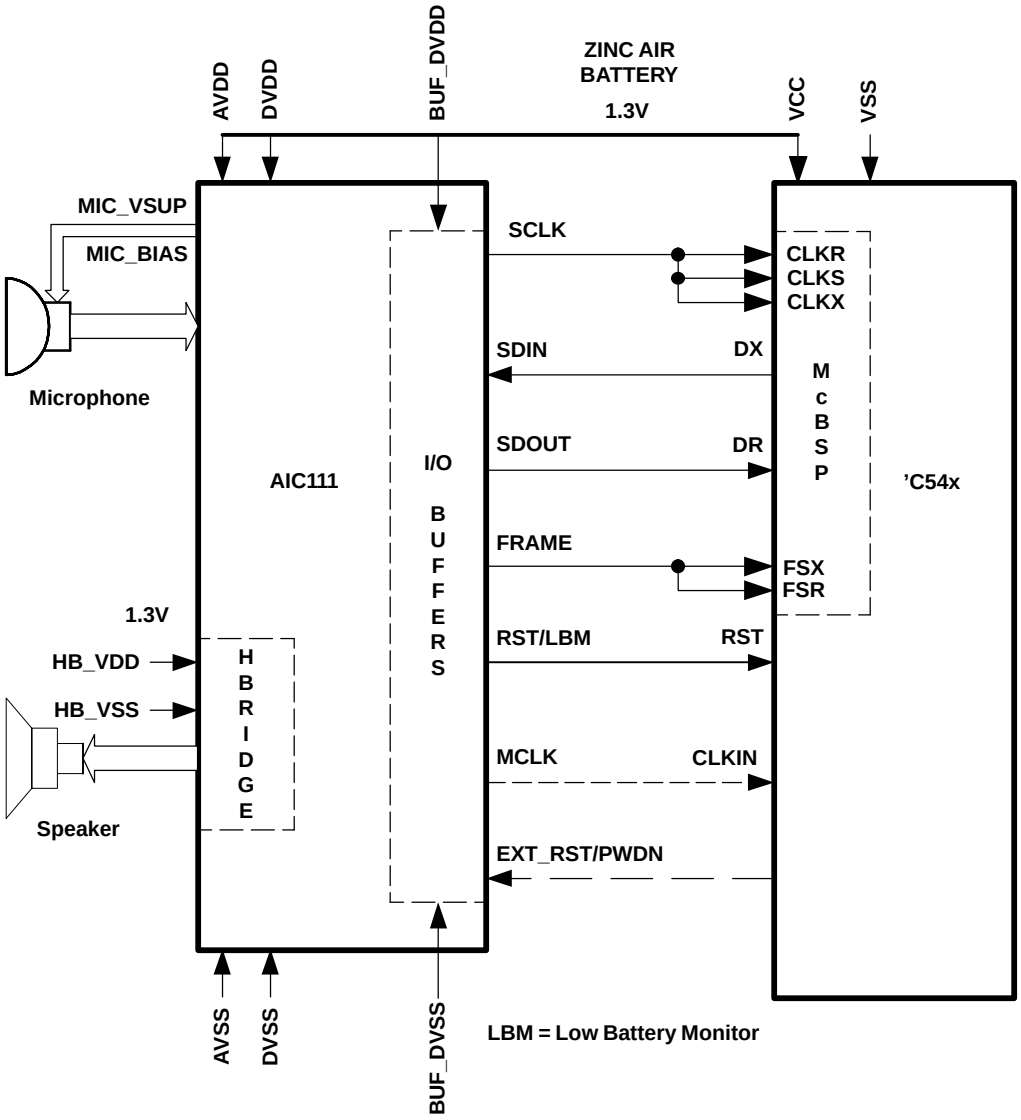
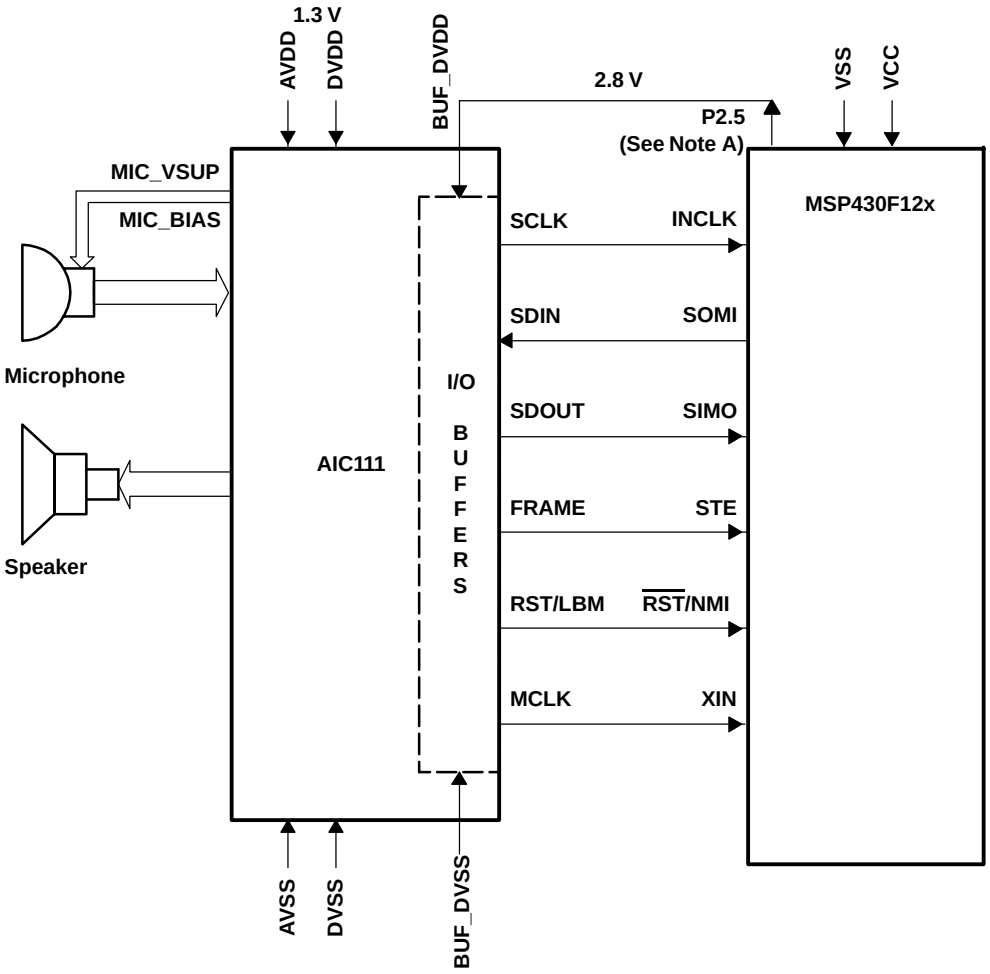


Figure 11. Interfacing to the TMS320C54xx for a Hearing Aid Application

Required external capacitors:

- 1-µF coupling capacitor on AVINP, AVINM
- 1-µF from VMID_FILT to analog ground
- 1-µF from VREF to analog ground
- 0.1-µF from MIC_VSUP to analog ground
- At least 0.1-µF from VRFILT to analog ground. 1-µF from VRFILT to analog ground is recommended.

TI MSP430F12x APPLICATION CIRCUIT



LBM = Low Battery Monitor ’430 Can Also Use
EXT_RST/PWDN to Reset or Power Down the AIC111

Note A: P2.5 enables the MSP430F12x to shut down the AIC111 when desired.

Figure 12. Interfacing to the MSP430F12x for a Hearing Aid Application

MECHANICAL AND ENVIRONMENTAL

Packaging

The AIC111 is available in a 32-pin quad QFN 5x5-mm package. The AIC111 will be available 3rd quarter 2003 as bare solder ball bumped die intended for direct PCB mounting (also known as wafer scale packaging).

- For *QFN packaged part* in tubes order: AIC111RHB.
- For *QFN packaged part* in tape and reel order: AIC111RHBR.
- For *ball bumped die* (in waffle pack) order: AIC111YE (Preview, available 3rd quarter 2003).
- For *ball bumped die* (in tape and reel) order: AIC111YER (Preview, available 3rd quarter 2003).

BOND PAD PITCH AND DIE AREA

Die dimensions		X = 2737.62 µ, Y = 3175.02 µ, **(107.78 mil, 125.0 mil)** **(2,74 mm, 3,18 mm)**		
Maximum die area (includes scribe area)		**13.47kmil^2 (8.69mm^2)**		
Minimum bond pad pitch		202.95 µ or 7.99 mil		
Nearest		PITCH		
PAD (#)	PAD (#)		(micron)	(mil)
7	8		202.950	(7.990)
30	31		202.950	(7.990)
12	13		237.690	(9.358)
14	15		237.690	(9.358)
16	15		237.690	(9.358)
28	29		241.200	(9.496)
18	19		256.410	(10.095)
20	19		256.410	(10.095)
21	20		256.410	(10.095)
22	21		256.410	(10.095)
25	26		287.651	(11.325)
9	10		295.470	(11.633)
10	11		295.470	(11.633)
23	24		306.360	(12.061)
1	32		327.147	(12.880)
32	1		327.147	(12.880)
4	5		356.940	(14.053)
27	28		357.034	(14.056)
17	16		359.453	(14.152)
6	7		369.450	(14.545)
2	1		371.520	(14.627)
3	2		380.700	(14.988)

Number of pins	32			
Pad locations:	**Bond Pad Coordinates**			**Bond Pad Dimensions**
Units: microns	Pad #	Xcenter	Ycenter	Diameter
Dimensions: X = 2737.62 Y = 3175 Bond pad origin: X = 0.000 Y = 0.000 Bond pad offset: X = 0.000 Y = 0.000 (X,Y) = (0,0) is located at the left bottom of the die by pads 8 and 9. See section 1.6, Figure 1–1.	1	154.080	2808.990	70.020
	2	154.080	2437.470	70.020
	3	154.080	2056.770	70.020
	4	154.080	1676.070	70.020
	5	154.080	1319.130	70.020
	6	154.080	938.430	70.020
	7	154.080	568.980	70.020
	8	154.080	366.030	70.020
	9	410.310	162.630	70.020
	10	705.780	162.630	70.020
	11	1001.250	162.630	70.020
	12	1327.860	162.630	70.020
	13	1565.550	162.630	70.020
	14	1803.240	162.630	70.020
	15	2040.930	162.630	70.020
	16	2278.620	162.630	70.020
	17	2574.990	366.030	70.020
	18	2574.990	782.550	70.020
	19	2574.990	1038.960	70.020
	20	2574.990	1295.370	70.020
	21	2574.990	1551.780	70.020
	22	2574.990	1808.190	70.020
	23	2574.990	2188.890	70.020
	24	2574.990	2495.250	70.020
	25	2574.990	2808.990	70.020
	26	2371.590	3012.390	70.020
	27	1910.430	2994.390	70.020
	28	1553.850	3012.390	70.020
	29	1312.650	3012.390	70.020
	30	955.530	3012.390	70.020
	31	752.580	3012.390	70.020
	32	410.310	3012.390	70.020

DIE THICKNESS

	TYPICAL	TOLERANCE
Final die thickness Z (without solder bump)	29.59 mil or 725 μm	±0.79 mil or 20 μm

SOLDER BUMP

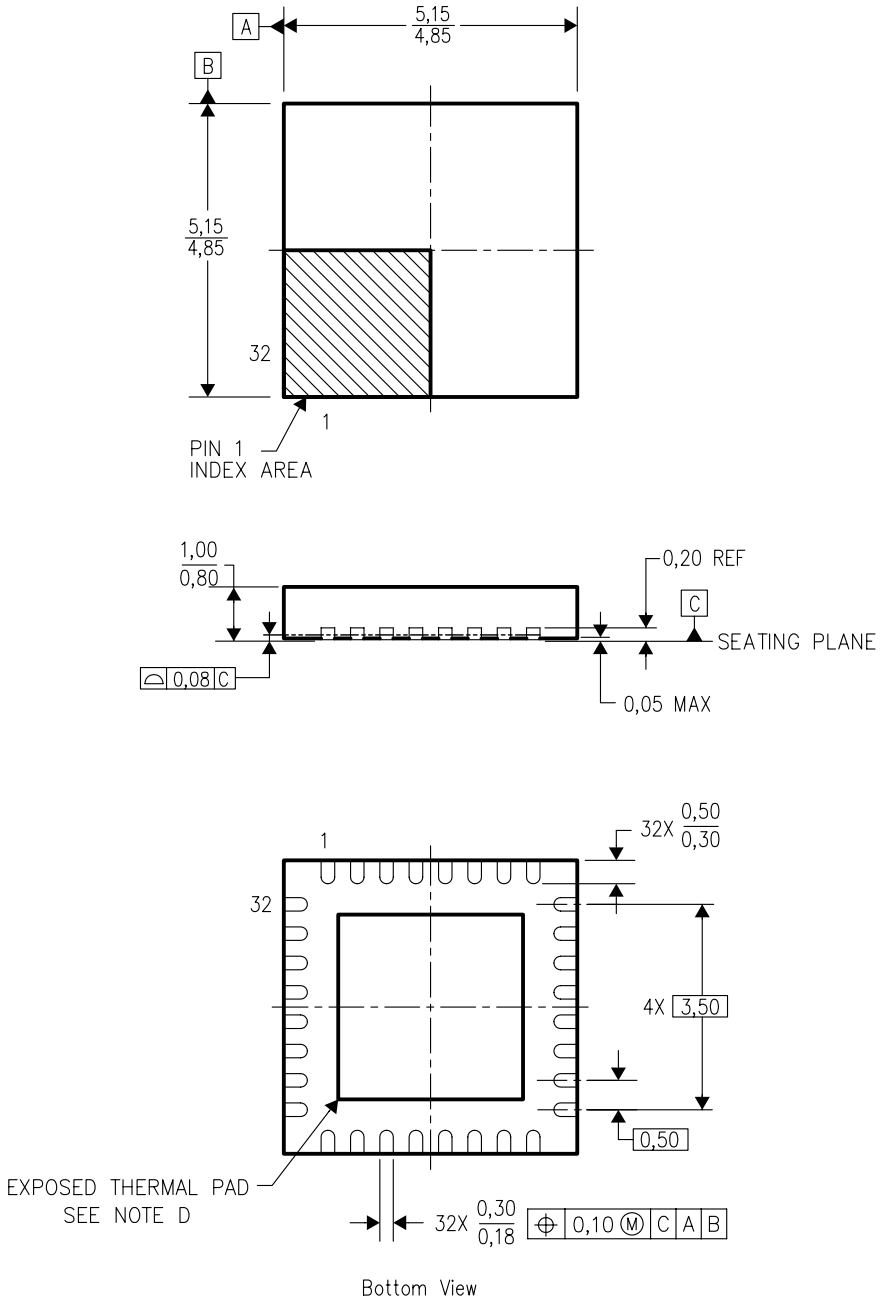
- Bump metal composition: 37% Pb (lead)/63% Sn (tin)
- Type: Spherical

BUMP SPEC.	TYPICAL	TOLERANCE	NOTE
Bump height	100 μm	+8 μm	Tolerance across a single die.
		+16 μm	Tolerance across any wafer.
Re-flow temperature	183°C		

WAFFLE SCALE PACKAGE DISCLAIMERS FOR AIC11YE AND AIC11YER

- The AIC111's die bond pads, their peripheral placement, passivation opening, and layout are in accordance with ASE's *Bumping Design Guide* revision D, June, 2001.
- The final application is assumed to use plastic overmolding where the die is hermetically sealed, and the maximum ratings apply only to the QFN package and not to the WSCP.

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



4204326/C xx/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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