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TWO-CHANNEL, 20-BIT, AC'97 2.3 CODECS WITH HEADPHONE DRIVE, SPDIF OUTPUT MICROPHONE & JACK SENSING STAC9752/9753

Description

IDT's STAC9752/9753 are general purpose 20-bit, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio CODEC 97 Component Specification Rev. 2.3). The STAC9752/9753 incorporate IDT's proprietary $\Sigma\Delta$ technology to achieve a DAC SNR in excess of 90dB. The DACs, ADCs and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9752/9753 include digital output capability for support of modern PC systems with an output that supports the SPDIF format. The STAC9752/9753 are standard 2-channel stereo CODECs. With IDT's headphone capability, headphones can be driven without an external amplifier. The STAC9752/9753 may be used as a secondary or tertiary CODECs, with STAC9700/21/44/56/08/84/50/66 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.3 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications. The STAC9752/9753 communicate via the five AC-Link lines to any digital component of AC'97, providing flexibility in the audio system design. Packaged in an AC'97 compliant 48-pin TQFP, the STAC9752/9753 can be placed on the motherboard, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

Features

- High performance $\Sigma\Delta$ technology
- AC'97 Rev 2.3 compliant
- 20-bit full duplex stereo ADCs, DACs
- Independent sample rates for ADCs & DACs
- 5-wire AC-Link protocol compliance
- 20-bit SPDIF Output
- Internal Jack Sensing on Headphone and Line_Out
- Internal Microphone Input Sensing
- Digital PC Beep Option
- Extended AC'97 2.3 Paging Registers
- Adjustable VREF amplifier
- Digital-ready status
- General purpose I/Os
- Crystal Elimination Circuit
- Headphone drive capability (50 mW)
- 0dB, 10dB, 20dB, and 30dB microphone boost capability
- +3.3 V (STAC9753) and +5 V (STAC9752) analog power supply options
- Pin compatible with the STAC9700, STAC9721, STAC9756
- 100% pin compatible with STAC9750 and STAC9766
- IDT Surround (SS3D) Stereo Enhancement
- Energy saving dynamic power modes
- Multi-CODEC option (Intel AC'97 rev 2.3)
- Six analog line-level inputs
- 90dB SNR Line to Line
- SNR > 89dB through Mixer and DAC

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1. PRODUCT BRIEF

1.1. Description

IDT's STAC9752/9753 are general purpose 20-bit, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio CODEC 97 Component Specification Rev. 2.3). The STAC9752/9753 incorporate IDT's proprietary $\Sigma\Delta$ technology to achieve a DAC SNR in excess of 90dB. The DACs, ADCs and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9752/9753 include digital output capability for support of modern PC systems with an output that supports the SPDIF format. The STAC9752/9753 are standard 2-channel stereo CODECs. With IDT's headphone capability, headphones can be driven without an external amplifier. The STAC9752/9753 may be used as a secondary or tertiary CODECs, with STAC9700/21/44/56/08/84/50/66 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.3 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications. The STAC9752/9753 communicate via the five AC-Link lines to any digital component of AC'97, providing flexibility in the audio system design. Packaged in an AC'97 compliant 48-pin TQFP, the STAC9752/9753 can be placed on the motherboard, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

The STAC9752/9753 block diagram is illustrated in Figure 1. The STAC9752/9753 provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing, and analog processing. Supported audio sample rates include 48 KHz, 44.1 KHz, 32 KHz, 22.05 KHz, 16 KHz, 11.025 KHz, and 8 KHz; additional rates are supported in the STAC9752/9753 soft audio drivers. All ADCs and DACs operate at 20-bit resolution.

Two 20-bit DACs convert the digital stereo PCM_OUT content to audio. The MIXER block combines the PCM_OUT with any analog sources, to drive the LINE_OUT and HP_OUT outputs. The MONO_OUT delivers either microphone only, or a mono mix of sources from the MIXER. The stereo variable-sample-rate 20-bit ADCs provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM-in signal back to the AC-Link. The microphone input and mono mix input can be recorded simultaneously, thus allowing for an all digital output in support of the digital ready initiative. For a digital ready record path, the microphone is connected to the left channel ADC while the mono output of the stereo mixer is connected to right channel ADC.

The STAC9752/9753 include jack sensing on the Headphone and Line_Out. The STAC9752/9753 jack sense can detect the presence of devices on the Headphone and Line Outputs and on both Microphone inputs. With proprietary IDT current and impedance-sensing techniques, the impedance load on the Headphone and Line Outputs can also be detected. The GPIOs on the STAC9752/9753 remain available for advanced configurations.

The STAC9752/9753 implementation of jack sense uses the Extended Paging Registers defined by the AC'97 2.3 Specification. This allows for additional registry space to hold the identification information about the CODEC, the jack sensing details and results, and the external surroundings of the CODEC. The information within the Extended Paging Registers will allow for the automatic configuration of the audio subsystem without end-user intervention. For example, the BIOS can populate the Extended Paging Registers with valuable information for both the audio driver and the operating system such as gain and attenuation stages, input population and input phase. With this input information, the IDT driver will automatically provide to the Volume Control Panel only the volume sliders that are implemented in the system, thus improving the end-user's experience with the PC.

The information in the Extended Paging Registers will also allow for automatic configuration of microphone inputs, the ability to switch between SPDIF and analog outputs, the routing of the mas-

ter volume slider to the proper physical output, and SoftEQ configurations. The fully parametric IDT SoftEQ can be initiated upon jack insertion and sensed impedance levels.

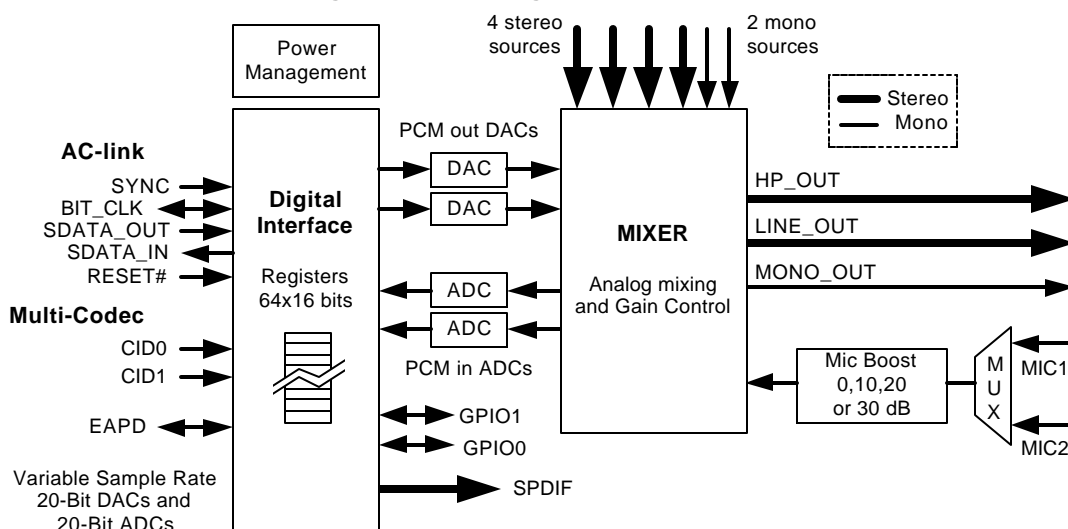
The STAC9752/9753 also offers 2 styles of PC BEEP; Analog and Digital. The digital PC BEEP is a new feature added to the AC'97 Specification Rev 2.3.

The STAC9752/9753 is designed primarily to support stereo (2-speaker) audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-CODEC option available in the STAC9752/9753 to support multiple CODECs in an AC'97 architecture. Additionally, the STAC9752/9753 provides for a stereo enhancement feature, IDT Surround 3D (SS3D). SS3D provides the listener with several options for improved speaker separation beyond the normal two- or four-speaker arrangements.

The STAC9752/9753 can be SoundBlaster® and Windows Sound System® compatible when used with IDT's WDM driver for Windows 98/2K/ME/XP or with Intel/Microsoft driver included with Windows 2K/ME/XP. SoundBlaster is a registered trademark of Creative Labs. Windows is a registered trademark of Microsoft Corporation.

1.2. STAC9752/9753 Block Diagram

Figure 1. Block Diagram



1.3. Key Specifications

- Analog LINE_OUT SNR: 90 dB
- STAC9752 DAC SNR: 89 dB
- STAC9753 DAC SNR: 84dB
- STAC9752 ADC SNR: 90 dB
- STAC9753 ADC SNR: 88 dB
- Crosstalk between Input Channels: -70 dB
- Spurious Tone Rejection: 100 dB

1.4. Related Materials

- Product Brief
- Reference Designs for MB, AMR, CNR, and ACR applications
- Audio Precision Performance Plots

1.5. Additional Support

Additional product and company information can be obtained by going to the IDT web site.

2. CHARACTERISTICS AND SPECIFICATIONS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9752/9753. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Pin | Maximum Rating |
|---------------------------------------|------|--|
| Analog maximum supply voltage | AVdd | 6 Volts |
| Digital maximum supply voltage | DVdd | 5.5 Volts |
| VREFOUT output current | | 5 mA |
| Voltage on any pin relative to ground | | Vss - 0.3 V to Vdd + 0.3 V |
| Operating temperature | | 0°C to +70°C |
| Storage temperature | | -55 °C to +125 °C |
| Soldering temperature | | 260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 90. |

2.1.2. Recommended Operation Conditions

| Parameter | | Min. | Typ. | Max. | Units |
|-------------------------------|-----------------------------|-------|------|-------|-------|
| Power Supply Voltage | Digital - 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | Analog - 5 V | 4.75 | 5 | 5.25 | V |
| | Analog - 3.3 V | 3.135 | 3.3 | 3.465 | V |
| Ambient Operating Temperature | | 0 | | +70 | °C |
| Case Temperature | T _{case} (48-LQFP) | | | +90 | °C |

ESD: The STAC9752/9753 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9752/9753 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.1.3. Power Consumption

| Parameter | Min | Typ | Max | Unit |
|---|------------------------------|-----|-----|------|
| Digital Supply Current | | | | |
| + 3.3V Digital | - | 30 | - | mA |
| Analog Supply Current (at Reset state) | | | | |
| + 5V Analog | - | 35 | - | mA |
| + 3.3V Analog | - | 35 | - | mA |
| Power Down Status (individually asserted) - All PR measurements taken while unmuted. | | | | |
| All paths unmuted | +5V Analog Supply Current | - | 50 | mA |
| | +3.3V Analog Supply Current | - | 44 | |
| | +3.3V Digital Supply Current | - | 33 | |
| PR0 | +5V Analog Supply Current | - | 42 | mA |
| | +3.3V Analog Supply Current | - | 39 | |
| | +3.3V Digital Supply Current | - | 22 | |
| PR1 | +5V Analog Supply Current | - | 41 | mA |
| | +3.3V Analog Supply Current | - | 38 | |
| | +3.3V Digital Supply Current | - | 28 | |
| PR2 | +5V Analog Supply Current | - | 32 | mA |
| | +3.3V Analog Supply Current | - | 29 | |
| | +3.3V Digital Supply Current | - | 12 | |
| PR3 | +5V Analog Supply Current | - | 23 | mA |
| | +3.3V Analog Supply Current | - | 19 | |
| | +3.3V Digital Supply Current | - | 12 | |
| PR4 | +5V Analog Supply Current | - | 50 | mA |
| | +3.3V Analog Supply Current | - | 44 | |
| | +3.3V Digital Supply Current | - | 0.2 | |
| PR5 | +5V Analog Supply Current | - | 50 | mA |
| | +3.3V Analog Supply Current | - | 44 | |
| | +3.3V Digital Supply Current | - | 12 | |
| PR6 | +5V Analog Supply Current | - | 38 | mA |
| | +3.3V Analog Supply Current | - | 36 | |
| | +3.3V Digital Supply Current | - | 33 | |
| PR0 & PR1 | +5V Analog Supply Current | - | 35 | mA |
| | +3.3V Analog Supply Current | - | 35 | |
| | +3.3V Digital Supply Current | - | 12 | |
| PR0, PR1, PR2, PR6 | +5V Analog Supply Current | - | 5 | mA |
| | +3.3V Analog Supply Current | - | 5 | |
| | +3.3V Digital Supply Current | - | 12 | |
| PR0, PR1, PR2, PR3, PR6 | +5V Analog Supply Current | - | 0.6 | mA |
| | +3.3V Analog Supply Current | - | 0.6 | |
| | +3.3V Digital Supply Current | - | 12 | |

2.1.4. AC-Link Static Digital Specifications

($T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$, $DV_{\text{dd}} = 3.3\text{V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{V}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------------|------------------------------|-----|------------------------------|---------------|
| Input voltage range | V_{in} | -0.30 | - | $DV_{\text{dd}} + 0.30$ | V |
| Low level input range | V_{il} | - | - | $0.35 \times DV_{\text{dd}}$ | V |
| High level input voltage | V_{ih} | $0.65 \times DV_{\text{dd}}$ | - | - | V |
| High level output voltage | V_{oh} | $0.90 \times DV_{\text{dd}}$ | - | - | V |
| Low level output voltage | V_{ol} | - | - | $0.1 \times DV_{\text{dd}}$ | V |
| Input leakage current (AC-Link inputs) | - | -10 | - | 10 | μA |
| Output leakage current (Hi-Z AC-Link outputs) | - | -10 | - | 10 | μA |
| BIT_CLK (primary mode) Output leakage current | - | -10 | - | 100 | μA |
| BIT_CLK (secondary mode) Output leakage current | - | -10 | - | 10 | μA |
| Output buffer drive current | - | - | 4 | - | mA |
| BIT_CLK/SPDIF Output drive current | - | - | 18 | - | mA |

Note: Due to an internal pulldown resistor, the BIT_CLK pin will exhibit less than 100 μA of leakage current when the CODEC is configured as primary. This pin meets the +/- 10 μA leakage specification when configured as secondary.

2.1.5. STAC9752 5 V Analog Performance Characteristics

($T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$, $AV_{\text{dd}} = 5.0\text{ V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 V_{rms} , with a 10 $\text{K}\Omega$, 50 pF load, Testbench Characterization BW: 20 Hz to 20 KHz, 0 dB settings on all gain stages)

| Parameter | Min | Typ | Max | Unit |
|---|-----|------|--------|------------------|
| Full Scale Input Voltage: | | | | |
| All Analog Inputs except Microphone | - | 1.00 | - | V_{rms} |
| Microphone Inputs (Note 1) | - | 0.03 | - | V_{rms} |
| Full Scale Output: | | | | |
| Line Output | - | 1.00 | - | V_{rms} |
| PCM (DAC) to LINE_OUT | - | 1.00 | - | V_{rms} |
| MONO_OUT | - | 1.00 | - | V_{rms} |
| HEADPHONE_OUT (32 Ω load) per channel (peak) | - | 50 | - | mW |
| Dynamic Range: -60dB signal level (Note 2) | | | | |
| CD to LINE_OUT | - | 90 | - | dB |
| LINE / AUX / VIDEO to LINE_OUT | - | 90 | - | dB |
| PCM (DAC) to LINE_OUT | 80 | 87 | - | dB |
| PCM (DAC) in BYPASS Mode to LINE_OUT | - | 88 | - | dB |
| LINE_IN to A/D (1 V_{RMS} Input Referenced) | 80 | 90 | - | dB |
| LINE_IN to HEADPHONE_OUT | - | 90 | - | dB |
| Analog Frequency Response (Note 3) | 10 | - | 30,000 | Hz |
| Total Harmonic Distortion + Noise (-3dB): (Note 4) | | | | |
| CD to LINE_OUT | - | -85 | - | dB |
| Other to LINE_OUT | - | -87 | - | dB |
| PCM (DAC) to LINE_OUT (full scale) | - | -83 | - | dB |
| PCM (DAC) in BYPASS Mode to LINE_OUT | - | -86 | - | dB |
| LINE_IN to A/D (-3dBV input Level) | - | -85 | - | dB |

| Parameter | Min | Typ | Max | Unit |
|--|--------|------------|--------|-------------------|
| HEADPHONE_OUT (32 Ω load) | - | -68 | - | dB |
| HEADPHONE_OUT (10 K Ω load) | - | -81 | - | dB |
| SNR (idle channel) (Note 5) | | | | |
| DAC to LINE_OUT | 80 | 90 | - | dB |
| DAC in BYPASS Mode | - | 92 | - | dB |
| LINE / AUX / VIDEO to LINE_OUT | - | 90 | - | dB |
| LINE_IN to A/D with High Pass Filter enabled | - | 92 | - | dB |
| A/D & D/A Digital Filter Pass Band (Note 6) | 20 | - | 19,200 | Hz |
| A/D & D/A Digital Filter Transition Band | 19,200 | - | 28,800 | Hz |
| A/D & D/A Digital Filter Stop Band | 28,800 | - | - | Hz |
| A/D & D/A Digital Filter Stop Band Rejection (Note 7) | -100 | - | - | dB |
| DAC Out-of-Band Rejection (Note 8) | -55 | - | - | dB |
| Group Delay (48 KHz sample rate) | - | - | 1 | ms |
| Power Supply Rejection Ratio (1 KHz) | - | -70 | - | dB |
| Power Supply Rejection Ratio (20 KHz) | - | -40 | - | dB |
| Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency) | - | -80 | - | dB |
| Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency) | - | -100 | - | dB |
| Spurious Tone Rejection | - | -100 | - | dB |
| Attenuation, Gain Step Size | - | 1.5 | - | dB |
| Input Impedance | - | 50 | - | K Ω |
| Input Capacitance | - | 15 | - | pF |
| VREFout | - | 0.5 X AVdd | - | V |
| VREF | - | 0.45X AVdd | - | V |
| Interchannel Gain Mismatch ADC | - | - | 0.5 | dB |
| Interchannel Gain Mismatch DAC | - | - | 0.5 | dB |
| Gain Drift | - | 100 | - | ppm/ $^{\circ}$ C |
| DAC Offset Voltage | - | 10 | 20 | mV |
| Deviation from Linear Phase | - | - | 1 | degrees |
| LINE_OUT / MONO_OUT Load Resistance | 10 | - | - | K Ω |
| LINE_OUT / MONO_OUT Load Capacitance | - | - | 50 | pF |
| HEADPHONE_OUT Load Resistance | - | 32 | - | Ω |
| HEADPHONE_OUT Load Capacitance | - | - | 100 | pF |
| Mute Attenuation | 90 | 96 | - | dB |
| PLL lock time | - | 100 | 200 | μ sec |
| PLL 24.576 MHz clock jitter | - | - | 750 | psec |
| PLL frequency multiplication tolerance | - | - | 12.5 | ppm |
| PLL bit clock jitter | - | - | 750 | psec |

- Note:**
1. With +30dB Boost on, 1.00 Vrms with Boost off.
 2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A-weighted" over a 20 Hz to a 20 KHz bandwidth.
 3. \pm 1dB limits for Line Output & 0 dB gain, at -20dBV
 4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A-weighted" over a 20 Hz to a 20 KHz bandwidth. 48 KHz Sample Frequency
 5. Ratio of Full Scale signal to idle channel noise output is measured "A-weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).

6. Peak-to-Peak Ripple over Passband meets ± 0.25 dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.1.6. STAC9753 3.3V Analog Performance Characteristics

($T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$, $AV_{\text{dd}} = DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}} = DV_{\text{ss}} = 0\text{ V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 Vrms, with a 10 K Ω , 50 pF load, Testbench Characterization BW: 20 Hz to 20 KHz, 0 dB settings on all gain stages)

| Parameter | Min | Typ | Max | Unit |
|---|--------|------|--------|------|
| Full Scale Input Voltage: | | | | |
| All Analog Inputs except Microphone | - | 1.00 | - | Vrms |
| Microphone Inputs (Note 1) | - | 0.03 | - | Vrms |
| Full Scale Output: | | | | |
| Line Output | - | 0.5 | - | Vrms |
| PCM (DAC) to LINE_OUT | - | 0.5 | - | Vrms |
| MONO_OUT | - | 0.5 | - | Vrms |
| HEADPHONE_OUT (32 Ω load) per channel (peak) | - | 12.5 | - | mW |
| Dynamic Range: -60dB signal level (Note 2) | | | | |
| CD to LINE_OUT | - | 85 | - | dB |
| LINE / AUX / VIDEO to LINE_OUT | - | 85 | - | dB |
| PCM (DAC) to LINE_OUT | 75 | 82 | - | dB |
| PCM (DAC) in BYPASS Mode to LINE_OUT | - | 83 | - | dB |
| LINE_IN to A/D | 75 | 85 | - | dB |
| LINE_IN to HEADPHONE_OUT | - | 85 | - | dB |
| Analog Frequency Response (Note 3) | 10 | - | 30,000 | Hz |
| Total Harmonic Distortion + Noise (-3dB): (Note 4) | | | | |
| CD to LINE_OUT | - | -85 | - | dB |
| LINE / AUX / VIDEO to LINE_OUT | - | -85 | - | dB |
| PCM (DAC) to LINE_OUT (full scale) | - | -81 | - | dB |
| PCM (DAC) in BYPASS Mode to LINE_OUT | - | -84 | - | dB |
| LINE_IN to A/D (-3dBV input Level) | - | -85 | - | dB |
| HEADPHONE_OUT (32 Ω load) | - | -68 | - | dB |
| HEADPHONE_OUT (10 k Ω load) | - | -77 | - | dB |
| SNR (idle channel) (Note 5) | | | | |
| DAC to LINE_OUT | 75 | 85 | - | dB |
| DAC in BYPASS Mode | - | 87 | - | dB |
| LINE / AUX / VIDEO to LINE_OUT | - | 86 | - | dB |
| LINE_IN to A/D with High Pass Filter enabled | - | 88 | - | dB |
| A/D & D/A Digital Filter Pass Band (Note 6) | 20 | - | 19,200 | Hz |
| A/D & D/A Digital Filter Transition Band | 19,200 | - | 28,800 | Hz |
| A/D & D/A Digital Filter Stop Band | 28,800 | - | - | Hz |
| A/D & D/A Digital Filter Stop Band Rejection (Note 7) | -100 | - | - | dB |
| DAC Out-of-Band Rejection (Note 8) | -55 | - | - | dB |
| Group Delay (48 KHz sample rate) | - | - | 1 | ms |
| Power Supply Rejection Ratio (1 KHz) | - | -70 | - | dB |

| Parameter | Min | Typ | Max | Unit |
|--|-----|------------|------|-------------------|
| Power Supply Rejection Ratio (20 KHz) | - | -40 | - | dB |
| Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency) | - | -80 | - | dB |
| Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency) | - | -100 | - | dB |
| Spurious Tone Rejection | - | -100 | - | dB |
| Attenuation, Gain Step Size | - | 1.5 | - | dB |
| Input Impedance | - | 50 | - | K Ω |
| Input Capacitance | - | 15 | - | pF |
| VREFout | - | 0.5 X AVdd | - | V |
| VREF | - | 0.41X AVdd | - | V |
| Interchannel Gain Mismatch ADC | - | - | 0.5 | dB |
| Interchannel Gain Mismatch DAC | - | - | 0.5 | dB |
| Gain Drift | - | 100 | - | ppm/ $^{\circ}$ C |
| DAC Offset Voltage | - | 10 | 20 | mV |
| Deviation from Linear Phase | - | - | 1 | degrees |
| LINE_OUT/MONO_OUT Load Resistance | 10 | - | - | K Ω |
| LINE_OUT/MONO_OUT Load Capacitance | - | - | 50 | pF |
| HEADPHONE_OUT Load Resistance | - | 32 | - | Ω |
| HEADPHONE_OUT Load Capacitance | - | - | 100 | pF |
| Mute Attenuation | - | 96 | - | dB |
| PLL lock time | - | 100 | 200 | μ sec |
| PLL 24.576 MHz clock jitter | - | - | 750 | psec |
| PLL frequency multiplication tolerance | - | - | 12.5 | ppm |

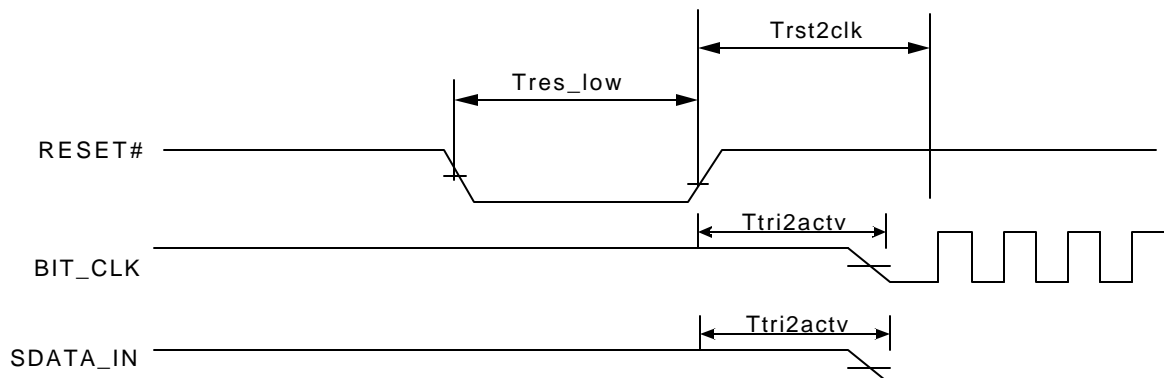
- Note:**
1. With +30 dB Boost on, 1.00 Vrms with Boost off.
 2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A-weighted" over a 20 Hz to a 20 KHz bandwidth.
 3. \pm 1dB limits for Line Output & 0 dB gain, at -20dBV
 4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A-weighted" over a 20 Hz to a 20 KHz bandwidth. 48 KHz Sample Frequency
 5. Ratio of Full Scale signal to idle channel noise output is measured "A-weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
 6. Peak-to-Peak Ripple over Passband meets \pm 0.25dB limits, 48 KHz Sample Frequency.
 7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
 8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.2. AC Timing Characteristics

($T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$, $AV_{\text{dd}} = 3.3\text{ V}$ or $5\text{ V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{ V}$; 75 pF external load for BIT_CLK and 60 pF external load for SDATA_IN)

2.2.1. Cold Reset

Figure 2. Cold Reset Timing

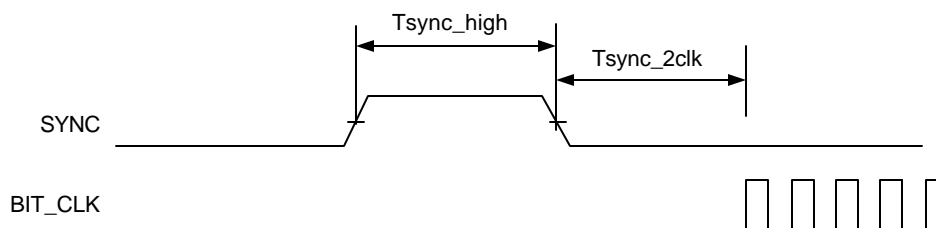


| Parameter | Symbol | Min | Typ | Max | Units |
|--|----------|---------|-----|-----|---------------|
| RESET# active low pulse width | Tres_low | 1.0 | - | - | μs |
| RESET# inactive to SDATA_IN or BIT_CLK active delay | Tri2actv | - | - | 25 | ns |
| RESET# inactive to BIT_CLK startup delay | Trst2clk | 0.01628 | - | 400 | μs |
| BIT_CLK active to RESET# asserted (Not shown in diagram) | Tclk2rst | 0.416 | - | - | μs |

Note: BIT_CLK and SDATA_IN are in a high impedance state during reset.

2.2.2. Warm Reset

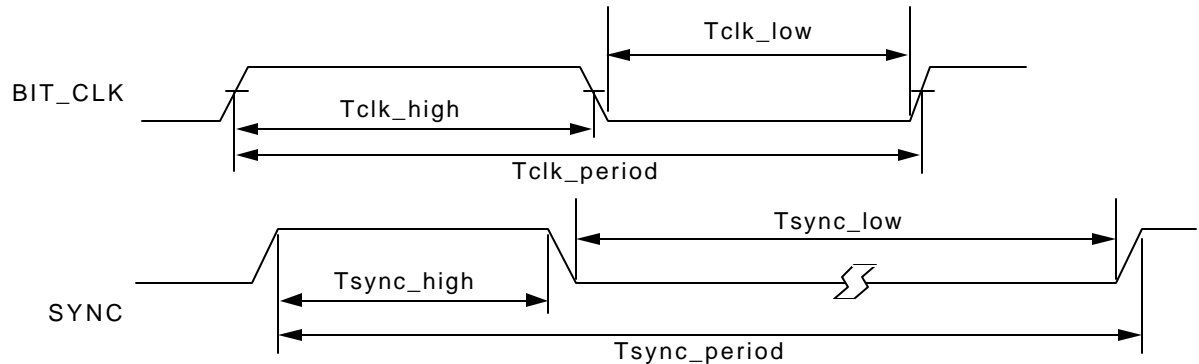
Figure 3. Warm Reset Timing



| Parameter | Symbol | Min | Typ | Max | Units |
|--|------------|-------|-----|-----|---------------|
| SYNC active high pulse width | Tsync_high | 1.0 | 1.3 | - | μs |
| SYNC inactive to BIT_CLK startup delay | Tsync2clk | 162.8 | - | - | ns |

2.2.3. Clocks

Figure 4. Clocks Timing



| Parameter | Symbol | Min | Typ | Max | Units |
|-----------------------------------|--------------|-----|--------|-----|-------|
| BIT_CLK frequency | | - | 12.288 | - | MHz |
| BIT_CLK period | Tclk_period | - | 81.4 | - | ns |
| BIT_CLK output jitter | | - | 750 | - | ps |
| BLT_CLK high pulse width (Note 1) | Tclk_high | 36 | 40.7 | 45 | ns |
| BIT_CLK low pulse width (Note 1) | Tclk_low | 36 | 40.7 | 45 | ns |
| SYNC frequency | | - | 48.0 | - | KHz |
| SYNC period | Tsync_period | - | 20.8 | - | μs |
| SYNC high pulse width | Tsync_high | - | 1.3 | - | μs |
| SYNC low pulse width | Tsync_low | - | 19.5 | - | μs |

Note: 1. Worst case duty cycle restricted to 45/55.

2.2.4. STAC9752/9753 Crystal Elimination Circuit and Clock Frequencies

The STAC9752/9753 supports several clock frequency inputs as described in the following table. In general, when a 24.576 MHz crystal is not used, the XTALOUT pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

CODEC Modes:

P = The STAC9752/9753 as a Primary CODEC.

S = The STAC9752/9753 as a Secondary CODEC.

Table 1. Clock Mode Configuration

| XTL_OUT Pin Config | CID1 Pin Config | CID0 Pin Config | Clock Source Input | CODEC Mode | CODEC ID |
|--------------------|-----------------|-----------------|---------------------|------------|----------|
| XTAL | float | float | 24.576 MHz xtal | P | 0 |
| XTAL or open | float | pulldown | 12.288 MHz bit clk | S | 1 |
| XTAL or open | pulldown | float | 12.288 MHz bit clk | S | 2 |
| XTAL or open | pulldown | pulldown | 12.288 MHz bit clk | S | 3 |
| short to ground | float | float | 14.31818 MHz source | P | 0 |
| short to ground | float | pulldown | 27 MHz source | P | 0 |
| short to ground | pulldown | float | 48 MHz source | P | 0 |
| short to ground | pulldown | pulldown | 24.576 MHz source | P | 0 |

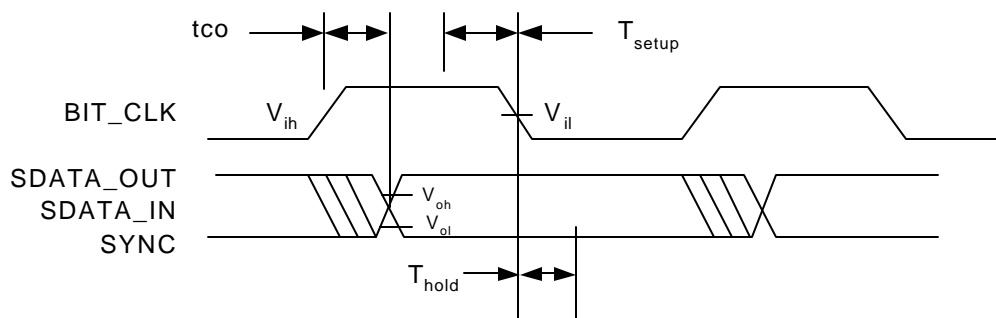
Table 2. Common Clocks and Sources

| Clock Source | Clock Frequency |
|---------------|-----------------|
| XTAL | 24.576 MHz |
| BIT_CLK | 12.288 MHz |
| VGA | 14.31818 MHz |
| Digital Video | 27 MHz |
| USB | 48 MHz |

2.2.5. Data Setup and Hold

(50 pF external load)

Figure 5. Data Setup and Hold Timing



| Parameter | Symbol | Min | Typ | Max | Units |
|---|--------------------|-----|-----|-----|-------|
| Setup to falling edge of BIT_CLK | T_{setup} | 10 | - | - | ns |
| Hold from falling edge of BIT_CLK | T_{hold} | 10 | - | - | ns |
| Output Valid Data from rising edge of BIT_CLK | t_{co} | - | - | 15 | ns |

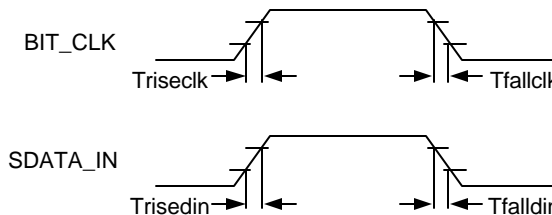
Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

2.2.6. Signal Rise and Fall Times

(BIT_CLK: 75 pF external load; from 10% to 90% of Vdd)

(SDATA_IN: 60 pF external load; from 10% to 90% of Vdd)

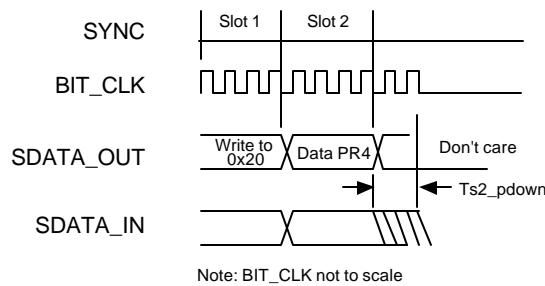
Figure 6. Signal Rise and Fall Times Timing



| Parameter | Symbol | Min | Typ | Max | Units |
|--------------------|----------------------|-----|-----|-----|-------|
| BIT_CLK rise time | T_{riseclk} | - | - | 6 | ns |
| BIT_CLK fall time | T_{fallclk} | - | - | 6 | ns |
| SDATA_IN rise time | T_{risedin} | - | - | 6 | ns |
| SDATA_IN fall time | T_{falldin} | - | - | 6 | ns |

2.2.7. AC-Link Low Power Mode Timing

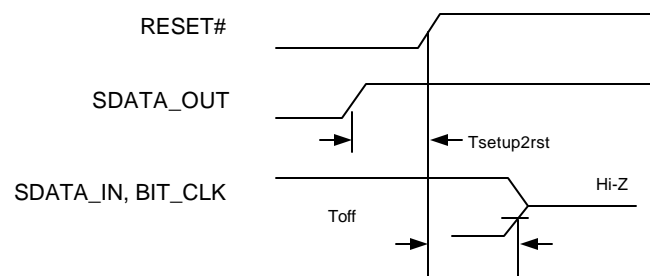
Figure 7. AC-Link Low Power Mode Timing



| Parameter | Symbol | Min | Typ | Max | Units |
|--|-----------|-----|-----|-----|-------|
| End of Slot 2 to BIT_CLK, SDATA_IN low | Ts2_pdown | - | - | 1.0 | μs |

2.2.8. ATE Test Mode

Figure 8. ATE Test Mode Timing

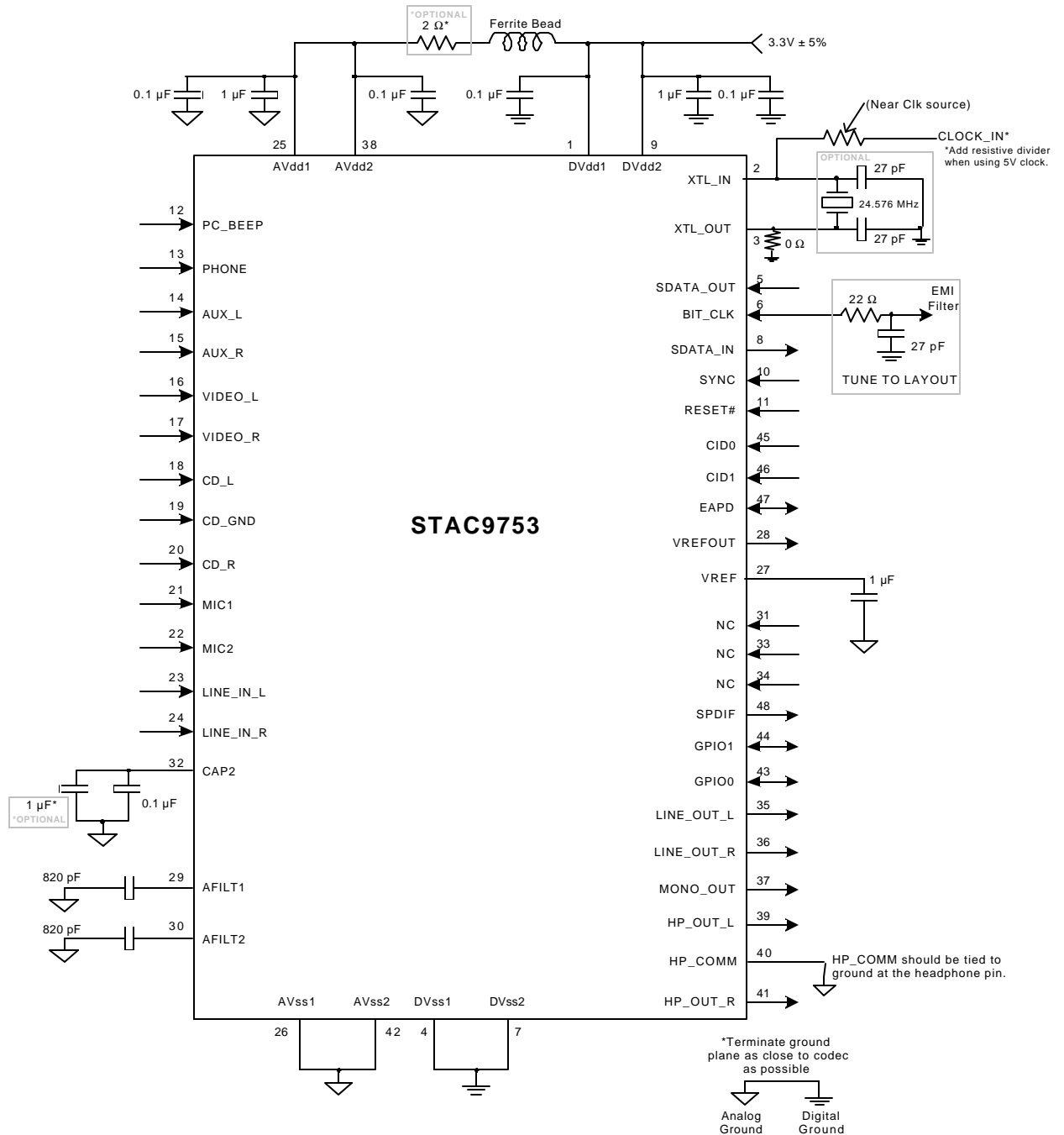


| Parameter | Symbol | Min | Typ | Max | Units |
|---|------------|------|-----|------|-------|
| Setup to trailing edge of RESET# (also applies to SYNC) | Tsetup2rst | 15.0 | - | - | ns |
| Rising edge of RESET# to Hi-Z delay | Toff | - | - | 25.0 | ns |

- Note:**
1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes the STAC9752/9753 AC-Link outputs to go high-impedance which is suitable for ATE in circuit testing.
 2. Once the test mode has been entered, the STAC9752/9753 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.
 3. The pound sign (#) appended to the end of a signal name denotes that the signal is active low.

3. TYPICAL CONNECTION DIAGRAM

Figure 9. Typical Connection Diagram



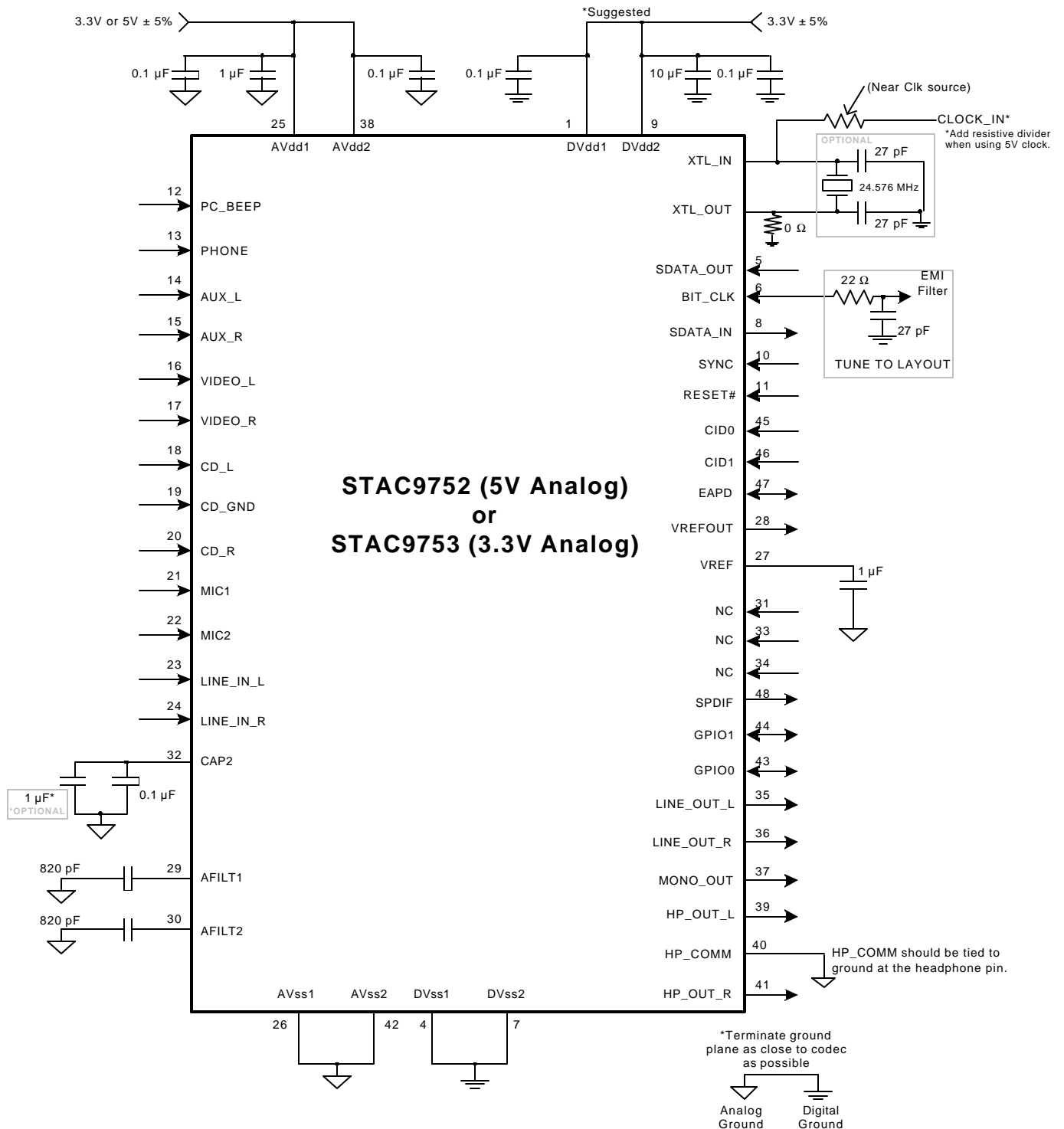
3.1. Split Independent Power Supply Operation

In PC applications, one power supply input to the STAC9752/9753 may be derived from a supply regulator and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's CODECs would be subject to on-chip SCR type latch-up.

IDT's STAC9752/9753 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the CODEC. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

However, the STAC9752/9753 is not designed to operate for extended periods with only the analog supply active.

Figure 10. Split Independent Power Supply Operation



Note: Pin 48: To Enable SPDIF, use an 1 KW to 10 KW external pulldown resistor. To Disable SPDIF, use an 1 KW to 10 KW external pullup resistor. Do NOT leave Pin 48 floating.

4. CONTROLLER, CODEC AND AC-LINK

This section describes the physical and high-level functional aspects of the AC'97 Controller to CODEC interface, referred to as AC-Link.

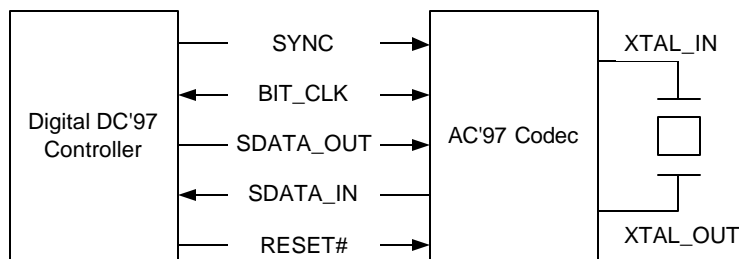
4.1. AC-Link Physical Interface

The STAC9752/9753 communicates with its companion Digital Controller via the AC-Link digital serial interface. AC-Link has been defined to support connections between a single Controller and up to four CODECs. All digital audio, modem and handset data streams, as well as all control (command/status) information are communicated over this serial interconnect, which consists of a clock (BIT_CLK), frame synchronization (SYNC), serial data in (SDATA_IN), serial data out (SDATA_OUT) and a reset (RESET#).

4.2. Controller to Single CODEC

The simplest and most common AC'97 system configuration is a point-to-point AC-Link connection between Controller and the STAC9752/9753, as illustrated in Figure 11.

Figure 11. AC-Link to its Companion Controller

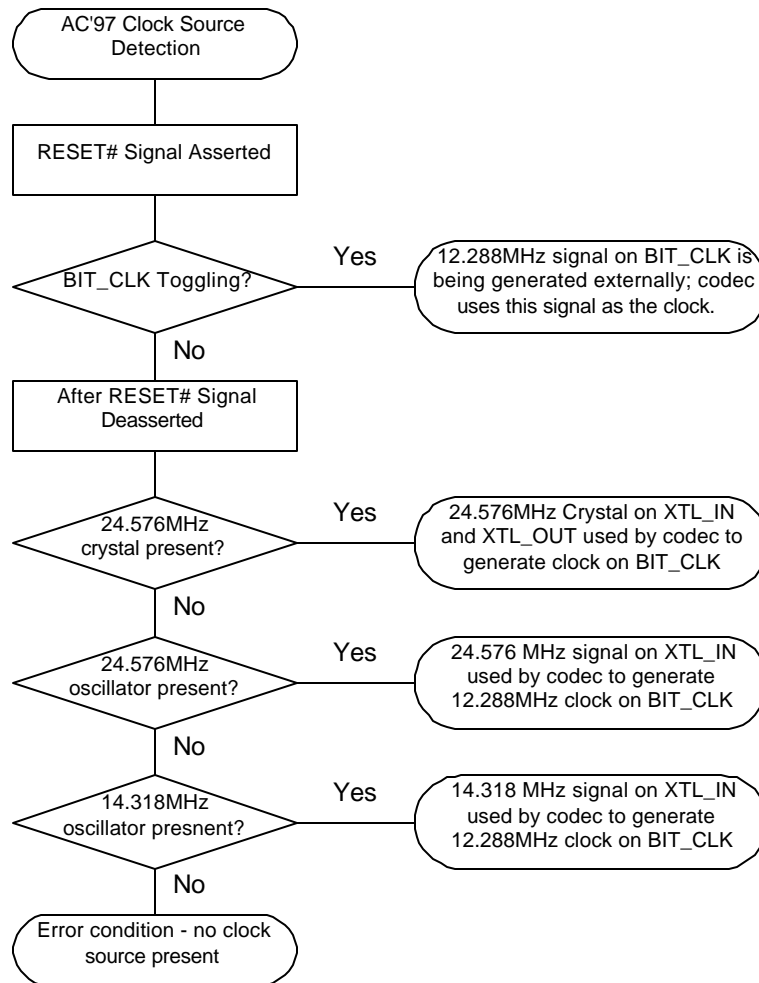


A primary CODEC may act as either a source or a consumer of the bit clock (BIT_CLK), depending on the configuration.

While RESET# is asserted, if a clock is present at the BIT_CLK pin for at least five cycles before RESET# is de-asserted, then the CODEC is a consumer of BIT_CLK, and must not drive BIT_CLK when RESET# is de-asserted. The clock is being provided by other than the primary CODEC, for instance by the controller or an independent clock chip. In this case the primary CODEC must act as a consumer of the BIT_CLK signal as if it were a secondary CODEC.

This clock source detection must be done each time the RESET# line is asserted. In the case of a warm reset, where the clock is halted but RESET# is not asserted, the CODEC must remember the clock source, and not begin generating the clock on the assertion of SYNC, if the CODEC had previously determined that it was a consumer of BIT_CLK.

Figure 12. CODEC Clock Source Detection



The STAC9752/9753 uses the XTAL_OUT Pin (Pin 3) and the CID0 and CID1 pins (Pins 45 & 46) to determine its alternate clock frequencies. See section 2.2.4: page17 for additional information on Crystal Elimination and for supported clock frequencies.

If, when the RESET# signal has been de-asserted, the CODEC has not detected a signal on BIT_CLK as defined in the previous paragraph, then the AC'97 CODEC derives its clock internally from an externally attached 24.576 MHz crystal or oscillator, or optionally from an external 14.31 MHz oscillator, and drives a buffered 12.288 MHz clock to its digital companion Controller over AC-Link under the signal name "BIT_CLK". Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock will provide AC'97 with a clean clock that is independent of the physical proximity of AC'97's companion Digital Controller (henceforth referred to as "the Controller").

If BIT_CLK begins toggling while the RESET# signal is still asserted, the clock is being provided by other than the primary CODEC, for instance by the controller or by a discrete clock source. In this case, the primary CODEC must act as a consumer of the BIT_CLK signal as if it were a secondary CODEC.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-Link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the Controller. The Controller gener-

ates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48 KHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving device on the receiving side of AC-Link on each immediately following falling edge of BIT_CLK.

4.3. Controller to Multiple CODECs

Several vendor specific methods of supporting multiple CODEC configurations on AC-Link have been implemented or proposed, including CODECs with selective AC-Link pass-through and controllers with duplicate AC-Links.

Potential implementations include:

- 6-channel audio using 3 x 2-channel CODECs
- Separate CODECs for independent audio and modem AFE
- Docking stations, where one CODEC is in the laptop and another is in the dock

This specification defines support for up to four CODECs on the AC-Link. By definition there can be one Primary CODEC (ID 00) and up to three Secondary CODECs (IDs 01, 10, and 11). The CODEC ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

Multiple CODEC AC-Link implementations must run off a common BIT_CLK. They can potentially save Controller pins by sharing SYNC, SDATA_OUT, and RESET# from the AC'97 Digital Controller. Each device requires its own SDATA_IN pin back to the Controller. This prevents contention of multiple devices on one serial input line.

Support for multiple CODEC operation necessitates a specially designed Controller. An AC'97 Digital Controller that supports multiple CODEC configurations implements multiple SDATA_IN inputs, supporting one Primary CODEC and up to three Secondary CODECs.

4.3.1. Primary CODEC Addressing

Primary AC'97 CODECs respond to register read and write commands directed to CODEC ID 00 (see Section 10 for details of the Primary and Secondary CODEC addressing protocols). Primary devices must be configurable (by hardwiring, strap pin(s), or other methods) as CODEC ID 00, and reflect this in the two-bit CODEC ID field(s) of the Extended Audio and/or Extended Modem ID Register(s).

The Primary CODEC may either drive the BIT_CLK signal or consume a BIT_CLK signal provided by the digital controller or other clock generator.

4.3.2. Secondary CODEC Addressing

Secondary AC'97 CODECs respond to register read and write commands directed to CODEC IDs 01, 10, or 11. Secondary devices must be configurable (via hardwiring, strap pin(s), or other methods) as CODEC IDs 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

CODECs configured as Secondary must power up with the BIT_CLK pin configured as an input. Using the provided BIT_CLK signal is necessary to ensure that everything on the AC-Link is synchronous. BIT_CLK is the clock source (multiplied by 2 so that the internal rate is 24.576 MHz).

4.3.3. CODEC ID Strapping

Audio CODECs in the 48-pin package use pins 45 and 46 (defined as ID0# and ID1#) as strapping (i.e. configuration) pins to configure the CODEC ID. The ID0# and ID1# strapping bits adopt inverted polarity and default to 00 = Primary (via a weak internal pullup) when left floating. This eliminates the need for external resistors for CODECs configured as Primary, and maintains backward compatibility with existing layouts that treat pins 45 and 46 as “no connect” or cap to ground. Pulldowns are typically 0-10 k Ω and connected to Digital (not Analog) Ground.

Table 3. Recommended CODEC ID strapping

| CID1 (pin 46) | CID0 (pin 45) | Configuration |
|---------------|---------------|-------------------|
| NC | NC | Primary ID = 00 |
| NC | pulldown | Secondary ID = 01 |
| pulldown | NC | Secondary ID = 10 |
| pulldown | pulldown | Secondary ID = 11 |

4.4. Clocking for Multiple CODEC Implementations

To keep the system synchronous, all Primary and Secondary CODEC clocking must be derived from the same clock source, so all CODECs are operating on the same time base. In addition, all AC-Link protocol timing must be based on the BIT_CLK signal, to ensure that everything on the AC-Link will be synchronous.

The following are potential 24.576 MHz clock options available to a Secondary CODEC:

- Using an external 24.576 MHz signal source (external oscillator or AC'97 Digital Controller).
- Using the Primary's XTAL_OUT.
- Using the Primary's BIT_CLK output to derive 24.576 MHz.

See section 2.2.4: page17 for supported clock frequencies and configurations.

4.5. STAC9752/9753 as a Primary CODEC

Primary devices are required to support correctly any of the following clocking options:

- 24.576 MHz crystal attached to XTAL_IN and XTAL_OUT.
- 24.576 MHz external oscillator provided to XTAL_IN.
- 12.288 MHz oscillator provided to the BIT_CLK input.

The Primary device may also, optionally, support the following clocking option:

- 14.318 MHz external oscillator provided to XTAL_IN.

See section 2.2.4: page17 for supported clock frequencies and configurations.

4.5.1. STAC9752/9753 as a Secondary CODEC

Secondary devices are required to function correctly using one or more of the following clocking options:

- 24.576 MHz external oscillator provided to XTAL_IN (synchronous and in phase with Primary 24.576 MHz clock).
- BIT_CLK input provided by the Primary. In this mode, a clock at XTAL_IN (Pin 2) is ignored.

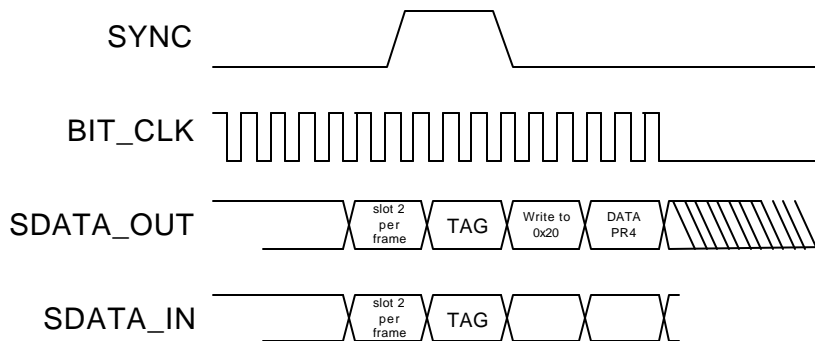
See section 2.2.4: page17 for supported clock frequencies and configurations.

4.6. AC-Link Power Management

4.6.1. Powering down the AC-Link

The AC-Link signals can be placed in a low power mode. When the AC'97's Powerdown Register (26h) is programmed to the appropriate value, both BIT_CLK and SDATA_IN are brought to and held at a logic low voltage level. After signaling a reset to AC'97, the AC'97 Controller should not attempt to play or capture audio data until it has sampled a CODEC Ready indication from AC'97.

Figure 13. STAC9752/9753 Powerdown Timing



Note: BIT_CLK not to scale

BIT_CLK and SDATA_IN are transitioned low immediately following decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 Controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame.

After programming the AC'97 device to this low power, halted mode, the AC'97 Controller is required to drive and keep SYNC and SDATA_OUT low.

Once the AC'97 CODEC has been instructed to halt BIT_CLK, a special "wake-up" protocol must be used to bring the AC-Link to the active mode since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

4.6.2. Waking up the AC-Link

There are two methods for bringing the AC-Link out of a low power, halted mode. Regardless of the method, it is the AC'97 Controller that performs the wake-up task.

4.6.2.1. Controller Initiates Wake-up

The AC-Link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current powerdown state ultimately dictates which form of AC'97 reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset Register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all powerdown modes.

Once powered down, re-activation of the AC-Link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the powerdown was triggered. When AC-Link powers up, the CODEC indicates readiness via the CODEC Ready bit (input slot 0, bit 15).

4.6.2.2. CODEC Initiates Wake-up

The STAC9752/9753 (running off Vaux) can trigger a wake event (PME#) by transitioning SDATA_IN from low to high and holding it high until either a warm or cold reset is observed on the AC-Link. This functionality is typically implemented in modem CODECs that detect ring, Caller ID, etc.

Note that when the AC-Link is either programmed to the low power mode or shut off completely, BIT_CLK may stop if the primary CODEC is supplying the clock, which shuts down the AC-Link clock to the Secondary CODEC¹. In order for a Secondary CODEC to react to an external event (phone ringing), it must support an independent clocking scheme for any PME# associated logic that must be kept alive when the AC-Link is down. This includes logic to asynchronously drive SDATA_IN to a logic high-level which signals a wake request to the AC'97 Digital Controller.

4.6.3. CODEC Reset

There are three types of AC'97 reset:

- a *cold* reset where all AC'97 logic (most registers included) is initialized to its default state
- a *warm* reset where the contents of the AC'97 register set are left unaltered
- a *register* reset which only initializes the AC'97 registers to their default states

4.6.3.1. Cold AC'97 Reset

A cold reset is achieved by asserting RESET# (low) for the minimum specified time, then subsequently de-asserting RESET# (high). BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all AC'97 control registers will be initialized to their default power on reset values.

RESET# is an asynchronous AC'97 input.

4.6.3.2. Warm AC'97 Reset

A warm AC'97 reset will re-activate the AC-Link without altering the current AC'97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 μ s in the absence of BIT_CLK.

Within normal audio frames, SYNC is a synchronous AC'97 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to AC'97.

AC'97 MUST NOT respond with the activation of BIT_CLK until SYNC has been sampled low again by AC'97. This will preclude the false detection of a new audio frame.

4.6.3.3. Register AC'97 Reset

Most registers in an AC device can be restored to their default values by performing a write (any value) to the Reset Register, 00h.

1. Secondary CODECs always configure the BIT_CLK pin as an input.

5. AC-LINK DIGITAL INTERFACE

5.1. Overview

AC-Link is the 5 pin digital serial interface that links the AC'97 CODEC to the Controller. The AC-Link protocol is a bi-directional, fixed clock rate, serial digital stream. AC-Link handles multiple input and output PCM audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme that divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

The STAC9752/9753 DACs, ADCs, and SPDIF can be assigned to slots 3&4, 6&9, 7&8 or 10&11.

Figure 14. Bi-directional AC-Link Frame with Slot assignments

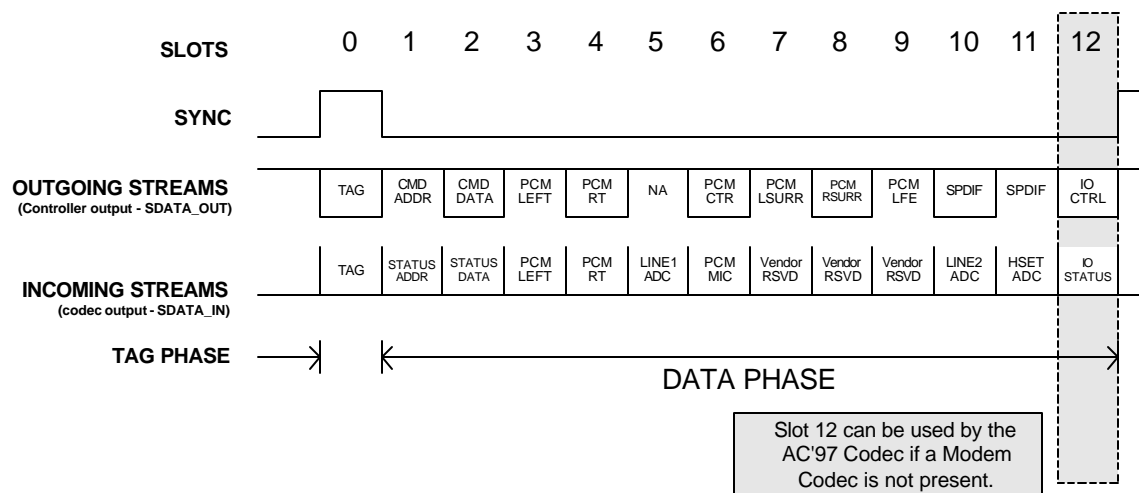


Table 4. AC-Link output slots (transmitted from the Controller)

| Slot | Name | Description |
|------------|-------------------------------|---|
| 0 | SDATA_OUT TAG | MSBs indicate which slots contain valid data; LSBs convey CODEC ID |
| 1 | Control CMD ADDR write port | Read/write command bit plus 7-bit CODEC register address |
| 2 | Control DATA write port | 16-bit command register write data |
| 3, 4 | PCM L&R DAC playback | 20-bit PCM data for Left and Right channels |
| 5 | Modem Line 1 DAC | 16-bit modem data for modem Line 1 output |
| 6, 7, 8, 9 | PCM Center, Surround L&R, LFE | 20-bit PCM data for Center, Surround L&R, LFE channels |
| 10 | Modem Line 2 DAC | 16-bit modem data for modem Line 2 output |
| 11 | Modem handset DAC | 16-bit modem data for modem Handset output |
| 12 | Modem I/O control | GPIO write port for modem Control |
| 12 | CODEC IRQ | Can be used by CODEC if a modem CODEC is not present. |
| 10-11 | SPDIF Out | Optional AC-Link bandwidth for SPDIF output |
| 10-12 | Double rate audio | Optional AC-Link bandwidth for 88.2 KHz or 96 KHz on L, C, R channels |

Table 5. The AC-Link input slots (transmitted from the CODEC)

| Slot | Name | Description |
|------|-----------------------|--|
| 0 | SDATA_IN TAG | MSBs indicate which slots contain valid data |
| 1 | STATUS ADDR read port | MSBs echo register address; LSBs indicate which slots request data |
| 2 | STATUS DATA read port | 16-bit command register read data |
| 3, 4 | PCM L&R ADC record | 20-bit PCM data from Left and Right inputs |
| 5 | Modem Line 1 ADC | 16-bit modem data from modem Line1 input |
| 6-11 | PCM ADC Record | 20-bit PCM data - Alternative Slots for Input |
| 12 | GPIO Status | GPIO read port and interrupt status |

5.2. AC-Link Serial Interface Protocol

The AC'97 Controller signals synchronization of all AC-Link data transactions. The AC'97 CODEC, Controller, or external clock source drives the serial bit clock (BIT_CLK) onto AC-Link, which the AC'97 Controller then qualifies with a synchronization signal (SYNC) to construct audio frames. SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-Link data (CODEC for outgoing data and Controller for incoming data) samples each serial bit on the falling edges of BIT_CLK.

The AC-Link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data (AC'97 CODEC for the input stream, AC'97 Controller for the output stream), to stuff all bit positions with 0 during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that an AC'97 CODEC be implemented as a static design to allow its register contents to remain intact when entering a power savings mode.

5.2.1. AC-Link Variable Sample Rate Operation

The AC-Link serial interconnect defines a digital data and control pipe between the Controller and the CODEC. The AC-Link supports 12 20-bit slots at 48 KHz on SDATA_IN and SDATA_OUT. The time division multiplexed (TDM) "slot-based" architecture supports a per-slot valid tag infrastructure that the source of each slot's data sets or clears to indicate the validity of the slot data within the current audio frame. This tag infrastructure can be used to support transfers between Controller and CODEC at any sample rate.

5.2.2. Variable Sample Rate Signaling Protocol

AC-Link's tag infrastructure imposes FIFO requirements on both sides of the AC-Link. For example, in passing a 44.1 KHz stream across the AC-Link, for every 480 audio output frames that are sent across, 441 of them must contain valid sample data. Does the AC'97 Digital Controller pass all 441 PCM samples followed by 39 invalid slots? Or does the AC'97 Digital Controller evenly interleave

valid and non-valid slots? Each possible method brings with it different FIFO requirements. To achieve interoperability between AC'97 Digital Controllers and CODECs designed by different manufacturers, it is necessary to standardize the scheme for at least one side of the AC-Link so that the FIFO requirements will be common to all designs. The CODEC side of the AC-Link is the focus of this standardization.

The new standard approach calls for the addition of “on demand” slot request flags. These flags are passed from the CODEC to the AC'97 Digital Controller during every audio input frame. Each time the AC'97 Digital Controller sees one or more of the newly-defined slot request flags set active (low) in a given audio input frame, it knows that it must pass along the next PCM sample for the corresponding slot(s) in the AC-Link output frame that immediately follows.

The VRA (Variable Rate Audio) bit in the Extended Audio Status and Control Register must be set to 1 to enable variable sample rate audio operation. Setting the VRA = 1 has two functions:

1. Enables PCM DAC/ADC conversions at variable sample rates by write enabling Sample Rate Registers 2Ch through 34h.
2. Enables the on demand CODEC-to-Controller signaling protocol using SLOTREQ bits that becomes necessary when a DAC's sample rate varies from the 48 KHz AC-Link serial frame rate.

The table below summarizes the behavior:

Table 6. VRA Behavior

| AC'97 Functionality | VRA = 0 | VRA = 1 |
|-----------------------|----------------------------|-------------------------|
| SLOTREQ bits | always 0 (data each frame) | 0 or 1 (data on demand) |
| sample rate registers | forced to 48KHz | writable |

Note: If more than one CODEC is being used with the SAME controller DMA engine, VRA should NOT be used.

For variable sample rate output, the CODEC examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each AC-Link output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current AC-Link input frame signal which *active output slots* require data from the AC'97 Digital Controller in the next audio output frame. An *active output slot* is defined as any slot supported by the CODEC that is not in a power-down state. For fixed 48KHz operation the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the CODEC is always the master: for SDATA_IN (CODEC to Controller), the CODEC sets the TAG bit; for SDATA_OUT (Controller to CODEC), the CODEC sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

The VRM (Variable Rate Microphone Audio) bit in the Extended Audio Status and Control Register controls the optional MIC ADC input behavior in the same way that VRA = 1 controls the PCM ADC.

5.2.2.1. SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots should be driven low (zero) for maximum compatibility with the original AC'97 Component Specification. When a DAC channel is powered down, it disappears completely from the serial frame: output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero).

When the Controller wants to power-down a channel, all it needs to do is:

1. Disable source of DAC samples in Controller
2. Set PR bit for DAC channel in Registers 26h, 2Ah, or 3Eh

When it wants to power up the channel, all it needs to do is:

1. Clear PR bit for DAC channel in Registers 26h, 2Ah, or 3Eh
2. Enable source of DAC samples in Controller

5.2.3. **Primary and Secondary CODEC Register Addressing**

The 2-bit CODEC ID field in the LSBs of Output Slot 0 is an addition to the original AC-Link protocol that enables an AC'97 Digital Controller to independently access Primary and Secondary CODEC registers.

For Primary CODEC access, the AC'97 Digital Controller:

1. Sets the AC-Link Frame valid bit (Slot 0, bit 15)
2. *Validates* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13)
3. Sets a *zero* value (00) into the CODEC ID field (Slot 0, bits 1 and 0)
4. Transmits the desired Primary CODEC Command Address and Command Data in Slots 1 and 2

For Secondary CODEC access, the AC'97 Digital Controller:

1. Sets the AC-Link Frame valid bit (Slot 0, bit 15)
2. Places a *non-zero* value (01, 10, or 11) into the CODEC ID field (Slot 0, bits 1 and 0)
3. Transmits the desired Secondary CODEC Command Address and Command Data in Slots 1 and 2

Secondary CODECs disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits. In a sense the Secondary CODEC ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

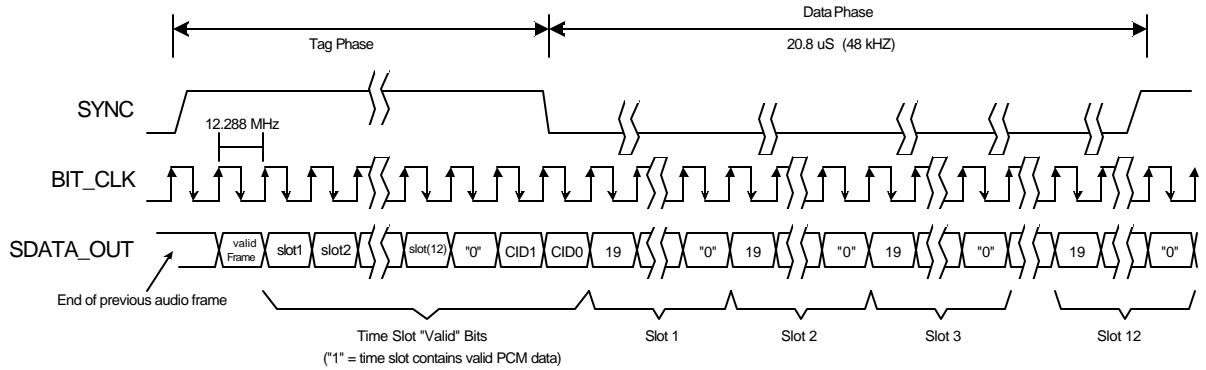
Secondary CODECs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary CODEC ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a Secondary register access, even if no other bits in the output tag slot except the Secondary CODEC ID bits are set.

5.3. AC-Link Output Frame (SDATA_OUT)

The AC-Link output frame data streams correspond to the multiplexed bundles of all digital output data targeting AC'97's DAC inputs and control registers. As mentioned earlier, each AC-Link output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-Link protocol infrastructure.

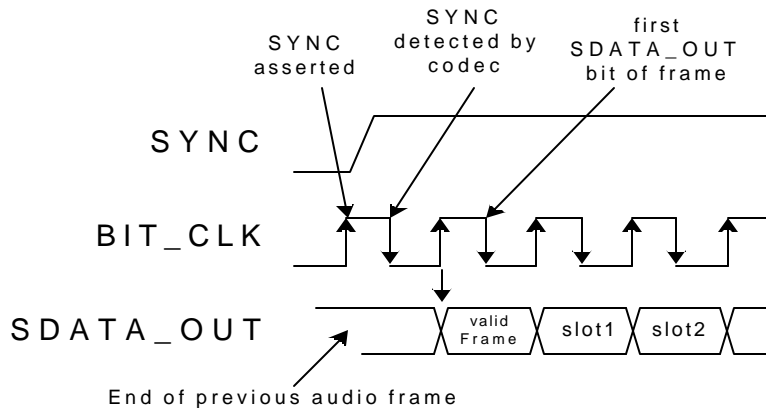
Figure 15 illustrates the time slot based AC-Link protocol.

Figure 15. AC-Link Audio Output Frame



A new AC-Link output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC'97 CODEC samples the assertion of SYNC. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC'97 Controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and subsequently sampled by the AC'97 CODEC on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 16. Start of an Audio Output Frame



SDATA_OUT's composite stream is sent MSB first, with all non-valid slots bit positions stuffed with 0 by the AC'97 Controller. If there are less than 20 valid bits within an assigned and valid time slot, the AC'97 Controller always stuffs the trailing non-valid bit positions of the 20-bit slot with 0.

As an example, consider an 8-bit sample stream that is being played out to one of the STAC9752/9753 DACs. The first 8 bit-positions are presented to the DAC (MSB first) followed by the next 12 bit-positions which are stuffed with 0 by the AC'97 Controller. This ensures that regardless of the resolution of the implemented DAC (16, 18 or 20-bit), no DC biasing will be introduced by the least significant bits.

When mono audio sample streams are output from the AC'97 Controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

5.3.1. Slot 0: TAG / CODEC ID

Table 7. Output Slot 0 Bit Definitions

| Bit | Description |
|-----|---|
| 15 | Frame Valid |
| 14 | Slot 1 Primary CODEC Valid Command Address bit (Primary CODEC only) |
| 13 | Slot 2 Primary CODEC Valid Command Data bit (Primary CODEC only) |
| | <i>Slot 3-12 Valid Data bits</i> |
| 12 | Slot 3: PCM Left channel |
| 11 | Slot 4: PCM Right channel |
| 10 | Slot 5: Modem Line 1 (not used on STAC9752/9753) |
| 9 | Slot 6: Alternative PCM1 Left |
| 8 | Slot 7: Alternative PCM2 Left |
| 7 | Slot 8: Alternative PCM2 Right |
| 6 | Slot 9: Alternative PCM1 Right |
| 5 | Slot 10: SPDIF Left |
| 4 | Slot 11: SPDIF Right |
| 3 | Slot 12: Audio GPIO |
| 2 | Reserved (Set to 0) |
| 1-0 | 2-bit CODEC ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary) |

Note: The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one time slot of valid data. The next 12 bit positions sampled by AC'97 indicate which of the corresponding 12 time slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-Link at its fixed 48 KHz audio frame rate.

The two LSBs of Slot 0 transmit the CODEC ID used to distinguish Primary and Secondary CODEC register access.

5.3.2. Slot 1: Command Address Port

The command port is used to control features and monitor status (see AC-Link input frame Slots 1 and 2) for AC'97 CODEC functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are currently defined, odd register (01h, 03h, etc.) accesses are reserved for future expansion.

Note that shadowing of the control register file on the AC'97 Controller is an option left open to the implementation of the AC'97 Controller. The AC'97 CODEC's control register file is nonetheless required to be readable as well as writeable to provide more robust testability.

AC-Link output frame slot 1 communicates control register address, and write/read command information to the STAC9752/9753.

Table 8. Command Address Port Bit Assignments

| Bit | Description | Comments |
|-------|------------------------|--|
| 19 | Read/Write command | 1= read, 0 = write |
| 18:12 | Control Register Index | Sixty-four 16-bit locations, addressed on even byte boundaries |
| 11:0 | Reserved | Stuffed with 0 |

The first bit (MSB) sampled by AC'97 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be stuffed with 0 by the AC'97 Controller.

5.3.3. Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19).

- Bit(19:4) Control Register Write Data (Stuffed with 0 if current operation is a read)
- Bit(3:0) Reserved (Stuffed with 0)

If the current command port operation is a read then the entire slot time must be stuffed with 0 by the AC'97 Controller.

5.3.4. Slot 3: PCM Playback Left Channel

AC-Link output frame slot 3 is the composite digital audio left playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 Controller must stuff all trailing non-valid bit positions within this time slot with 0.

The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.3.5. Slot 4: PCM Playback Right Channel

AC-Link output frame slot 4 is the composite digital audio right playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 Controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 Controller must stuff all trailing non-valid bit positions within this time slot with 0.

The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.3.6. Slot 5: Modem Line 1 Output Channel

Audio output frame slot 5 is reserved for modem operation and is not used by the STAC9752/9753.

5.3.7. Slot 6 - 11: DAC

The DAC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.3.8. Slot 12: Audio GPIO Control Channel

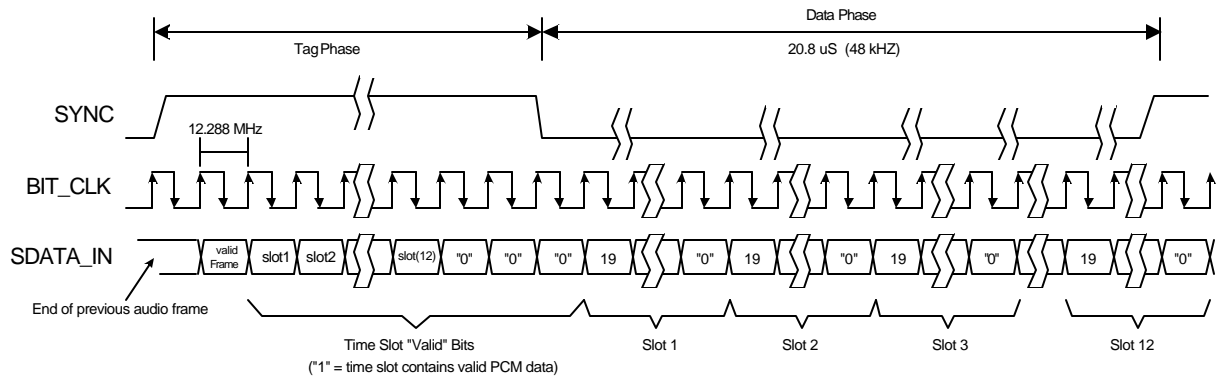
AC-Link output frame slot 12 contains the audio GPIO control outputs.

5.4. AC-Link Input Frame (SDATA_IN)

The AC-Link input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 Controller. As is the case for audio output frame, each AC-Link input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-Link protocol infrastructure.

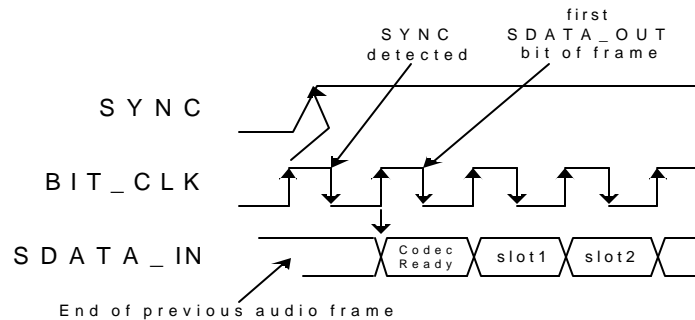
The following diagram illustrates the time slot-based AC-Link protocol.

Figure 17. STAC9752/9753 Audio Input Frame



A new AC-Link input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the AC'97 CODEC samples the assertion of SYNC. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC'97 CODEC transitions SDATA_IN into the first bit position of slot 0 ("CODEC Ready" bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and subsequently sampled by the AC'97 Controller on the falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 18. Start of an Audio Input Frame



SDATA_IN's composite stream is MSB first with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0 by the AC'97 CODEC. SDATA_IN data is sampled on the falling edges of BIT_CLK.

5.4.1. Slot 0: TAG

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the AC'97 CODEC is in the "CODEC Ready" state or not. If the "CODEC Ready" bit is a 0, this indicates that the AC'97 CODEC is not ready for normal operation. This condition is normal following the deassertion of power-on-reset for example, while the AC'97 CODEC's voltage references settle. When the AC-Link "CODEC Ready" indicator bit is a 1, it indicates that the AC-Link and AC'97 CODEC control and status registers are in a fully operational state. The CODEC must assert "CODEC Ready" within 400 μ s after it starts receiving valid SYNC pulses from the controller, to provide indication of connection to the link and Control/Status registers are available for access. The AC'97 Controller and related software **must wait** until all of the lower four bits of the Control/Status Register, 26h, are set before attempting any register writes, or attempting to enable any audio stream, to avoid undesirable audio artifacts.

Prior to any attempts at putting an AC'97 CODEC into operation, the AC'97 Controller should poll the first bit in the AC-Link input frame (SDATA_IN slot 0, bit 15) for an indication that CODEC has gone "CODEC Ready". Once an AC'97 CODEC is sampled "CODEC Ready"¹, then the next 12 bit positions sampled by the AC'97 Controller indicate which of the corresponding 12 time slots are assigned to input data streams, and whether they contain valid data.

5.4.2. Slot 1: Status Address Port / SLOTREQ signalling bits

5.4.2.1. Status Address Port

The status port is used to monitor status for the STAC9752/9753 functions including, but not limited to, mixer settings and power management. AC-Link input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2 (assuming that slots 1 and 2 had been tagged "valid" by the AC'97 CODEC during slot 0).

Table 9. Status Address Port Bit Assignments

| Bit | Description | Comments |
|-------|------------------------|---|
| 19 | Reserved | Stuffed with 0 |
| 18:12 | Control Register Index | Echo of register index for which data is being returned |
| 11:2 | SLOTREQ | See Next Section |
| 1:0 | Reserved | Stuffed with 0 |

The first bit (MSB) generated by AC'97 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, the next 10 bits support AC'97's variable sample rate signaling protocol, and the trailing 2 bit positions are stuffed with 0 by AC'97.

5.4.2.2. SLOTREQ signaling bits

AC-Link input frame Slot #1, the Status Address Port, now delivers CODEC control register read address *and* variable sample rate slot request flags for all output slots. Ten of the formerly reserved least significant bits have been defined as data request flags for output slots 3-12.

-
1. There are several subsections within an AC'97 CODEC that can independently go busy/ready. It is the responsibility of the AC'97 Controller to probe more deeply into the AC'97 CODEC's register file to determine which subsections are actually ready.

The AC-Link input frame Slot 1 tag bit is independent of the bit 11-2 slot request field, and ONLY indicates valid Status Address Port data (Control Register Index). The CODEC should only set SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to 1 when returning valid data from a previous register read. They should otherwise be set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ bits are always 0 in the following cases:

- fixed rate mode (VRA = 0)
- inactive (powered down) ADC channel

SLOTREQ bits are only set to 1 by the CODEC in the following case:

- Variable rate audio mode (VRA = 1) AND active (power ready) ADC AND a non-48 KHz ADC sample rate AND CODEC does not need a sample

5.4.3. Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Table 10. Status Data Port Bit Assignments

| Bit | Description | Comments |
|------|----------------------------|------------------------------------|
| 19:4 | Control Register Read Data | Stuffed with 0 if tagged "invalid" |
| 3:0 | Reserved | Stuffed with 0 |

If Slot 2 is tagged invalid by AC'97, then the entire slot will be stuffed with 0 by AC'97.

5.4.4. Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of STAC9752/9753 input MUX, post-ADC. STAC9752/9753 ADCs are implemented to support 20-bit resolution.

NOTE: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.4.5. Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of STAC9752/9753 input MUX, post-ADC. STAC9752/9753 ADCs are implemented to support 20-bit resolution.

NOTE: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.4.6. Slot 5: Modem Line 1 ADC

Audio input frame slot 5 is not used by the STAC9752/9753 and is always stuffed with 0.

5.4.7. Slot 6 - 9: ADC

The left and right ADC channels of the STAC9752/9753 may be assigned to slots 6&9 by Register 6Eh.

NOTE: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.4.8. Slots 7 & 8: Vendor Reserved

The left and right ADC channels of the STAC9752/9753 may be assigned to slots 7&8 by Register 6Eh.

NOTE: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.4.9. Slot 10 & 11: ADC

The left and right ADC channels of the STAC9752/9753 may be assigned to slots 10&11 by Register 6Eh.

NOTE: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

5.4.10. Slot 12: Reserved

AC-Link input frame slot 12 contains the GPIO status inputs and allows for audio interrupts. Slot 12 can not be used by the AC'97 CODEC because a modem CODEC is not present.

5.5. AC-Link Interoperability Requirements and Recommendations

5.5.1. “Atomic slot” Treatment of Slot 1 Address and Slot 2 Data

Command or Status Address and Data cannot be split across multiple AC-Link frames. The following transactions require that valid Slot 1 Address and valid Slot 2 Data be treated as “atomic” (inseparable) with Slot 0 Tag bits for Address and Data set accordingly (that is, both valid):

1. AC'97 Digital Controller write commands to Primary CODECs
2. AC'97 CODEC status responses

Whenever the AC'97 Digital Controller addresses a Primary CODEC or an AC'97 CODEC responds to a read command, Slot 0 Tag bits should always be set to indicate actual Slot 1 and Slot 2 data validity.

Table 11. Primary CODEC Addressing: Slot 0 Tag Bits

| Function | Slot 0, bit 15 (Valid Frame) | Slot 0, bit 14 (Valid Slot 1 Address) | Slot 0, bit 13 (Valid Slot 2 Data) | Slot 0, Bits 1-0 (CODEC ID) |
|---|---------------------------------|--|---------------------------------------|--------------------------------|
| AC'97 Digital Controller Primary Read Frame N, SDATA_OUT | 1 | 1 | 0 | 00 |
| AC'97 Digital Controller Primary Write Frame N, SDATA_OUT | 1 | 1 | 1 | 00 |
| AC'97 CODEC Status Frame N+1, SDATA_IN | 1 | 1 | 1 | 00 |

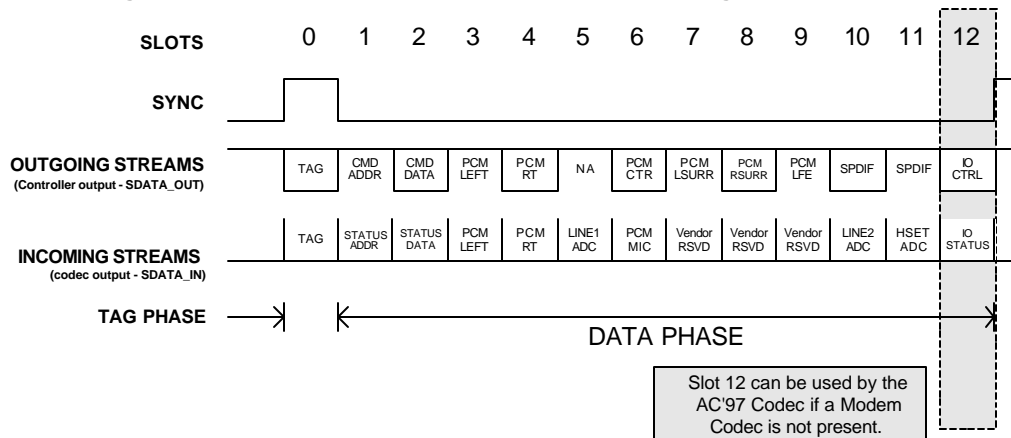
When the AC'97 Digital Controller addresses a Secondary CODEC, the Slot 0 Tag bits for Address and Data must be 0. A non-zero, 2-bit CODEC ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2.

Table 12. Secondary CODEC Addressing: Slot 0 Tag Bits

| Function | Slot 0, bit 15 (Valid Frame) | Slot 0, bit 14 (Valid Slot 1 Address) | Slot 0, bit 13 (Valid Slot 2 Data) | Slot 0, Bits 1-0 (CODEC ID) |
|---|---------------------------------|--|---------------------------------------|--------------------------------|
| AC'97 Digital Controller Secondary Read Frame N, SDATA_OUT | 1 | 0 | 0 | 01, 10, or 11 |
| AC'97 Digital Controller Secondary Write Frame N, SDATA_OUT | 1 | 0 | 0 | 01, 10, or 11 |
| AC'97 CODEC Status Frame N+1, SDATA_IN | 1 | 1 | 1 | 00 |

5.6. Slot Assignments for Audio

Figure 19. Bi-directional AC-Link Frame with Slot assignments



Note: The DAC & ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

The AC-Link output slots dedicated to audio are defined as follows:

Table 13. AC-Link Slot Definitions

| Slot | Name | Description |
|-------|--------------------|--|
| 3 | PCM L DAC playback | 20-bit PCM data for Left channel |
| 4 | PCM R DAC playback | 20-bit PCM data for Right channel |
| 6 | PCM Center | 20-bit PCM data for Center channel |
| 7 | PCM L Surround | 20-bit PCM data for L Surround channel |
| 8 | PCM R Surround | 20-bit PCM data for R Surround channel |
| 9 | PCM LFE | 20-bit PCM data for LFE channel |
| 10:11 | SPDIF Out | 20-bit SPDIF Output |
| 12 | Reserved | Reserved |

The AC-Link input slots dedicated to audio are defined as follows:

Table 14. AC-Link Input Slots Dedicated To Audio

| Slot | Name | Description |
|------|--------------------------|---|
| 3 | PCM L ADC record | 20-bit PCM data from Left input |
| 4 | PCM R ADC record | 20-bit PCM data from Right inputs |
| 6 | Dedicated Microphone ADC | 20-bit PCM data from optional 3rd ADC input |
| 7 | Vendor reserved | Vendor specific (enhanced input for docking, array mic, etc.) |
| 8 | Vendor reserved | Vendor specific (enhanced input for docking, array mic, etc.) |
| 9 | Vendor reserved | Vendor specific (enhanced input for docking, array mic, etc.) |
| 12 | Audio Interrupt | Provides optional interrupt capability for Audio CODEC (not usable when a modem is present) |

Note: The ADC can be assigned to slots 3&4, 6&9, 7&8, or 10&11.

Table 15. Audio Interrupt Slot Definitions

| Bit | Description |
|------|---|
| 19-1 | Reserved (Audio CODEC will return zeros in bits 19-1) |
| 0 | Optional: Assertion = 1 will cause interrupt to be propagated to Audio controller system interrupt. See register 24h definition for enabling mechanism. |

6. STAC9752/9753 MIXER

The STAC9752/9753 includes an analog mixer for maximum flexibility. The analog mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. The analog mixer also includes several extensions of the AC'97 specification to support "all analog record" capability as well as "POP BYPASS" mode for all digital playback. The analog sources include:

- **System Audio:** digital PCM input and output for business, games & multimedia
- **CD/DVD:** analog CD/DVD-ROM audio with internal connections to CODEC mixer
- **Mono microphone:** choice of desktop microphone, with programmable boost and gain
- **Speakerphone:** use of system microphone and speakers for telephone, DSVD, and video conferencing
- **Video:** TV tuner or video capture card with internal connections to CODEC mixer
- **AUX/synth:** analog FM or wavetable synthesizer, or other internal source
- **Line in:** external analog line level source from consumer audio, video camera, etc.

| Source | Function | Connection |
|---------|--|------------------------------|
| PC_BEEP | PC BEEP pass through to LINE_OUT | from PC_BEEP output |
| PHONE | MONO input | from telephony subsystem |
| MIC1 | desktop microphone | from microphone jack |
| MIC2 | second microphone | from second microphone jack |
| LINE_IN | external audio source | from line-in jack |
| CD | audio from CD-ROM | cable from CD-ROM |
| VIDEO | audio from TV tuner or video camera | cable from TV or VidCap card |
| AUX | upgrade synth or other external source | internal connector |
| PCM_OUT | digital audio output from AC'97 Controller | AC-Link |

| Destination | Function | Connection |
|-------------|---|---------------------------|
| HP_OUT | stereo mix of all sources | To headphone out jack |
| LINE_OUT | stereo mix of all sources | To output jack |
| MONO_OUT | microphone or MONO Analog mixer output | to telephony subsystem |
| PCM_IN | digital data from the CODEC to the AC'97 Controller | AC-Link |
| SPDIF | SPDIF digital audio output | To SPDIF output connector |

7. MIXER FUNCTIONAL DIAGRAMS

Figure 20. STAC9752 2-Channel Mixer Functional Diagram

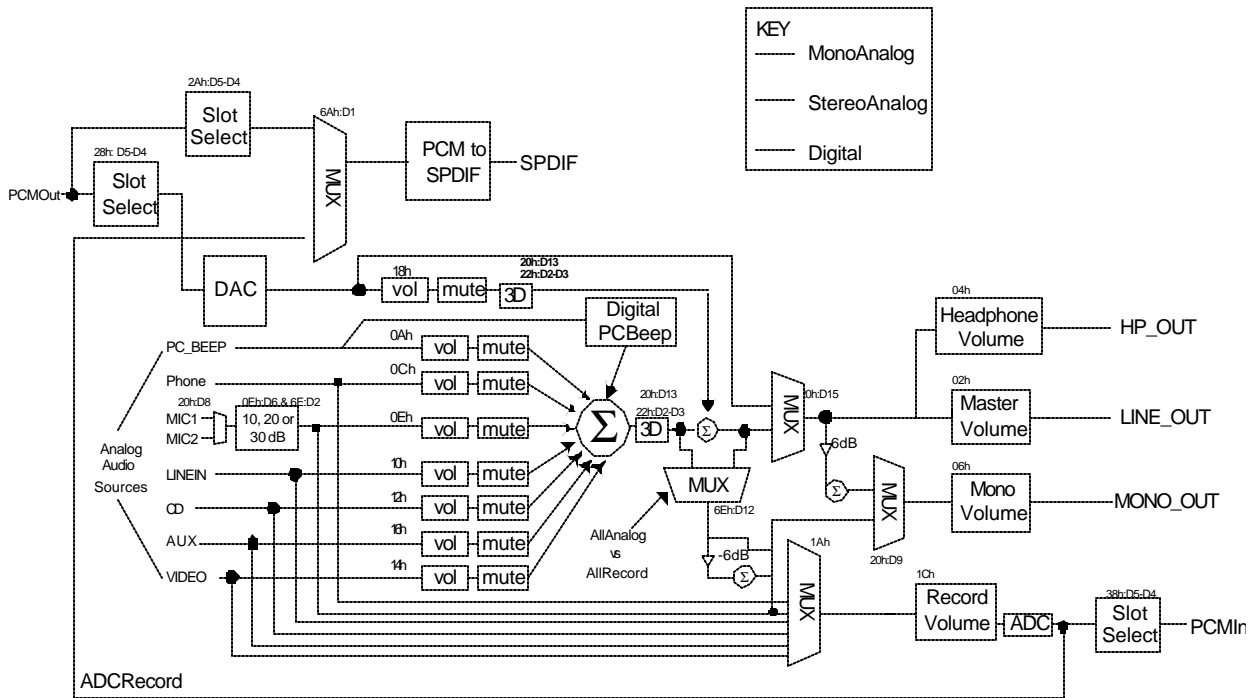
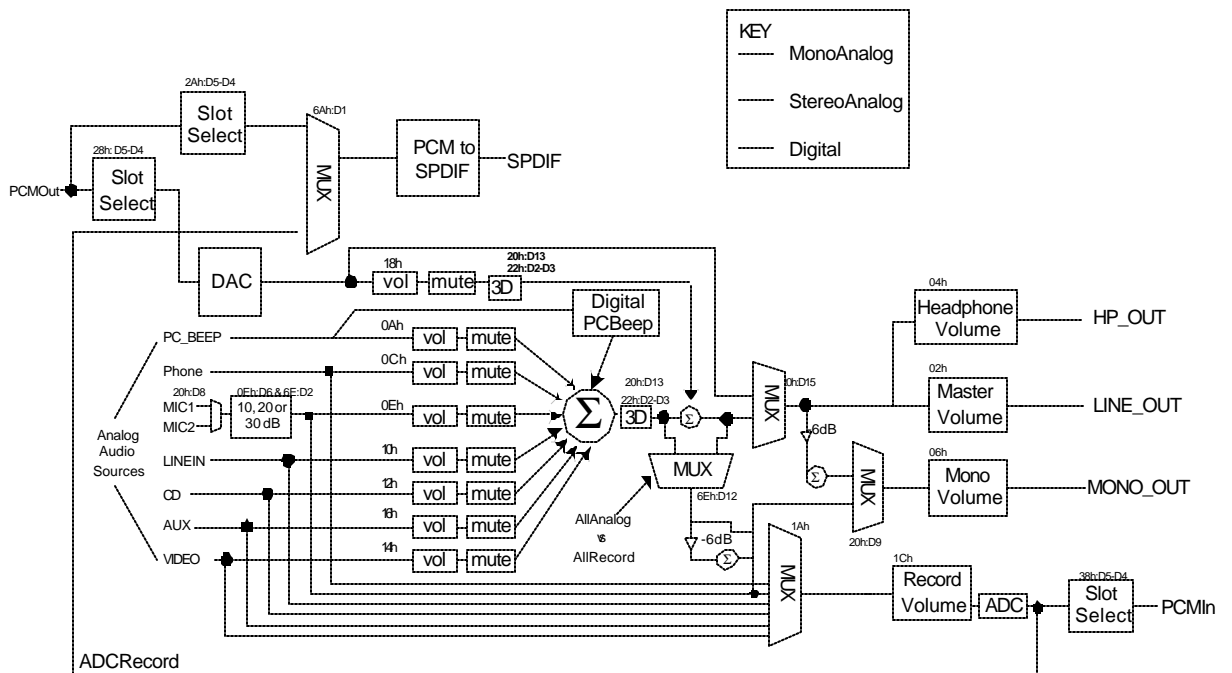


Figure 21. STAC9753 2-Channel Mixer Functional Diagram



7.1. Analog Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The STAC9752/9753 supports the following input sources:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/mono output reference (microphone or stereo mix)

Note: All unused inputs should be tied together and connected to ground through a capacitor (0.1 μ F suggested).

Note: The MIC should be tied to ground through a separate 0.1 μ F capacitor.

7.2. Mixer Analog Output

The mixer generates three distinct outputs:

- A stereo mix of all sources for output to the LINE_OUT
- A stereo mix of all sources for output to HP_OUT
- A mono, microphone only, or mix of all sources, for MONO_OUT

7.3. SPDIF Digital Mux

The STAC9752/9753 incorporates a digital output that supports SPDIF formats. A multiplexer determines which of two digital input streams are used for the digital output conversion process. These two streams include the PCM_OUT data from the audio controller and the ADC recorded output. The normal analog LINE_OUT signal can be converted to the SPDIF formats by using the internal ADC to record the "MIX" output, which is the combination of all analog and all digital sources. In the case of digital controllers with support for 4 or more channels, the SPDIF output mode can be used to support compressed 6-channel output streams for delivery to home theater systems. These can be routed on alternate AC-Link slots to the SPDIF output, while the standard 2-channel output is delivered as selected by bits D5 and D4 in Register 6E. If the digital controller supports 6 channels, a SPDIF output with 4 analog channels can also be configured.

If the Digital Controller has independent DMA engines, SPDIF and Analog can be used simultaneously and independently.

Pin 48: To Enable SPDIF, use an 1 K Ω to 10 K Ω external pulldown. To Disable SPDIF, use an 1 K Ω to 10 K Ω external pullup. Do NOT leave Pin 48 floating.

7.4. PC Beep Implementation

The STAC9752/9753 offers 2 styles of PC BEEP, Analog and Digital. The digital PC Beep is a new feature added to the AC'97 Specification Rev 2.3. This style of PC Beep will eventually replace the analog style, thus eliminating the need for a PC Beep pin. Until this feature is widely accepted, IDT will provide BOTH styles of PC Beep. Both PC Beep styles use Reg 0Ah. Additional information about Reg 0Ah can be found in Section 8.1.5: page 51.

7.4.1. Analog PC Beep

PC Beep is active on power up and defaults to an un-muted state. The PC_BEEP input is routed directly to the MONO_OUT, LINE_OUT and HP_OUT pins of the CODEC. Because the PC_BEEP input drive is often a full scale digital signal, some resistive attenuation of the PC_BEEP input is recommended to keep the beep tone within reasonable volume levels. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation. This style of PC Beep is related to the AC'97 Specification Rev 2.2. To use the analog PC Beep, a value of 00h written to bits F[7:0] (D[12:5]) disables the Digital PC Beep generation. PV[3:0] (D[4:1]) controls the volume level from 0 to 45dB of attenuation in 3dB steps.

7.4.2. Digital PC Beep

The Digital PC Beep uses the identical register as the analog style, Reg 0Ah. This register controls the level and frequency for the PC Beep. The beep frequency is the result of dividing the 48 KHz clock by 4 times the number specified in F[7:0], allowing tones from 47 Hz to 12 KHz. A value of 00h written to bits F[7:0] disables the digital PC Beep generation and enables the analog PC Beep. The volume control bits, PV[3:0] operate identically to the analog PC Beep mode. Applying a signal to the PC Beep pin, pin 12, may cause the digital PC Beep signal to become distorted or inaudible. When using the digital PC Beep feature, we recommend leaving the PC Beep input pin unconnected or connected to analog ground through a capacitor. Connecting a capacitor from the PC Beep input pin to ground will create a more pleasing sound by changing the digital output to a more sinusoidal like output.

Table 16. Digital PC Beep Examples

| Value | Reg 0Ah, bits[7:0] | Frequency |
|-------|--------------------|-----------|
| 1 | 0x01 | 12,000 Hz |
| 10 | 0x0A | 1200 Hz |
| 25 | 0x19 | 480 Hz |
| 50 | 0x32 | 240 Hz |
| 100 | 0x64 | 120 Hz |
| 127 | 0x7F | 94.48 Hz |
| 255 | 0xFF | 47.05 Hz |

This will be programmed directly by the BIOS.

8. PROGRAMMING REGISTERS

Table 17. Programming Registers

| Address | Name | Default | Location |
|----------------|-------------------------------|---------|----------------|
| 00h | Reset | 6A90h | 8.1.1; page48 |
| 02h | Master Volume | 8000h | 8.1.2; page48 |
| 04h | HP_OUT Mixer Volume | 8000h | 8.1.3; page49 |
| 06h | Master Volume MONO | 8000h | 8.1.4; page50 |
| 0Ah | PC Beep Mixer Volume | 0000h | 8.1.5; page51 |
| 0Ch | Phone Mixer Volume | 8008h | 8.1.6; page51 |
| 0Eh | Microphone Mixer Volume | 8008h | 8.1.7; page52 |
| 10h | Line In Mixer Volume | 8808h | 8.1.8; page52 |
| 12h | CD Mixer Volume | 8808h | 8.1.9; page53 |
| 14h | Video Mixer Volume | 8808h | 8.1.10; page53 |
| 16h | Aux Mixer Volume | 8808h | 8.1.11; page54 |
| 18h | PCM Out Mixer Volume | 8808h | 8.1.12; page54 |
| 1Ah | Record Select | 0000h | 8.1.13; page55 |
| 1Ch | Record Gain | 8000h | 8.1.14; page55 |
| 20h | General Purpose | 0000h | 8.1.15; page56 |
| 22h | 3D Control | 0000h | 8.1.16; page56 |
| 24h | Audio Int. & Paging | 0000h | 8.1.17; page57 |
| 26h | Powerdown Ctrl/Stat | 000Fh | 8.1.18; page58 |
| 28h | Extended Audio ID | 0A05h | 8.1.19; page59 |
| 2Ah | Extended Audio Control/Status | 0400h* | 8.1.20; page61 |
| 2Ch | PCM DAC Rate | BB80h | 8.1.22; page63 |
| 32h | PCM LR ADC Rate | BB80h | 8.1.23; page63 |
| 3Ah | SPDIF Control | 2000h | 8.1.24; page64 |
| 3Eh | Extended Modem Stat/Ctl | 0100h | 8.2.4; page65 |
| 4Ch | GPIO Pin Configuration | 0003h | 8.2.5; page66 |
| 4Eh | GPIO Pin Polarity/Type | FFFFh | 8.2.6; page66 |
| 50h | GPIO Pin Sticky | 0000h | 8.2.7; page66 |
| 52h | GPIO Wake-up | 0000h | 8.2.8; page67 |
| 54h | GPIO Pin Status | 0000h | 8.2.9; page67 |
| 60h | CODEC Class/Rev | 1201h | 8.3; page68 |
| 62h (Page 01h) | PCI SVID | FFFFh | 8.4.2; page70 |
| 64h (Page 01h) | PCI SSID | FFFFh | 8.4.3; page70 |
| 66h (Page 01h) | Function Select | 0000h | 8.4.4; page71 |
| 68h (Page 01h) | Function Information | xxxxh | 8.4.5; page72 |
| 6Ah | Digital Audio Control | 0000h | 8.4.6; page73 |
| 6Ah (Page01h) | Sense Details | NA | 8.4.7; page74 |
| 6Ch | Revision Code | xxxxh | 8.4.7; page74 |
| 6Ch (Page01h) | Reserved | 0000h | NA |
| 6Eh | Analog Special | 1000h | 8.4.9; page76 |
| 6Eh (Page01h) | Reserved | 0000h | NA |
| 70h | Enable Register | 0000h | NA |

Table 17. Programming Registers (Continued)

| Address | Name | Default | Location |
|---------|-------------------------|---------|----------------|
| 72h | Analog Current Adjust | 0000h | 8.4.10; page77 |
| 74h | EAPD Access | 0800h | 8.4.11; page77 |
| 78h | High Pass Filter Bypass | 0000h | 8.4.12; page78 |
| 7Ah | Reserved | NA | NA |
| 7Ch | Vendor ID1 | 8384h | 8.5.1; page79 |
| 7Eh | Vendor ID2 | 7652h | 8.5.2; page79 |

Note: * depends upon CODEC ID

8.1. Register Descriptions

8.1.1. Reset (00h)

Default: 6A90h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-------|-----|-----|-----|-----|-----|-----|-----|
| RSRVD | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. This register reset also resets all the digital block. Reading this register returns the ID code of the part.

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|-----------------------------------|
| 15 | 0 | RESERVED | Bit not used, should read back 0 |
| 14:10 | 11010 | SE4:SE0 | IDT ID for SS3D |
| 9 | 1 | ID9 | 20-bit ADC resolution (supported) |
| 8 | 0 | ID8 | 18-bit ADC resolution |
| 7 | 1 | ID7 | 20-bit DAC resolution (supported) |
| 6 | 0 | ID6 | 18-bit DAC resolution |
| 5 | 0 | ID5 | Loudness (bass boost) |
| 4 | 1 | ID4 | Headphone Out (supported) |
| 3 | 0 | ID3 | Simulated Stereo (mono to stereo) |
| 2 | 0 | ID2 | Bass & Treble Control |
| 1 | 0 | ID1 | Reserved |
| 0 | 0 | ID0 | Dedicated MIC PCM IN channel |

8.1.2. Master Volume Registers (02h)

Default: 8000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------|-----|-----|-----|-----|-----|-----|
| Mute | RSRVD | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 15 | 1 | Mute | 0 = No mute 1 = Mutes both left & right channels |
| 14 | 0 | RESERVED | Bit not used, should read back 0 |
| 13 | 0 | ML5 | 0 = Lineout attenuation is a function of bits12-8 1 = Forces register bits 12-8 to be 11111. Always reads back 0. |
| 12:8 | 0 | ML<4:0> | Left Lineout Volume Control 00000 = 0dB attenuation 00001 = 1.5dB attenuation 11111 = 46.5dB attenuation |
| 7:6 | 0 | RESERVED | Bits not used, should read back 0 |
| 5 | 0 | MR5 | 0 = Lineout attenuation is a function of bits 4-0 1 = Forces register bits 4-0 to be 11111 Always reads back 0 |
| 4:0 | 0 | MR<4:0> | Right Channel Lineout Volume Control 00000 = 0dB attenuation 00001 = 1.5dB attenuation 11111 = 46.5dB attenuation |

8.1.3. Headphone Volume Registers (04h)

Default: 8000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------|------|------|------|------|------|------|
| Mute | RSRVD | HPL5 | HPL4 | HPL3 | HPL2 | HPL1 | HPL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | HPR5 | HPR4 | HPR3 | HPR2 | HPR1 | HPR0 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 15 | 1 | Mute | 0 = No mute 1 = Mutes both left & right channels |
| 14 | 0 | RESERVED | Bit not used, should read back 0 |
| 13 | 0 | ML5 | 0 = Headphone attenuation is a function of bits12-8 1 = Forces register bits 12-8 to be 11111. Always reads back 0 |
| 12:8 | 0 | ML<4:0> | Left Headphone Volume Control 00000 = 0dB attenuation 00001 = 1.5dB attenuation 11111 = 46.5dB attenuation |
| 7:6 | 0 | RESERVED | Bits not used, should read back 0 |
| 5 | 0 | MR5 | 0 = Headphone attenuation is a function of bits 4-0 1 = Forces register bits 4-0 to be 11111. Always reads back 0 |
| 4:0 | 0 | MR<4:0> | Right Channel Headphone Volume Control 00000 = 0dB attenuation 00001 = 1.5dB attenuation 11111 = 46.5dB attenuation |

8.1.4. Master Volume MONO (06h)

Default: 8000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|--|-----|-----|-----|-----|
| Mute | RESERVED | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | MM5 | MM4 | MM3 | MM2 | MM1 | MM0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute mono | | | | |
| 14:6 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 5 | 0 | MM5 | 0 = Mono attenuation is a function of bits 4-0 1 = Forces register bits 4-0 to be 11111. Always reads back 0 | | | | |
| 4:0 | 0 | MM<4:0> | Mono Volume Control 00000 = 0dB attenuation 00001 = 1.5dB attenuation 11111 = 46.5dB attenuation | | | | |

8.1.5. PC BEEP Volume (0Ah)

Default: 0000h

Additional information on the PC Beep can be found in Section 7.4: page46.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | |
|------|----------|-----|-----|-----|-----|-----|-------|----|
| Mute | RESERVED | | | F7 | F6 | F5 | F4 | F3 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| F2 | F1 | F0 | PV3 | PV2 | PV1 | PV0 | RSRVD | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|--|
| 15 | 1 | Mute | 0 = No mute 1 = Mute PC BEEP |
| 14:13 | 0 | RESERVED | Bit not used, should read back 0 |
| 12:5 | 00h | F[7:0] | The Beep frequency is the result of dividing the 48 KHz clock by 4 times the value of the number specified in F[7:0], allowing tones from 47 Hz to 12 KHz. A value of 00h in bits F[7:0] disables internal PC BEEP generation and enables external PC BEEP input, if available. |
| 4:1 | 0 | PV(3:0) | PCBEEP Volume Control 0000 = 0dB attenuation 0001 = 3dB attenuation 1111 = 45dB attenuation |
| 0 | 0 | RESERVED | Bit not used, should read back 0 |

8.1.6. Phone Volume (Index 0Ch)

Default: 8008h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | RESERVED | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | GN4 | GN3 | GN2 | GN1 | GN0 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|--|
| 15 | 1 | Mute | 0 = No mute 1 = Mute phone |
| 14:5 | 0 | RESERVED | Bit not used, should read back 0 |
| 4:0 | 0 | GN<4:0> | Phone Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain |

8.1.7. Mic Volume (Index 0Eh)

Default: 8008h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|---|-----|-----|-----|-----|
| Mute | RESERVED | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | BOOSTEN | RESERVED | GN4 | GN3 | GN2 | GN1 | GN0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute phone | | | | |
| 14:7 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 6 | 0 | BOOSTEN | Works with MICGAINVAL (Register 6Eh, Bit D2) BOOSTEN MICGAINVAL = Microphone Gain Boost 0 0 = 0 dB 0 1 = 10 dB 1 0 = 20 dB 1 1 = 30 dB | | | | |
| 5 | 0 | RESERVED | | | | | |
| 4:0 | 0 | GN<4:0> | Phone Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |

8.1.8. LineIn Volume (Index 10h)

Default: 8808h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|---|-----|-----|-----|-----|
| Mute | RESERVED | | GL4 | GL3 | GL2 | GL1 | GR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute linein | | | | |
| 14:13 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 12:8 | 0 | GL<4:0> | Left LineIn Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |
| 7:5 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 4:0 | 0 | GR<4:0> | Right LineIn Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |

8.1.9. CD Volume (Index 12h)

Default: 8808h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|---|-----|-----|-----|-----|
| Mute | RESERVED | | GL4 | GL3 | GL2 | GL1 | GR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute CD | | | | |
| 14:13 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 12:8 | 0 | GL<4:0> | Left CD Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |
| 7:5 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 4:0 | 0 | GR<4:0> | Right CD Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |

8.1.10. Video Volume (Index 14h)

Default: 8808h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|--|-----|-----|-----|-----|
| Mute | RESERVED | | GL4 | GL3 | GL2 | GL1 | GR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute video | | | | |
| 14:13 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 12:8 | 0 | GL<4:0> | Left Video Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |
| 7:5 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 4:0 | 0 | GR<4:0> | Right video Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |

8.1.11. Aux Volume (Index 16h)

Default: 8808h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|--|-----|-----|-----|-----|
| Mute | RESERVED | | GL4 | GL3 | GL2 | GL1 | GR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute AUX | | | | |
| 14:13 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 12:8 | 0 | GL<4:0> | Left Aux Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |
| 7:5 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 4:0 | 0 | GR<4:0> | Right Aux Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |

8.1.12. PCMOut Volume (Index 18h)

Default: 8808h.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|---|-----|-----|-----|-----|
| Mute | RESERVED | | GL4 | GL3 | GL2 | GL1 | GR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | Mute | 0 = No mute 1 = Mute PCM OUT | | | | |
| 14:13 | 0 | RESERVED | Bit not used, should read back 0 | | | | |
| 12:8 | 0 | GL<4:0> | Left PCM Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|--|
| 7:5 | 0 | RESERVED | Bit not used, should read back 0 |
| 4:0 | 0 | GR<4:0> | Right PCM Volume Control 00000 = 12dB gain 00001 = 10.5dB gain 01000 = 0dB gain 11111 = -34.5dB gain |

8.1.13. Record Select (1Ah)

Default: 0000h (corresponding to Microphone in)

Used to select the record source independently for right and left.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|-----|-----|
| RESERVED | | | | | SL2 | SL1 | SL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | SR2 | SR1 | SR0 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 15:11 | 0 | RESERVED | Bits not used, should read back 0 |
| 10:8 | 0 | SL2:SL0 | LEFT CHANNEL INPUT SELECT 000 = Microphone 001 = CD In (left) 010 = Video In (left) 011 = Aux In (left) 100 = Line In (left) 101 = Stereo Mix (left) 110 = Mono Mix 111 = Phone |
| 7:3 | 0 | RESERVED | Bits not used, should read back 0 |
| 2:0 | 0 | SR2:SR0 | RIGHT CHANNEL INPUT SELECT 000 = Microphone 001 = CD In (right) 010 = Video In (right) 011 = Aux In (right) 100 = Line In (right) 101 = Stereo Mix (right) 110 = Mono Mix 111 = Phone |

8.1.14. Record Gain (1Ch)

Default: 8000h (corresponding to 0 dB gain with mute on)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|-----------------------------------|-----|-----|-----|-----|
| Mute | RESERVED | | | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | GR3 | GR2 | GR1 | GR0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15 | 1 | MUTE | Mutes RECORD GAIN | | | | |
| 14:12 | 0 | RESERVED | Bits not used, should read back 0 | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|--|
| 11:8 | 0 | GL<3:0> | Left Channel Volume Control 0000 = 0dB gain 0001 = 1.5dB gain 1111 = 22.5dB gain |
| 7:4 | 0 | RESERVED | Bits not used, should read back 0 |
| 3:0 | 0 | GR<3:0> | Right Channel Volume Control 0000 = 0dB gain 0001 = 1.5dB gain 1111 = 22.5dB gain |

8.1.15. General Purpose (20h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|----------|-----|-----|-----|----|
| POP BYP | RESERVED | 3D | RESERVED | | | MIX | MS |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LOOPBACK | RESERVED | | | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|------------|---|
| 15 | 0 | POP BYPASS | 0 = Normal 1 = DAC bypasses mixer and connects directly to Line Out, Headphone Out and Mono Out. |
| 14 | 0 | RESERVED | Bit not used, should read back 0 |
| 13 | 0 | 3D | 0 = 3D EFFECT disabled 1 = 3D EFFECT enabled |
| 12:10 | 0 | RESERVED | Bits not used, should read back 0 |
| 9 | 0 | MIX | Mono Output select (0 = Mix, 1 = Microphone) |
| 8 | 0 | MS | Microphone select (0 = Microphone1, 1 = Microphone2) |
| 7 | 0 | LOOPBACK | 1 = Enables ADC to DAC Loopback Test 0 = Loopback Disabled Do not send in conflicting data on AC-Link while running this. |
| 6:0 | 0 | RESERVED | Bits not used, should read back 0 |

8.1.16. 3D Control (22h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----------|----|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | DP3 | DP2 | RESERVED | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 15:4 | 0 | RESERVED | Bits not used, should read back 0 |
| 3:2 | 0 | DP3, DP2 | LINE_OUT SEPARATION RATIO DP3 DP2 effect 0 0 0 (OFF) 0 1 3 (LOW) 1 0 4.5 (MED) 1 1 6 (HIGH) |
| 1:0 | 0 | RESERVED | Bits not used, should read back 0 |

This register is used to control the 3D stereo enhancement function, **IDT Surround 3D (SS3D)**, built into the AC'97 component. Note that register bits DP3-DP2 are used to control the separation ratios in the 3D control for LINE_OUT. **SS3D** provides for a wider soundstage extending beyond the normal 2-speaker arrangement. Note that the 3D bit in the general purpose register (20h) must be set to 1 to enable SS3D functionality to allow the bits in 22h to take effect. The three separation ratios are implemented. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during 2-channel playback. The ratios provide for options to narrow or widen the soundstage.

8.1.17. Audio Interrupt and Paging (24h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|----------|-----|-----|
| I4 | I3 | I2 | I1 | I0 | RESERVED | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | PG3 | PG2 | PG1 | PG0 |

| Bit(s) | Reset Value | Access | Name | Description |
|--------|-------------|--------------|-------|---|
| 15 | 0 | Read / Write | I4 | 0 = Interrupt is clear 1 = Interrupt is set Interrupt event is cleared by writing a 1 to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the ACLink will follow this bit change when interrupt enable (I0) is unmasked. |
| 14-13 | 0 | Read Only | I3-I2 | Interrupt Cause 00 = Reserved 01 = Sense Cycle Complete, sense info available. 10 = Change in GPIO input status 11 = Sense Cycle Complete and Change in GPIO input status. These bits will reflect the general cause of the first interrupt event generated. It should be read after interrupt status has been confirmed as interrupting. The information should be used to scan possible interrupting events in proper pages. |
| 12 | 0 | Read / Write | I1 | Sense Cycle 0 = Sense Cycle not in Progress 1 = Sense Cycle Start. Writing a 1 to this bit causes a sense cycle start if supported. If sense cycle is not supported this bit is read only. |

| Bit(s) | Reset Value | Access | Name | Description |
|--------|-------------|--------------|----------|--|
| 11 | 0 | Read / Write | I0 | Interrupt Enable 0 = Interrupt generation is masked. 1 = Interrupt generation is un-masked. The driver should not un-mask the interrupt unless ensured by the AC '97 controller that no conflict is possible with modem slot 12 - GPI functionality. Some AC'97 2.2 compliant controllers will not likely support audio CODEC interrupt infrastructure. In either case, S/W should poll the interrupt status after initiating a sense cycle and wait for Sense Cycle Max Delay to determine if an interrupting event has occurred. |
| 10:4 | 0 | Read Only | RESERVED | Bits not used, should read back 0 |
| 3:0 | 0 | Read / Write | PG3:PG0 | Page Selector 0h = Vendor Specific 1h = Page ID 01 (See Section 8.4 for additional information on the Paging Registers) Fh = Reserved Pages This register is used to select a descriptor of 16 word pages between registers 60h to 6Fh. Value 0h is used to select vendor specific space to maintain compatibility with AC'97 2.2 vendor specific registers. System S/W determines implemented pages by writing the page number and reading the value back. All implemented pages must be consecutive. (i.e., page 2h cannot be implemented without page 1h). These registers are NOT reset on RESET#. |

8.1.18. Powerdown Ctrl/Stat (26h)

Default: 000Fh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|-----|-----|
| EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | REF | ANL | DAC | ADC |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|------|---|
| 15 | 0 | EAPD | 1 = Forces EAPD pad to Vdd 0 = Forces EAPD pad to GND |
| 14 | 0 | PR6 | 0 = Headphone Amp powered up 1 = Headphone Amp powered down |
| 13 | 0 | PR5 | 0 = Digital Clk active 1 = Digital Clk disable. |
| 12 | 0 | PR4 | 0 = digital active 1 = Powerdown: PLL, AC-Link, Xtal oscillator ; |
| 11 | 0 | PR3 | 0 = VREF and VREFOUT are active 1 = VREF and VREFOUT are powered down, and PR2 is asserted in analog block |
| 10 | 0 | PR2 | 0 = analog active 1 = all signal path analog is powered down |
| 9 | 0 | PR1 | 0 = DAC powered up 1 = DAC powered down |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 8 | 0 | PR0 | 0 = ADC powered up 1 = ADC powered down |
| 7:4 | 0 | RESERVED | Bit not used, should read back 0 |
| 3 | 1 | REF | Read Only --- VREF status 1 = VREFs enabled |
| 2 | 1 | ANL | Read Only ---- ANALOG MIXERS, etc. Status 1 = Analog Mixers ready. |
| 1 | 1 | DAC | Read Only ---- DAC Status 1 = DAC ready to playback |
| 0 | 1 | ADC | Read Only ---- ADC Status 1 = ADC ready to record |

8.1.18.1. Ready Status

The lower half of this register is read only status, a 1 indicating that each subsection is “ready”. Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read-only bits 0-7.

When the AC-Link “CODEC Ready” indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready. When this register is written, the bit values that come in on AC-Link will have no effect on read-only bits 0-7.

8.1.18.2. Powerdown Controls

The STAC9752/9753 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). See the section “Low Power Modes” for more information.

8.1.18.3. External Amplifier Power Down Control Output

The EAPD bit 15 of the Powerdown Control/Status Register (Index 26h) directly controls the output of the EAPD output, pin 45, and produces a logical 1 when this bit is set to logic high. This function is used to control an external audio amplifier power down. EAPD = 0 places approximately 0V on the output pin, enabling an external audio amplifier. EAPD = 1 places approximately DVdd on the output pin, disabling the external audio amplifier. Audio amplifiers that operate with reverse polarity will likely require an external inverter to maintain software driver compatibility.

EAPD can also act as a GPIO. See Section 8.4.11: page77. The GPIO controls in Section 8.2: page64 have no effect on EAPD.

8.1.19. Extended Audio ID (28h)

Default: 0A05h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|----------|------|------|-------|------|------|
| ID1 | ID0 | RESERVED | | | | AMAP | RSVD |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | DSA1 | DSA0 | RSVD | SPDIF | RSVD | VRA |

The Extended Audio ID register is a read only register except for bits D4 and D5. ID1 and ID0 echo the configuration of the CODEC as defined by the programming of pins 45 and 46 externally. The primary CODEC returns "00", while any other code identifies the CODEC as one of three secondary CODEC possibilities. The AMAP bit, D9, will return a 1 indicating that the CODEC supports the optional "AC'97 2.3 compliant AC-Link slot to audio DAC mappings". The default condition assumes that 0 is loaded into the DSA0 and DSA1 bits of the Extended Audio ID (Index 28h). With 0 in the DSA1 and DSA0 bits, the CODEC slot assignments are as per the AC'97 specification recommendations. If the DSA1 and DSA0 bits do not contain 0, the slot assignments are as per the table in the section describing the Extended Audio ID (Index 28h). The VRA bit, D0, will return a 1 indicating that the CODEC supports the optional variable sample rate conversion as defined by the AC'97 specification.

Table 18. Extended Audio ID Register Functions

| Bit | Name | Access | Reset Value | Function |
|-------|-----------|------------|-------------|---|
| 15:14 | ID [1,0] | Read only | variable | 0,0 = XTAL_OUT grounded (Note 1) CID1#, CID0# = XTAL_OUT crystal or floating |
| 13:12 | RESERVED | Read only | 00 | Bits not used, should read back 00 |
| 11:10 | REV[1:0] | Read only | 10 | Indicates CODEC is AC'97 Rev 2.3 compliant |
| 9:6 | RSVD | Read only | 0 | Reserved |
| 5:4 | DSA [1,0] | Read/Write | 00 | DAC slot assignment If CID[1:0] = 00 then DSA[1:0] resets to 00 If CID[1:0] = 01 then DSA[1:0] resets to 01 If CID[1:0] = 10 then DSA[1:0] resets to 01 If CID[1:0] = 11 then DSA[1:0] resets to 10 00 = left slot 3, right slot 4 01 = left slot 7, right slot 8 10 = left slot 6, right slot 9 11 = left slot 10, right slot 11 |
| 3 | RSVD | Read only | 0 | RESERVED |
| 2 | SPDIF | Read only | 1 | 0 = SPDIF pulled high on reset, SPDIF disabled 1 = default, SPDIF enabled (Note 2) |
| 1 | RSVD | Read only | 0 | RESERVED |
| 0 | VRA | Read only | 1 | Variable sample rates supported (Always = 1) |

- External CID pin status (from analog) these bits are the logical inversion of the pin polarity (pin 45-46). These bits are zero if XTAL_OUT is grounded with an alternate external clock source in primary mode only. Secondary mode can either be through BIT CLK driven or 24MHz clock driver, with XTAL_OUT floating.
- If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available.
Pin 48: To Enable SPDIF, use an external 1K Ω - 10K Ω pulldown resistor. To Disable SPDIF, use an external 1K Ω - 10K Ω pullup resistor. Do NOT leave Pin 48 floating.

8.1.20. Extended Audio Control/Status (2Ah)

Default: 0400h* (*default depends on CODEC ID)

| | | | | | | | |
|----------|----------|-------|-------|-------|-------|----------|------------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| VCFG | RESERVED | | | | SPCV | RESERVED | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | SPSA1 | SPSA0 | RSRVD | SPDIF | RSRVD | VRA enable |

Note: If pin 48 is held high at powerup, the SPDIF is not available and bits D15:D1 can not be written and will read back zero.

Pin 48: To Enable SPDIF, use an external 1K Ω - 10K Ω pulldown resistor. To Disable SPDIF, use an external 1K Ω - 10K Ω pullup resistor. Do NOT leave Pin 48 floating.

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|-------------|---|
| 15 | | VCFG | Determines the SPDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the deassertion of the SPDIF "Validity" flag, which is bit 28 transmitted by the SPDIF sub-frame. The "V" bit is defined in the SPDIF Control Register (Reg 3Ah). If "V" = 1 and "VCFG" = 0, then for each S/PDIF sub-frame (Left & Right), bit[28] "Validity" flag reflects whether or not an internal CODEC transmission error has occurred. Specifically an internal CODEC error should result in the "Validity" flag being set to 1. If "V" = 0 and "VCFG" = 1, In the case where the S/PDIF transmitter does not receive a valid sample from the AC'97 controller, (Left or Right), the S/PDIF transmitter should set the "Validity" flag to "0" and pad the "Audio Sample Word" with "0"s for sub-frame in question. If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be "0" for that sub-frame. Default state, coming out of reset, for "V" and "VCFG" should be 0 and 0. These bits can be set via driver .inf options. |
| 14-11 | | Reserved | Reserved |
| 10 | 0 | SPCV | 0 = Invalid SPDIF configuration 1 = Valid SPDIF configuration |
| 9:6 | 0 | Reserved | Bit not used, should read back 0 |
| 5:4 | 0 | SPSA1:SPSA0 | SPDIF slot assignment If CID[1:0] = 00 then SPSA[1:0] resets to 01 If CID[1:0] = 01 then SPSA[1:0] resets to 10 If CID[1:0] = 10 then SPSA[1:0] resets to 10 If CID[1:0] = 11 then SPSA[1:0] resets to 11 00 = left slot 3, right slot 4 01 = left slot 7, right slot 8 10 = left slot 6, right slot 9 11 = left slot 10, right slot 11 |
| 3 | | Reserved | Reserved |
| 2 | 0 | SPDIF | 0 = Disables SPDIF (SPDIF_OUT is high Z) (note 1) 1 = Enable SPDIF SPDIF is a control register for Reg 3Ah, this bit must be set low i.e. SPDIF disabled in order to write to Reg 3Ah Bits D15,D13:D0. |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|------------|--|
| 1 | 0 | Reserved | Bit not used, should read back 0 |
| 0 | 0 | VRA Enable | 0 = VRA Disabled, DAC and ADC set to 48 KHz (Registers 2Ch and 32h loaded with the value BB80h) 1 = VRA Enabled, Reg. 2Ch & 32h control sample rate |

8.1.20.1. Variable Rate Sampling Enable

The Extended Audio Status Control register also contains one active bit to enable or disable the Variable Sampling Rate capabilities of the DACs and ADCs. If the VRA (bit D0) is 1, the variable sample rate control registers (2Ch and 32h) are active, and “on-demand” slot data required transfers are allowed. If the VRA bit is 0, the DACs and ADCs will operate at the default 48 KHz data rate.

The STAC9752/9753 supports “on-demand” slot request flags. These flags are passed from the CODEC to the AC'97 controller in every audio input frame. Each time a slot request flag is set (active low) in a given audio frame, the controller will pass the next PCM sample for the corresponding slot in the audio frame that immediately follows. The VRA enable bit must be set to 1 to enable “on-demand” data transfers. If the VRA enable bit is not set, the CODEC defaults to 48 KHz transfers and every audio frame includes an active slot request flag and data transfers every frame.

For variable sample rate output, the CODEC examines its sample rate control registers, the state of the FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits are asserted during the current audio input frame for active output slots, which will require data in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the CODEC is always the master: for SDATA_IN (CODEC to Controller), the CODEC sets the TAG bit; for SDATA_OUT (Controller to CODEC), the CODEC sets the SLOTREQ bit and then checks for the TAG bit in the next frame. Whenever VRA is set to 0, the PCM rate registers (2Ch and 32h) are overwritten with BB80h (48 KHz).

8.1.20.2. SPDIF

The SPDIF bit in the Extended Audio Status Control Register is used to enable and disable the SPDIF functionality within the STAC9752/9753. If the SPDIF is set to a 1, then the function is enabled, and when set to a 0 it is disabled.

8.1.20.3. SPCV (SPDIF Configuration Valid)

The SPCV bit is read only and indicates whether or not the SPDIF system is set up correctly. When SPCV is a 0, it indicates the SPDIF configuration is invalid. When SPCV is a 1, it indicates the SPDIF configuration is valid.

8.1.20.4. SPSA1, SPSA0 (SPDIF Slot Assignment)

SPSA1 and SPSA0 combine to provide the slot assignments for the SPDIF data. The following details the slot assignment relationship between SPSA1 and SPSA0.

The STAC9752/9753 are AMAP compliant with the following table.

Table 19. AMAP compliant

| CODEC ID | Function | SPSA = 00 slot assignment | SPSA = 01 slot assignment | SPSA = 10 slot assignment | SPSA = 11 slot assignment |
|----------|-------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| 00 | 2-ch Primary w/SPDIF | 3 & 4 | 7 & 8* | 6 & 9 | 10 & 11 |
| 01 | 2-ch Dock CODEC w/SPDIF | 3 & 4 | 7 & 8 | 6 & 9* | 10 & 11 |
| 10 | +2-ch Surr w/ SPDIF | 3 & 4 | 7 & 8 | 6 & 9* | 10 & 11 |
| 11 | +2-ch Cntr/LFE w/ SPDIF | 3 & 4 | 7 & 8 | 6 & 9 | 10 & 11* |

Note: * indicates the default slot assignment

8.1.21. PCM DAC Rate Registers (2Ch and 32h)

The internal sample rate for the DACs and ADCs are controlled by a value in these read/write registers (that contain a 16-bit unsigned value between 0 and 65535) representing the conversion rate in Hertz (Hz). In VRA mode (register 2Ah bit D0 = 1), if the value written to these registers is supported, that value will be echoed back when read; otherwise the closest (higher in the case of a tie) sample rate is supported and returned. Per PC 99 / PC 2001 specification, independent sample rates are supported for record and playback.

Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) will be loaded with BB80h (48 KHz).

If VRA is set to a 0, any write to this address will be ignored and the rate remains at 48 KHz.

Table 20. Hardware Supported Sample Rates

| Sample Rate | SR[15:0] Value |
|-------------|----------------|
| 8 KHz | 1F40h |
| 11.025 KHz | 2B11h |
| 16 KHz | 3E80h |
| 22.05 KHz | 5622h |
| 32 KHz | 7D00h |
| 44.1 KHz | AC44h |
| 48 KHz | BB80h |

8.1.22. PCM DAC Rate (2Ch)

Default: BB80h (see table20: page63)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |

8.1.23. PCM LR ADC Rate (32h)

Default: BB80h (see table20: page63)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |

8.1.24. SPDIF Control (3Ah)

Default: 2000h

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|-----------|-----------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| V | DRS | SPSR1 | SPSR2 | L | CC6 | CC5 | CC4 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CC3 | CC2 | CC1 | CC0 | PRE | COPY | /AUDIO | PRO |

| Bit(s) | Reset Value | Access | Name | Description (note 1-2) |
|-----------|-------------|--------------|-----------|--|
| 15 in 2.3 | | | V | Validity: This bit affects the "Validity" flag, bit[28] transmitted in each S/PDIF subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. Subframe bit[28] = 0 indicates that data is valid for conversion at the receiver, 1 indicates invalid data (not suitable for conversion at the receiver). If "V" = 1, then each S/PDIF subframe (Left & Right) should have bit[28] "Validity" flag = 1 or set based on the assertion or de-assertion of the AC'97 "VFORCE" bit within the Extended Audio Status and Control Register (D15, register 2Ah). |
| 14 | 0 | Read Only | DRS | 1 = Double Rate SPDIF support (always = 0) |
| 13:12 | 10 | Read & Write | SPSR[1,0] | SPDIF Sample Rate. 00 - 44.1 KHz Rate 01 - Reserved 10 - 48 KHz Rate (default) 11 - 32 KHz Rate |
| 11 | 0 | Read & Write | L | Generation Level is defined by the IEC standard, or as appropriate. |
| 10:4 | 0 | Read & Write | CC[6, 0] | Category Code is defined by the IEC standard or as appropriate by media. |
| 3 | 0 | Read & Write | PRE | 0 = Pre-emphasis = 0 μsec 1 = Pre-emphasis = 50/15 μsec |
| 2 | 0 | Read & Write | COPY | 0 = Copyright not asserted 1 = Copyright is asserted |
| 1 | 0 | Read & Write | /AUDIO | 0 = PCM data 1 = Non-Audio or non-PCM format |
| 0 | 0 | Read & Write | PRO | 0 = Consumer use of the channel 1 = Professional use of the channel |

8.2. General Purpose Input & Outputs**8.2.1. EAPD**

EAPD can act as a GPIO, but is unaffected by the following registers. To use EAPD as a GPIO, use Register 74h, the EAPD Access Register located in Section 8.4.11: page77. Additional information about EAPD can also be found in Section 8.1.18.3: page 59.

8.2.2. GPIO Pin Definitions

GPIO pins are programmable to have input/output functionality. The data values (status) for these pins are all in one register with input/output configuration in a separate register. Control of GPIO pins configured for output is achieved by setting the corresponding bit in output slot 12; status of GPIO pins configured for input is returned on input slot 12. The CODEC must constantly set the GPIO pins that are configured for output, based upon the value of the corresponding bit position of the control slot 12. The CODEC should ignore output slot 12 bits that correspond to GPIO control pins configured as inputs. The CODEC must constantly update status on input slot 12, based upon the logic level detected at each GPIO pin configured for input. A GPIO output pin value that is written via slot 12 in the current frame will not affect the GPIO status that is returned in that particular write frame.

This slot-12 based control/status protocol minimizes the latency and complexity, especially for host-based Controllers and host data pump software, and provides high speed monitoring and control, above what could be achieved with command/status slots. For host-based implementations, most AC'97 registers can be shadowed by the driver in order to provide immediate response when read by the processor, and GPIO pins configured as inputs should be capable of triggering an interrupt upon a change of status.

The AC-Link request for GPIO pin status is always delayed by at least one frame time. Read-Modify-Write operations across the AC-Link will incur latency that must be accounted for by the software driver or AC'97 Digital Controller firmware. PCI retries should be kept to a minimum wherever possible.

8.2.3. GPIO Pin Implementation

The GPIOs are set to a high impedance state on power-on or a cold reset. It is up to the AC'97 Digital Controller to first enable the output after setting it to the desired state.

8.2.4. Extended Modem Status and Control Register (3Eh)

Default: 0100h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------|-------------|----------|---|-----|----|------|
| RESERVED | | | | | | | PRA |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | | GPIO |
| Bit(s) | Access | Reset Value | Name | Description | | | |
| 15:9 | Read Only | 0 | RESERVED | Bit not used, should read back 0 | | | |
| 8 | Read / Write | 1 | PRA | 0 = GPIO powered up / enabled 1 = GPIO powered down / disabled | | | |
| 7:1 | Read Only | 0 | RESERVED | Bit not used, should read back 0 | | | |
| 0 | Read Only | 0 | GPIO | 0 = GPIO not ready (powered down) 1 = GPIO ready (powered up) | | | |

8.2.5. GPIO Pin Configuration Register (4Ch)

Default: 0003h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------|-------------|----------|---|-----|----------------|----------------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | GC1 (GPIO1) | GC0 (GPIO0) |
| Bit(s) | Access | Reset Value | Name | Description | | | |
| 15:2 | Read Only | 0 | RESERVED | Bit not used, should read back 0 | | | |
| 1 | Read / Write | 1 | GC1 | 0 = GPIO1 configured as output 1 = GPIO1 configured as input | | | |
| 0 | Read / Write | 1 | GC0 | 0 = GPIO0 configured as output 1 = GPIO0 configured as input | | | |

8.2.6. GPIO Pin Polarity/Type Register (4Eh)

Default: FFFFh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------|-------------|----------|--|-----|----------------|----------------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | GP1 (GPIO1) | GP0 (GPIO0) |
| Bit(s) | Access | Reset Value | Name | Description | | | |
| 15:2 | Read Only | 0 | RESERVED | Bit not used, should read back 0 | | | |
| 1 | Read / Write | 1 | GP1 | 0 = GPIO1 Input Polarity Inverted, CMOS output drive. 1 = GPIO1 Input Polarity Non-inverted, Open-Drain output drive. | | | |
| 0 | Read / Write | 1 | GP0 | 0 = GPIO0 Input Polarity Inverted, CMOS output drive. 1 = GPIO0 Input Polarity Non-inverted, Open-Drain output drive. | | | |

8.2.7. GPIO Pin Sticky Register (50h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------|-------------|----------|--|-----|----------------|----------------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | GS1 (GPIO1) | GS0 (GPIO0) |
| Bit(s) | Access | Reset Value | Name | Description | | | |
| 15:2 | Read Only | 0 | RESERVED | Bit not used, should read back 0 | | | |
| 1 | Read / Write | 0 | GS1 | 0 = GPIO1 Non Sticky configuration. 1 = GPIO1 Sticky configuration. | | | |
| 0 | Read / Write | 0 | GS0 | 0 = GPIO0 Non Sticky configuration. 1 = GPIO0 Sticky configuration. | | | |

8.2.8. GPIO Pin Mask Register (52h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------|-------------|----------|---|-----|----------------|----------------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | GW1 (GPIO1) | GW0 (GPIO0) |
| Bit(s) | Access | Reset Value | Name | Description | | | |
| 15:2 | Read Only | 0 | RESERVED | Bit not used, should read back 0 | | | |
| 1 | Read / Write | 0 | GW1 | 0 = GPIO1 interrupt not passed to GPIO_INT slot 12. 1 = GPIO1 interrupt is passed to GPIO_INT slot 12. | | | |
| 0 | Read / Write | 0 | GW0 | 0 = GPIO0 interrupt not passed to GPIO_INT slot 12. 1 = GPIO0 interrupt is passed to GPIO_INT slot 12. | | | |

8.2.9. GPIO Pin Status Register (54h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------|-------------|----------|--|-----|-------------|-------------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | GI1 (GPIO1) | GI0 (GPIO0) |
| Bit(s) | Access | Reset Value | Name | Description | | | |
| 15:2 | Read Only | 0 | RESERVED | Bits not used, should read back 0 | | | |
| 1 | Read / Write | x | GI1 | When GPIO1 is configured as output and Register h74 bit[0] = 0 (default), the value of this register will be placed on the GPIO1 pad. When GPIO1 is configured as output and Register h74 bit[0] = 1, the GPIO1 pad will get its value from slot12. When GPIO1 is configured as input and configured as a sticky bit, writing a 1 does nothing, writing a 0 clears this bit. When GPIO1 is configured as input, this register reflects the value on the GPIO1 pad after interpretation of the polarity and sticky configurations. | | | |
| 0 | Read / Write | x | GI0 | When GPIO0 is configured as output and Register h74 bit[0] = 0 (default), the value of this register will be placed on the GPIO0 pad. When GPIO0 is configured as output and Register h74 bit[0] = 1, the GPIO0 pad will get its value from slot12. When GPIO0 is configured as input and configured as a sticky bit, writing a 1 does nothing, writing a 0 clears this bit. When GPIO0 is configured as input, this register reflects the value on the GPIO0 pad after interpretation of the polarity and sticky configurations. | | | |

8.3. Extended CODEC Registers Page Structure Definition

Registers 60h-68h are the Extended CODEC Registers: These registers allow for the definition of further capabilities. These bits provide a paged address space for extended CODEC information. The Page Selector bits in the Audio Interrupt and Paging register (Register 24h bits 3:0) control the page of information viewed through this page window.

8.3.1. *Extended Registers Page 00*

Page 00 of the Extended CODEC Registers is reserved for vendor specific use. Driver writers should not access these registers unless the Vendor ID register has been checked first to ensure that the vendor of the AC'97 component has been identified and the usage of the vendor defined registers understood.

8.3.2. *Extended Registers Page 01*

The usage of Page 01 of the Extended CODEC Registers is defined in Register 24h found in Section 8.1.17: page 57.

8.3.3. *Extended Registers Page 02, 03*

Pages 02 and 03 of the Extended CODEC Registers are reserved for future use.

8.4. STAC9752/9753 Paging Registers

The AC'97 Specification Rev 2.3 uses a paging mechanism in order to increase the number of registers. The registers currently used in the paging are 60h to 6Eh. For additional information about the Extended CODEC Registers, please refer to Section 8.3: page68.

One of two pages can be made active at any time, set in Register 24h. Register 24h is the Audio Interrupt and Paging Register. Additional details about Register 24h is located in Section 8.1.17: page57.

If page 00h is active, registers 60h to 6Eh are Vendor Specific.

If page 01h is active, registers 60h to 6Eh have the following functionality:

| Reg | NAME | FUNCTION | Location |
|-----|----------------------|--|---------------|
| 60h | CODEC Class/Revision | Provides the CODEC Class and a Vendor specified revision identifier. | 8.4.1: page69 |
| 62h | PCI SVID | Allows for population by the system BIOS to identify the PCI Sub System Vendor ID. | 8.4.2: page70 |
| 64h | PCI SSID | Allows for population by the system BIOS to identify the PCI Sub System ID. | Note:: page70 |
| 66h | Function Select | Provides the type of audio function being selected and which jack conductor the selected value is measured from. | Note:: page70 |
| 68h | Function Information | Includes information about Gain, Inversion, Buffer delays, Information Validity, and Function Information presence. | 8.4.5: page72 |
| 6Ah | Sense Register | Includes information about the connector/jack location, Input verses Output sensing, the order of the sense results, and the IDT specific sense results. | 8.4.7: page74 |
| 6Ch | | Reserved | |
| 6Eh | | Reserved | |

8.4.1. CODEC Class/Rev (60h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: 12xxh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|----------------------|-----|-----|-----|-----|
| RESERVED | | | CL4 | CL3 | CL2 | CL1 | CL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RV7 | RV6 | RV5 | RV4 | RV3 | RV2 | RV1 | RV0 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15-13 | | Reserved | Reserved-not defined | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|---------|---|
| 12-8 | | CL4:CL0 | CODEC Compatibility Class (RO) This is a CODEC vendor specific field to define software compatibility for the CODEC. Software reads this field together with the CODEC vendor ID (reg 7C-7Eh) to determine vendor specific programming interface compatibility. Software can rely on vendor specific register behavior to be compatible among vendor CODECs of the same class. 00h - Field not implemented 01h-1Fh - Vendor specific compatibility class code Equals Vendor ID2 (Reg 7Eh) bits D7 to D0 |
| 7-0 | | RV7:RV0 | Revision ID: (RO) This register specifies a device specific revision identifier. The value is chosen by the vendor. Zero is an acceptable value. This field should be viewed as a vendor defined extension to the CODEC ID. This number changes with new CODEC stepping of the same CODEC ID. Equals Major Rev bits (Reg 6Ch) bits D7 to D0. |

8.4.2. PCI SVID (62h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: FFFFh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-------|-------|-------|-------|-------|-------|------|------|
| PVI15 | PVI14 | PVI13 | PVI12 | PVI11 | PVI10 | PVI9 | PVI8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PVI7 | PVI6 | PVI5 | PVI4 | PVI3 | PVI2 | PVI1 | PVI0 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|------------|---|
| 15-0 | | PVI15:PVI0 | PCI Sub System Vendor ID: This field provides the PCI Sub System Vendor ID of the Audio or Modem Sub Assembly Vendor (i.e., CNR Manufacturer, Motherboard Vendor). This is NOT the CODEC vendor PCI Vendor ID, nor the AC'97 Controller PCI Vendor ID. If data is not available, returns FFFFh. |

Note: This register is populated by the BIOS and does not reset on RESET#.

8.4.3. PCI SSID (64h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: FFFFh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| PI15 | PI14 | PI13 | PI12 | PI11 | PI10 | PI9 | PI8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| PI7 | PI6 | PI5 | PI4 | PI3 | PI2 | PI1 | PI0 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 15-0 | | PI15:PI0 | PCI Sub System ID: This field provides the PCI Sub System ID of the Audio or Modem Sub Assembly (i.e., CNR Model, Motherboard SKU). This is NOT the CODEC vendor PCI ID, nor the AC'97 Controller PCI ID. Information in this field must be available for AC'97 controller reads when CODEC Ready is asserted in AC-Link. If data is not available, returns FFFFh. |

Note: This register is populated by the BIOS and does not reset on RESET#.

8.4.4. Function Select (66h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|---|-----|-----|-----|-----|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | FC3 | FC2 | FC1 | FC0 | T/R |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15-5 | | Reserved | Reserved | | | | |
| 4-1 | 00h | FC3:FC0 | Function Code bits: 00h - Line Out (Master Out) 01h - Head Phone Out (AUX Out) Setting the T/R bit to 0 = Left, 1 = Right 02h - DAC 3 (C/LFE) - Not Supported 03h - SPDIF out 04h - Phone In 05h - Mic1 (Microphone select = 0) 06h - Mic2 (Microphone select = 1) 07h - Line In 08h - CD In 09h - Video In 0Ah - Aux In 0Bh - Mono Out 0C-0Fh - Reserved For supported Jack and Microphone Sense Functions, see Table21: page71. The Function Code Bits are used to read Register 68h (Page 01h) and Register 6Ah (Page 01h). Mono I/O should report relevant sense and function information on Tip, and report Not-Supported on Ring. Setting the function code to unsupported values will return a 0 when accessing the Information Valid Bit in Page 01, Register 68h, bit 5. | | | | |
| 0 | 0 | T/R | Tip or Ring Selection Bit. This bit sets which jack conductor the sense value is measured from. Software will program the corresponding the Ring/Tip selector bit together with the I/O number in bits FC[3:0]. 0 - Tip (Left) 1 - Ring (Right) | | | | |

Note: This register does not reset on RESET#.

Table 21. Supported Jack and Microphone Sense Functions

| Function Code | I/O | Sense Capability |
|---------------|---------------|------------------|
| 00h | Line_Out | Jack Sense |
| 01h | Headphone_Out | Jack Sense |
| 05h | Mic1 | Microphone Sense |
| 06h | Mic2 | Microphone Sense |

8.4.5. Function Information (68h Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: 00xxh, see table 22: page73.

| | | | | | | | |
|-----|-----|-----|-----|----------|-----|-----|-----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| G4 | G3 | G2 | G1 | G0 | INV | DL4 | DL3 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| DL2 | DL1 | DL0 | IV | RESERVED | | | FIP |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|---------|---|
| 15 | 0 | G4 | Gain Sign Bit: The CODEC updates this bit with the sign of the gain value present in G[3:0]. The BIOS updates this to take into consideration external amplifiers or other external logic when relevant. G[4] indicates whether the value is a gain or attenuation. Gain in the G4 bit is in terms of dB. This bit is Read/Write and is only reset on POR and not by RESET#. |
| 14-11 | 0 | G3:G0 | Gain Bits: The CODEC updates these bits with the gain value (db relative to level-out) in 1.5dBV increments. The BIOS updates these to take into consideration external amplifiers or other external logic when relevant. G[0:3] indicates the magnitude of the gain. G[4] indicates whether the value is a gain or attenuation. For Gain/Attenuation settings, see Table 23: page73. These bits are read/write and are not reset on RESET#. |
| 10 | | INV | Inversion bit: Indicates that the CODEC presents a 180 degree phase shift to the signal. 0h - No inversion reported 1h - Inverted This bit is read/write and is not reset on RESET#. BIOS should invert for each inverting gain stage. |
| 9-5 | | DL4:DL0 | Buffer delays: CODEC will provide number a delay measurement for the input and output channels. Software will use this value to accurately calculate audio stream position with respect to what is been reproduced or recorded. These values are in 20.83 μ s (1/48000 second) units. For output channels, this timing is from the end of AC Link frame in which the sample is provided, until the time the analog signal appears at the output pin. For input streams, this is from when the analog signal is presented at the pin until the representative sample is provided on the AC Link. Analog in and out paths are not considered as part of this delay. The measurement is a "typical" measurement, at a 48 KHz sample rate, with minimal in-CODEC processing (i.e., 3D effects are turned off.) 00h - Information not provided 01h...1Eh - Buffer delay in 20.83 μ s units 1Fh - reserved These bits are read/write and are not reset on RESET#. The default value is the delay internal to the CODEC. The BIOS may add to this value the known delays external to the CODEC, such as for an external amplifier. |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 4 | 1 | IV | Information Valid Bit: Indicates whether a sensing method is provided by the CODEC and if information field is valid. This field is updated by the CODEC. 0 - After CODEC RESET# de-assertion, it indicates the CODEC does NOT provide sensing logic and this bit will be Read Only. After a sense cycle is completed, indicates that no information is provided on the sensing method. 1 - After CODEC RESET# de-assertion, it indicates the CODEC provides sensing logic for this I/O and this bit is Read/Write. After clearing this bit by writing 1, when a sense cycle is completed the assertion of this bit indicates that there is valid information in the remaining descriptor bits. Writing 0 to this bit has no effect. BIOS should NOT write this bit, as it is reset on RESET#. |
| 3-1 | 0 | RESERVED | Bits not used, should read back 0 |
| 0 | NA | FIP | Function Information Present This bit set to a 1 indicates that the G[4:0], INV, DL[4:0] (Register 68h, Page 01h) and ST[2:0] (register 6Ah, Page 01h) are supported and R/W capable. This bit is Read Only. |

Table 22. Reg 68h Default Values

| Reg 66h Function Code | Reg 68h Default Value |
|--------------------------|-----------------------|
| 00h Line Out | 0010h |
| 01h Headphone Out | 0010h |
| 05h Mic1 | 0010h |
| 06h Mic2 | 0010h |
| All other Function Codes | 0000h |

For RESET#: Reg 68h default value is 0000h.

Table 23. Gain or Attenuation Examples

| G[4:0] | Gain or Attenuation (dB relative to level-out) |
|--------|--|
| 00000 | 0 dBV |
| 00001 | +1.5 dBV |
| 01111 | +24 dBV |
| 10001 | -1.5 dBV |
| 11111 | -24 dBV |

Table 24. Register 68h/Page 01h Bit Overview

| Bit | Bit R/W Overview |
|--------|--|
| D15:D5 | Read/Write and only reset on POR (Power on Reset) and not by RESET#. |
| D4 | Read/Write and should NOT be set by the BIOS |
| D3:1 | Reserved |
| D0 | Read Only. |

8.4.6. Digital Audio Control (6Ah, Page 00h)

To access Register 6Ah, Page 00h must be selected in Register 24h.

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|--|-----|------|-----|------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | SPOR | DO1 | RSVD |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15:3 | 0 | RESERVED | Bits not used, should read back 0 | | | | |
| 2 | 0 | SPOR | Over-ride Register 2Ah, D12 write-lock when SPDIF_EN = 1. All bits except SPDIF sample-rate are affected (D13-D12). Allows for sub-code changing on-the-fly. | | | | |
| 1 | 0 | DO1 | SPDIF Digital Output Source Selection: DO1 = 0; PCM data from the AC-Link to SPDIF DO1 = 1; ADC record data to SPDIF | | | | |
| 0 | 0 | RESERVED | Bits not used, should read back 0 | | | | |

8.4.7. Sense Details (6Ah Page 01h)

Register 24h must be set to Page 01h to access this register.

Default: NA

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|--------|-------------|---------|---|-----|-----|-----|-----|
| ST2 | ST1 | ST0 | S4 | S3 | S2 | S1 | S0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OR1 | OR0 | SR5 | SR4 | SR3 | SR2 | SR1 | SR1 |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15-13 | | ST2:ST0 | Connector/Jack location bits This field describes the location of the jack in the system. 0h - Rear I/O Panel 1h - Front Panel 2h - Motherboard 3h - Dock/External 4h:6h - Reserved 7h - No Connection/unused I/O These bits are Read/Write. | | | | |
| 12-8 | | S4:S0 | Sensed bits meaning relates to the I/O being sense as output or inputs. Sensed bits (outputs): See Table 25: page75. This field allows for the reporting of the type of output peripheral/device plugged in the jack. Values specified below should be interrogated in conjunction with the SR[5:0] and OR[1:0] bits for accurate reporting. Sensed bits (inputs): See Table 26: page75. This field allows for the reporting of the type of input peripheral/device plugged in the jack. Values specified below should be interrogated in conjunction with the SR[5:0] and OR[1:0] bits for accurate reporting. This field is Read Only. | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|---------|--|
| 7-6 | | OR1:0 | Order Bits. These bits indicate the order the sense result bits SR[5:0] are using. 00 - 10^0 (i.e., Ohms) 01 - 10^1 (i.e., 10 Ohms) 10 - 10^2 (i.e., 100 Ohms) 11 - 10^3 (i.e., 1K Ohms) |
| 5-0 | | SR5:SR0 | Sense Result bits These bits are used to report a vendor specific fingerprint or value. (Resistance, impedance, reactance, etc.). This field is Read Only. |

Table 25. Sensed Bits (Outputs)

| Reported Value | Output Peripheral/Device |
|----------------|--|
| 0h | Data not valid. Indicates that the reported value(s) is (are) invalid. |
| 1h | No connection. Indicates that there are no connected devices. |
| 2h | Fingerprint. Indicates a specific fingerprint value for devices that are not specified or unknown. |
| 3h | Speakers (8 ohms) |
| 4h | Speakers (4 ohms) |
| 5h | Powered Speakers |
| 6h | Stereo Headphone |
| 7h | Reserved |
| 8h | Reserved |
| 9h | Headset (mono speaker left channel and microphone.) |
| Ah | Other. Allows a vendor to report sensing other type of devices/peripherals. SR[5:0] together with OR[1:0] provide information regarding the type of device sensed. |
| Bh-Eh | Reserved |
| Fh | Unknown (use fingerprint) |

Table 26. Sensed Bits (Inputs)

| Reported Value | Input Peripheral/Device |
|----------------|--|
| 0h | Data not valid. Indicates that the reported value(s) is (are) invalid. |
| 1h | No connection. Indicates that there are no connected devices. |
| 2h | Fingerprint. Indicates a specific fingerprint value for devices that are not specified. |
| 3h | Microphone (mono) |
| 4h | Reserved |
| 5h | Stereo Line In (CE device attached) |
| 6h | Reserved |
| 7h | Reserved |
| 8h | Reserved |
| 9h | Headset (mono speaker left channel and microphone.) |
| Ah | Other. Allows a vendor to report sensing other type of devices/peripherals. SR[5:0] together with OR[1:0] provide information regarding the type of device sensed. |
| Bh-Eh | Reserved |
| Fh | Unknown (use fingerprint) |

8.4.8. Revision Code (6Ch)

To access Register 6Ch, Page 00h must be selected in Register 24h.

Default: 00xxh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|----------|--|-----|-----|----|----|
| MINORREV | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| MAJORREV | | | | | | | |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15:8 | 00h | MINORREV | Minor Revision ID. These bits are read only and will be updated based on minor device changes which will not require software changes. | | | | |
| 7:0 | xxh | MAJORREV | Major Revision ID. These bits are read only and will be updated based on major device changes. | | | | |

8.4.9. Analog Special (6Eh)

To access Register 6Eh, Page 00h must be selected in Register 24h.

Default: 1000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|--------------------|--------------------|---|----------|-----------------|------------|-------------|
| RESERVED | | | AC97MIX | RESERVED | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RSVD | MUTEFIX DISABLE | ADCSLT1 | ADCSLT0 | RSVD | MIC GAIN VAL | SPLYOVR EN | SPLYOVR VAL |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15:13 | 0 | RESERVED | Bits not used, should read back 0 | | | | |
| 12 | 1 | AC97MIX | 0 = Mixer record contains a mix of all mono and stereo analog input signals, not the DAC (ALL ANALOG mode). 1 = Mixer record contains a mix of all mono and stereo analog input signals plus the DAC signal (AC'97 mode). This bit only has an effect when either Stereo Mix or Mono Mix is selected as the record source in Reg 1Ah. The "ALL" mode is useful in conjunction with the POP BYPASS mode (Reg 20h; D15) to record all analog sources, perform further processing in the digital domain, including combining with other PCM data, and routing through the DACs directly to Line Out, Headphone Out, or Mono Out. A Stereo Mix recording will be affected by the setting of the 3D Effects bit (Reg 20h; D13) | | | | |
| 11:7 | 0 | RESERVED | Bits not used, should read back 0 | | | | |
| 6 | 0 | MUTEFIX DISABLE | 0 = MUTE FIX Enabled 1 = MUTE FIX Disabled When this bit is zero, and either channel is set to -46.5dB attenuation (1Fh), then that channel is fully muted. When this bit is one, then operation is per AC'97 specification. | | | | |
| 5:4 | 0 | ADCSLT1:0 | Select slots for ADC data on ACLINK 00 = Left slot 3, right slot 4 01 = Left slot 7, right slot 8 10 = Left slot 6, right slot 9 11 = Left slot 10, right slot 11 | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|--------------|--|
| 3 | 0 | RESERVED | RESERVED |
| 2 | 0 | MIC GAIN VAL | Adds +10dB gain to the selected MIC input. Use in conjunction with BOOSTEN (Reg. 0Eh;D6) BOOSTEN MICGAINVAL 0 0 = 0 dB 0 1 = 10 dB 1 0 = 20 dB 1 1 = 30 dB |
| 1 | 0 | SPLYOVR_EN | Supply Override bit allows override of the supply detect. 0 = No override on supply detect 1 = Override supply detect with bit 0 |
| 0 | 0 | SPLYOVR_VAL | Supply Override Value provides the analog voltage operation values. 0 = Force 3.3 v operation 1 = Force 5 V operation |

8.4.10. Analog Current Adjust (72h)

To unlock Register 72h, write 0xABBA to Register 70h.

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|----|----|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| INT APOP | RESERVED | | | | | | |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|----------|---|
| 15:8 | 0 | Reserved | Reserved |
| 7 | 0 | INT_APOP | 0 = Anti Pop Enabled 1 = Anti Pop Disabled The STAC9752/9753 includes an internal power supply anti-pop circuit that prevents audible clicks and pops from being heard when the CODEC is powered on and off. This function is accomplished by delaying the charge/discharge of the VREF capacitor (Pin 27). A C_{VREF} value of 1 μ F will cause a turn-on delay of roughly 3 seconds, which will allow the power supplies to stabilize before the CODEC outputs are enabled. The delay will be extended to 30 seconds if a C_{VREF} value of 10 μ F is used. The CODEC outputs are also kept stable for the same amount of time at power-off to allow the system to be gracefully turned off. The Anti Pop bit allows this delay circuit to be bypassed for rapid production testing. Any external component anti-pop circuit is unaffected by the internal circuit. |
| 6:0 | 0 | Reserved | Reserved |

8.4.11. EAPD Access Register (74h)

Default: 0800h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|----------|----------|---------|-----------|
| EAPD | RESERVED | | | EAPD_OEN | RESERVED | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | INTDIS | GPIOACC | GPIOSLT12 |

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|-----------|--|
| 15 | 0 | EAPD | EAPD data Enable EAPD data is output on the EAPD pin when bit D11 = 1 EAPD data is input on the EAPD pin when bit D11 = 0 |
| 14:12 | 0 | Reserved | Bits not used, should read back 0 |
| 11 | 1 | EAPD_OEN | EAPD Pin Enable 0 = EAPD configured as input pin 1 = EAPD configured as output pin |
| 10:3 | 0 | Reserved | Bits not used, should read back 0 |
| 2 | 0 | INTDIS | Interrupt disable option. Interrupts cleared by writing a 1 to I4 (Reg24h:D15) 0 = Will clear both SENSE and GPIO interrupts 1 = Will only clear SENSE interrupts. GPIO interrupts will have to be cleared in Reg54h. |
| 1 | 0 | GPIOACC | GPIO ACCESS 0 = ACLINK access from GPIO Pads 1 = ACLINK access from GPIO Register 54h |
| 0 | 0 | GPIOSLT12 | 0 = GPIO0/1 access via Reg 54h when GPIO is set as an output, for input, Slot 12 data will be 0h. 1 = GPIO0/1 access via Slot 12 when GPIO is set as an output, for inputs, Reg54h will not be updated. This can only be used if a modem CODEC is not present in the system and using Slot 12. |

8.4.12. High Pass Filter Bypass (78h)

To unlock Register 78h, write 0xABBA to Register 76h.

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------------|-------------|--|-----|-----|----|-------------|
| RESERVED | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RESERVED | | | | | | | ADC HPF BYP |
| Bit(s) | Reset Value | Name | Description | | | | |
| 15:1 | 0 | RESERVED | Bits not used, should read back 0 | | | | |
| 0 | 0 | ADC HPF BYP | 0 = ADC High Pass Filter active, (Normal operation) 1 = ADC High Pass Filter Bypass | | | | |

8.5. Vendor ID1 and ID2 (Index 7Ch and 7Eh)

These two registers contain four 8-bit ID codes. The first three codes have been assigned by Microsoft using their Plug and Play Vendor ID methodology. The fourth code is a manufacturer assigned code identifying the STAC9752/9753. The ID1 register (index 7Ch) contains the value 8384h, which is the first (83h) and second (84h) bytes of the Microsoft ID code. The ID2 register (index 7Eh) contains the value 7652h, which is the third (76h) byte of the Microsoft ID code, and 52h which is the STAC9752/9753 ID code.

8.5.1. Vendor ID1 (7Ch)

Default: 8384h

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

8.5.2. Vendor ID2 (7Eh)

Default: 7652h

| | | | | | | | |
|-----|-----|-----|-----|-----|-----|----|----|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |

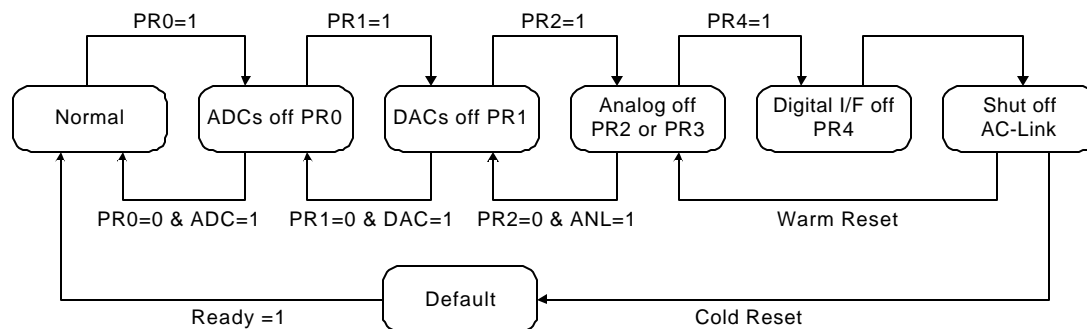
9. LOW POWER MODES

The STAC9752/9753 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. The power down options are listed in Table 27. The first three bits, PR[2:0], can be used individually or in combination with each other, and control power distribution to the ADCs, DACs and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR0, PR1, and PR2. PR3 essentially removes power from all analog sections of the CODEC, and is generally only asserted when the CODEC will not be needed for long periods. PR0 and PR1 control the PCM ADCs and DACs only. PR2 and PR3 do not need to be “set” before a PR4, but PR0 and PR1 should be “set” before PR4. PR5 disables the DSP clock and does not require an external cold reset for recovery. PR6 disables the headphone driver amplifier for additional analog power saving.

Table 27. Low Power Modes

| GRP Bits | Function |
|----------|--|
| PR0 | PCM_In ADCs & Input Mux Powerdown |
| PR1 | PCM_Out DACs Powerdown |
| PR2 | Analog Mixer powerdown (VREF still on) |
| PR3 | Analog Mixer powerdown (VREF off) |
| PR4 | Digital Interface (AC-Link) powerdown (BIT_CLK forced low) |
| PR5 | Digital Clock disable, BIT_CLK still on |
| PR6 | Powerdown HEADPHONE_OUT |

Figure 22. Example of STAC9752/9753 Powerdown/Powerup flow



The Figure 22 illustrates one example procedure to do a complete powerdown of STAC9752/9753. From normal operation, sequential writes to the Powerdown Register are performed to power down STAC9752/9753 a section at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-Link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-Link (resetting PR4 to zero). The STAC9752/9753 can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states (Paged Registers are semi-exempt). When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

Figure 23. Powerdown/Powerup flow with analog still alive

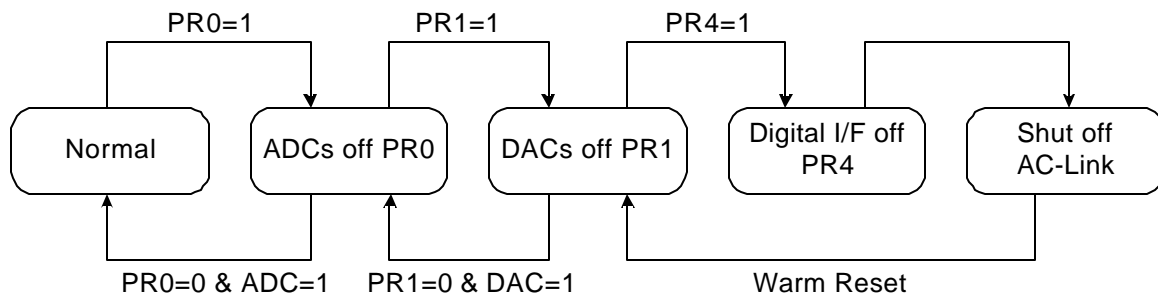


Figure 23 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through STAC9752/9753 to the speakers, while most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

10. MULTIPLE CODEC SUPPORT

The STAC9752/9753 provides support for the multi-CODEC option according to the Intel AC'97, rev 2.3 specification. By definition, there can be only one Primary CODEC (CODEC ID 00) and up to three Secondary CODECs (CODEC IDs 01, 10, and 11). The CODEC ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

10.1. Primary/Secondary CODEC Selection

In a multi-CODEC environment the CODEC ID is provided by external programming of pins 45 and 46 (CID0 and CID1). The CID pin electrical function is logically inverted from the CODEC ID designation. The corresponding pin state and its associated CODEC ID are listed in the "CODEC ID Selection" table.

Table 28. CODEC ID Selection

| CID1 State | CID0 State | CODEC ID | CODEC Status |
|------------------|------------------|----------|--------------|
| Dvdd or floating | Dvdd or floating | 00 | Primary |
| Dvdd or floating | 0 V | 01 | Secondary |
| 0 V | Dvdd or floating | 10 | Secondary |
| 0 V | 0 V | 11 | Secondary |

10.1.1. Primary CODEC Operation

As a Primary device, the STAC9752/9753 is completely compatible with existing AC'97 definitions and extensions. Primary CODEC registers are accessed exactly as defined in the AC'97 Component Specification and AC'97 Extensions. The STAC9752/9753 operates as Primary by default, and the external ID pins (45 and 46), have internal pull-ups so that these pins may be left as no-connects for operation as a primary.

When used as the Primary CODEC, the STAC9752/9753 generates the master AC-Link BIT_CLK for both the AC'97 Digital Controller and any Secondary CODECs. The STAC9752/9753 can support up to four loads of 10 K Ω and 50 pF on the BIT_CLK output. This is to ensure that up to four CODEC implementations will not load down the clock output.

10.1.2. Secondary CODEC Operation

When the STAC9752/9753 is configured as a Secondary device the BIT_CLK pin is configured as an input at power up. Using the BIT_CLK provided by the Primary CODEC insures that everything on the AC-Link will be synchronous. As a Secondary device it can be defined as CODEC ID 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

10.2. Secondary CODEC Register Access Definitions

The AC'97 Digital Controller can independently access Primary and Secondary CODEC registers by using a 2-bit CODEC ID field (chip select) which is defined as the LSBs of Output Slot 0. For Secondary CODEC access, the AC'97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the CODEC ID field (Slot 0, bits 1 and 0).

As a Secondary CODEC, the STAC9752/9753 will disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when it sees a 2-bit CODEC ID value (Slot 0, bits 1 and 0) that matches its configuration. In a sense the Secondary CODEC ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary CODECs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary CODEC ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary CODEC ID bits are set.

This method is designed to be backward compatible with existing AC'97 controllers and CODECs. There is no change to output Slot 1 or 2 definitions.

Table 29. Secondary CODEC Register Access Slot 0 Bit Definitions

| Output Tag Slot (16-bits) | |
|---------------------------|--|
| Bit | Description |
| 15 | Frame Valid |
| 14 | Slot 1 Valid Command Address bit (†Primary CODEC only) |
| 13 | Slot 2 Valid Command Data bit (†Primary CODEC only) |
| 12-3 | Slot 3-12 Valid bits as defined by AC'97 |
| 2 | Reserved (Set to 0) |
| †1-0 | 2-bit CODEC ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary) |

Note: † New definitions for Secondary CODEC Register Access

Using three CODECs typically requires a controller to support SDATA_IN2.

11. TESTABILITY

The STAC9752/9753 has two test modes. One is for ATE in-circuit test and the other is restricted for manufacturer's internal use. The STAC9752/9753 enters the ATE in-circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-Link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. Use of the ATE test mode is the recommended means of removing the CODEC from the AC-Link when another CODEC is to be used as the primary. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the STAC9752/9753 must be issued another RESET# with all AC-Link signals held low to return to the normal operating mode.

Table 30. Test Mode Activation

| SYNC | SDATA_OUT | Description |
|------|-----------|------------------------|
| 0 | 0 | Normal AC'97 operation |
| 0 | 1 | ATE Test Mode |
| 1 | 0 | IDT Internal Test Mode |
| 1 | 1 | Reserved |

11.0.1. ATE Test Mode

ATE test mode allows for in-circuit testing to be completed at the board level. For this to work, the outputs of the device must be driven to a high impedance state (Z). Internal pullups for digital I/O pins must be disabled in this mode. This mode initiates on the rising edge of RESET# pin. Only a cold reset will exit the ATE Test Mode.

Table 31. ATE Test Mode Operation

| Pin Name | Pin # | Function | Description |
|-----------|-------|----------|--|
| SDATA_OUT | 5 | 1 | Must be held high at the rising edge of RESET# |
| BIT_CLK | 6 | Z | |
| SDATA_IN | 8 | Z | |
| SYNC | 10 | 0 | Must be held low at rising edge of RESET# |
| RESET# | 11 | 1 | |
| N.C. | 31 | Z | Always an input |
| N.C. | 33 | Z | Always an input |
| N.C. | 34 | Z | Always an input |
| GPIO0 | 43 | Z | |
| GPIO1 | 44 | Z | |
| CID0 | 45 | Z | |
| CID1 | 46 | Z | |
| EAPD | 47 | Z | |
| SPDIF | 48 | Z | |

Note: Pins 31, 33, and 34 are NO CONNECTS.

12. PIN DESCRIPTION

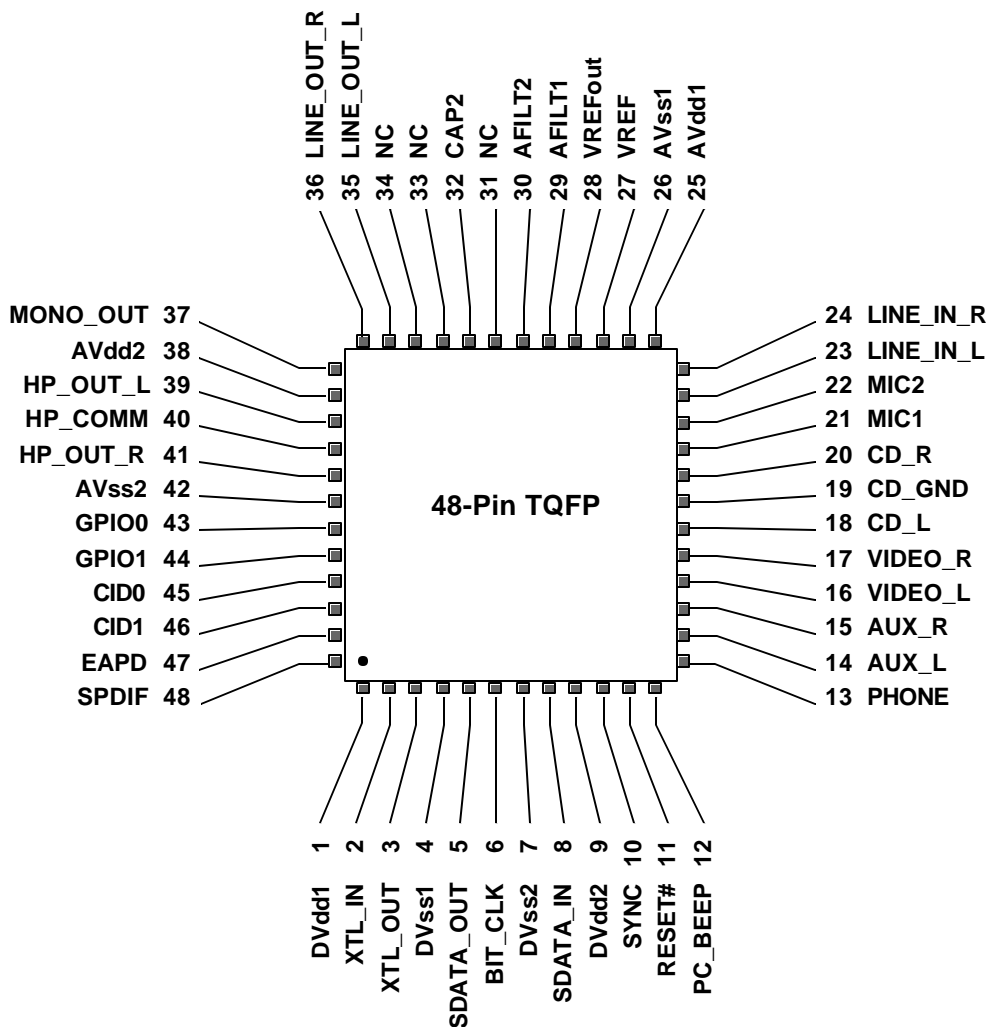


Figure 24. Pin Description Drawing

Pin 48: To Enable SPDIF, use a 1 K Ω -10 K Ω external pulldown. To Disable SPDIF, use a 1 K Ω -10 K Ω external pullup. Do NOT leave Pin 48 floating.

The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause serious distortion. If there is no analog CD input, then this pin can be No-Connect.

12.1. Digital I/O

These signals connect the STAC9752/9753 to its AC'97 controller counterpart, an external crystal, multi-CODEC selection and external audio amplifier.

Table 32. Digital Connection Signals

| Pin Name | Pin # | Type | Description |
|-----------|-------|------|---|
| XTL_IN | 2 | I | 24.576 MHz Crystal or External Clock Source |
| XTL_OUT | 3 | I/O | 24.576 MHz Crystal |
| SDATA_OUT | 5 | I | Serial, time division multiplexed, AC'97 input stream |
| BIT_CLK | 6 | I/O | 12.288 MHz serial data clock |
| SDATA_IN | 8 | O | Serial, time division multiplexed, AC'97 output stream |
| SYNC | 10 | I | 48 KHz fixed rate sample sync |
| RESET# | 11 | I | AC'97 Master H/W Reset |
| N.C. | 31 | I | IDT Internal Test mode only. |
| N.C. | 33 | I | IDT Internal Test mode only |
| N.C. | 34 | I/O | IDT Internal Test mode only |
| GPIO0 | 43 | I/O | General Purpose I/O |
| GPIO1 | 44 | I/O | General Purpose I/O |
| CID0 | 45 | I | Multi-CODEC ID select – bit 0 |
| CID1 | 46 | I | Multi-CODEC ID select – bit 1 |
| EAPD | 47 | I/O | External Amplifier Power Down/GPIO |
| SPDIF | 48 | I/O | SPDIF digital output Pin 48: To Enable SPDIF, use an 1 K Ω - 10 K Ω external pulldown. To Disable SPDIF, use an 1 K Ω - 10K Ω external pullup. Do NOT leave Pin 48 floating. |

Note: Pins 31, 33, and 34 are NO CONNECTS.

12.2. Analog I/O

These signals connect the STAC9752/9753 to analog sources and sinks, including microphones and speakers.

Table 33. Analog Connection Signals

| Pin Name | Pin # | Type | Description |
|---------------------|-------|------|--|
| PC_BEEP | 12 | I* | PC Speaker beep pass-through |
| PHONE | 13 | I* | From telephony subsystem speakerphone |
| AUX_L | 14 | I* | Aux Left Channel |
| AUX_R | 15 | I* | Aux Right Channel |
| VIDEO_L | 16 | I* | Video Audio Left Channel |
| VIDEO_R | 17 | I* | Video Audio Right Channel |
| CD_L | 18 | I* | CD Audio Left Channel |
| CD_GND [†] | 19 | I* | CD Audio analog signal return (Do NOT ground. See note. [†]) |
| CD_R | 20 | I* | CD Audio Right Channel |
| MIC1 | 21 | I* | Desktop Microphone Input |
| MIC2 | 22 | I* | Second Microphone Input |
| LINE_IN_L | 23 | I* | Line In Left Channel |
| LINE_IN_R | 24 | I* | Line In Right Channel |
| LINE_OUT_L | 35 | O | Line Out Left Channel |
| LINE_OUT_R | 36 | O | Line Out Right Channel |
| MONO_OUT | 37 | O | To telephony subsystem speakerphone |
| HP_OUT_L | 39 | O | Headphone Out Left Channel |
| HP_COMM | 40 | O | Headphone Ground Return |
| HP_OUT_R | 41 | O | Headphone Out Right Channel |

Note: * Unused input pins should be tied together and connected to ground through a capacitor (0.1 μ F suggested), except the MIC inputs which should have a separate capacitor to ground.

Note: [†] The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause serious distortion. If there is no analog CD input, then this pin can be No-Connect.

12.3. Filter/References

These signals are connected to resistors, capacitors, or specific voltages.

Table 34. Filtering and Voltage References

| Signal Name | Pin Number | Type | Description |
|-------------|------------|------|---|
| VREF | 27 | O | Analog ground ($0.45 * V_{dd}$, at 5 V; or $0.41 * V_{dd}$ at 3 V) |
| VREFOUT | 28 | O | Reference Voltage out 5 mA drive (intended for microphone bias) ($\sim V_{dd}/2$) |
| AFILT1 | 29 | O | Anti-Aliasing Filter Cap - ADC left channel |
| AFILT2 | 30 | O | Anti-Aliasing Filter Cap - ADC right channel |
| CAP2 | 32 | O | ADC reference Cap |

12.4. Power and Ground Signals

Table 35. Power and Ground Signals

| Pin Name | Pin # | Type | Description |
|----------|-------|------|-----------------------------|
| AVdd1 | 25 | I | Analog Vdd = 5.0 V or 3.3 V |
| AVdd2 | 38 | I | Analog Vdd = 5.0 V or 3.3 V |
| AVss1 | 26 | I | Analog Gnd |
| AVss2 | 42 | I | Analog Gnd |
| DVdd1 | 1 | I | Digital Vdd = 3.3 V |
| DVdd2 | 9 | I | Digital Vdd = 3.3 V |
| DVss1 | 4 | I | Digital Gnd |
| DVss2 | 7 | I | Digital Gnd |

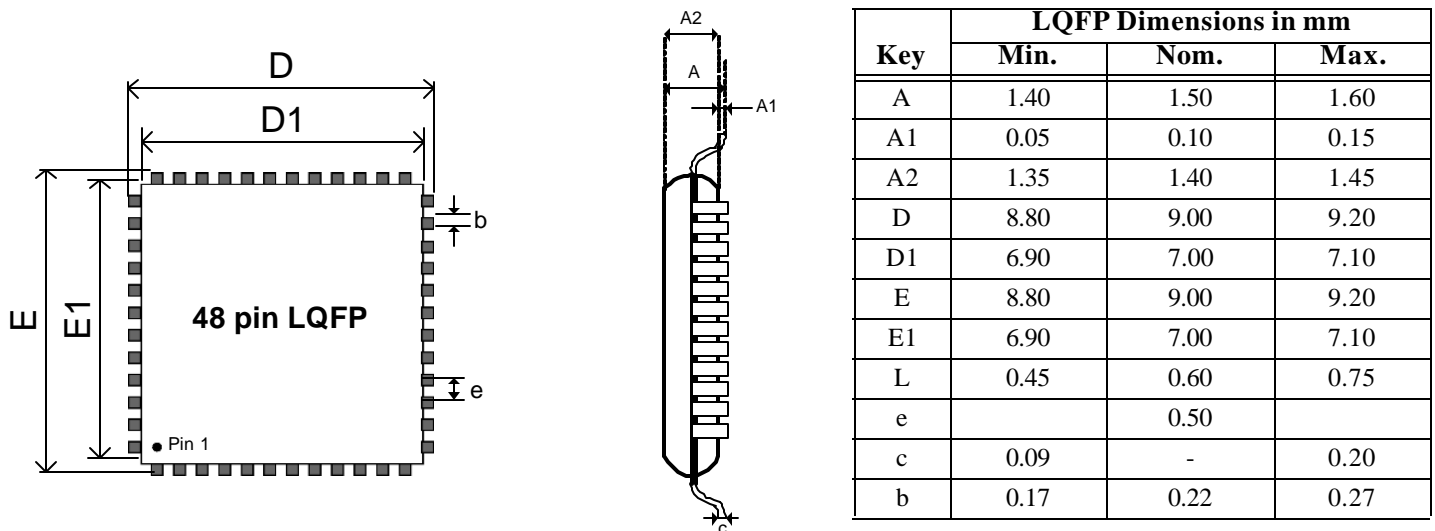
13. ORDERING INFORMATION

| Part Number | Package | Temp Range | Supply Range |
|------------------|-----------------------------------|----------------|--------------------------|
| STAC9752XXTAEyyX | 48-pin RoHS QFP 7mm x 7mm x 1.4mm | 0° C to +70° C | DVdd = 3.3V, AVdd = 5.0V |
| STAC9753XXTAEyyX | 48-pin RoHS QFP 7mm x 7mm x 1.4mm | 0° C to +70° C | DVdd = 3.3V, AVdd = 3.3V |

yy = 2 digit revision. Contact Sales for complete ordering number.

Add an "R" to the end of the Part number for Tape and Reel delivery. Minimum order quantity is 2ku.

14. PACKAGE DRAWING



15. SOLDER REFLOW PROFILE

15.1. Standard Reflow Profile Data

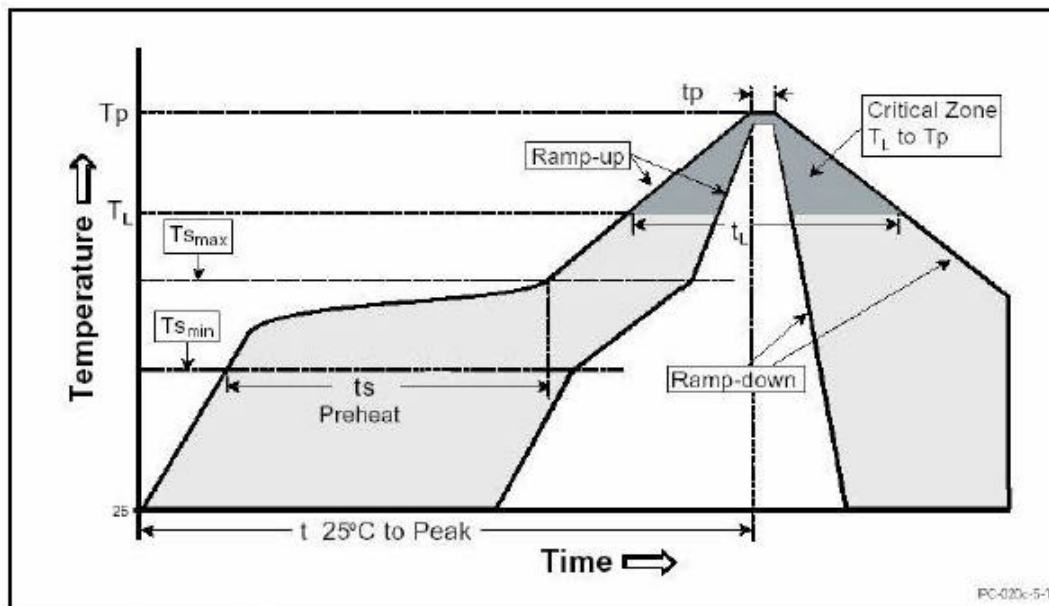
Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

| Profile Feature | Pb Free Assembly |
|---|--|
| Average Ramp-Up Rate ($T_{s_{max}} - T_p$) | 3 °C / second max |
| Preheat Temperature Min ($T_{s_{min}}$) Temperature Max ($T_{s_{max}}$) Time ($t_{s_{min}} - t_{s_{max}}$) | 150 °C 200 °C 60 - 180 seconds |
| Time maintained above Temperature (T_L) Time (t_L) | 217 °C 60 - 150 seconds |
| Peak / Classification Temperature (T_p) | See "Package Classification Reflow Temperatures" on page 91. |
| Time within 5 °C of actual Peak Temperature (t_p) | 20 - 40 seconds |
| Ramp-Down rate | 6 °C / second max |
| Time 25 °C to Peak Temperature | 8 minutes max |

Note: All temperatures refer to topside of the package, measured on the package body surface.

Figure 25. Reflow Profile



15.2. Pb Free Process - Package Classification Reflow Temperatures

| Package Type | MSL | Reflow Temperature |
|--------------|-----|--------------------|
| TQFP 48-pin | 3 | 260 °C* |

16. APPENDIX A: PROGRAMMING REGISTERS

| Reg # | Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | |
|-----------------|-------------------------------|----------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-------|-------|----------|----------|-------------|-------------|---------|-------|
| 00h | Reset | RSRVD | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | 6A90h | |
| 02h | Master Volume | Mute | RSRVD | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | RESERVED | | | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h |
| 04h | HP_OUT Mixer Volume | Mute | RSRVD | HPL5 | HPL4 | HPL3 | HPL2 | HPL1 | HPL0 | RESERVED | | | HPR5 | HPR4 | HPR3 | HPR2 | HPR1 | HPR0 | 8000h |
| 06h | Master Volume Mono | Mute | RESERVED | | | | | | | | | MM5 | MM4 | MM3 | MM2 | MM1 | MM0 | 8000h | |
| 0Ah | PC_BEEP Volume | Mute | X | X | F7 | F6 | F5 | F | F3 | F2 | F1 | F0 | PV3 | PV2 | PV1 | PV0 | RSRVD | 0000h | |
| 0Ch | Phone volume | Mute | RESERVED | | | | | | | | | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h | | |
| 0Eh | Mic Volume | Mute | RESERVED | | | | | | | | boosten | RSVD | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h | |
| 10h | Line In Volume | Mute | RESERVED | GL4 | GL3 | GL2 | GL1 | GL0 | RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | | |
| 12h | CD Volume | Mute | RESERVED | GL4 | GL3 | GL2 | GL1 | GL0 | RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | | |
| 14h | Video Volume | Mute | RESERVED | GL4 | GL3 | GL2 | GL1 | GL0 | RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | | |
| 16h | AUX Volume | Mute | RESERVED | GL4 | GL3 | GL2 | GL1 | GL0 | RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | | |
| 18h | PCM Out Volume | Mute | RESERVED | GL4 | GL3 | GL2 | GL1 | GL0 | RESERVED | | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | | |
| 1Ah | Record Select | RESERVED | | | | | SL2 | SL1 | SL0 | RESERVED | | | | | SR2 | SR1 | SR0 | 0000h | |
| 1Ch | Record Gain | Mute | RESERVED | | | GL3 | GL2 | GL1 | GL0 | RESERVED | | | | GR3 | GR2 | GR1 | GR0 | 8000h | |
| 20h | General Purpose | POP BYP | RSRVD | 3D | RESERVED | | | MIX | MS | LPBK | RESERVED | | | | | | | 0000h | |
| 22h | 3D Control | RESERVED | | | | | | | | | | | DP3 | DP2 | RESERVED | | 0000h | | |
| 24h | Audio Int. & Paging | I4 | I3 | I2 | I1 | I0 | RESERVED | | | | | | PG3 | PG2 | PG1 | PG0 | 0000h | | |
| 26h | Powerdown Ctrl/Stat | EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | RESERVED | | | | REF | ANL | DAC | ADC | 000Fh | |
| 28h | Extended Audio ID | ID1 | ID0 | RESERVED | | REV1 | REV0 | AMAP | LDAC | SDAC | CDAC | DSA1 | DSA0 | RSVD | SPDIF | DRA | VRA | 0A05h | |
| 2Ah | Extended Audio Control/Status | VCFG | PRL/RSVD | PRK/RSVD | PRJ/RSVD | PRI/RSVD | SPCV | MADC/RSVD | LDAC/RSVD | SDAC/RSVD | CDAC/RSVD | SPSA1 | SPSA0 | VRM/RSVD | SPDIF | DRA/RSVD | VRA | 0400h* | |
| 2Ch | PCM DAC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h | |
| 32h | PCM LR ADC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h | |
| 3Ah | SPDIF Control | V | DRS | SPSR1 | SPSR2 | L | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | PRE | COPY | #PCM/AUDIO | PRO | 2000h | |
| 3Eh | Extended Modern Status | RESERVED | | | | | | | PRA | RESERVED | | | | | | | GPIO | 0100h | |
| 4Ch | GPIO Pin Config | RESERVED | | | | | | | | | | | | | | GC1 (GPIO1) | GC0 (GPIO0) | 0300h | |
| 4Eh | GPIO Pin Polarity/Type | RESERVED | | | | | | | | | | | | | | GP1 (GPIO1) | GP0 (GPIO0) | FFFFh | |
| 50h | GPIO Pin Sticky | RESERVED | | | | | | | | | | | | | | GS1 (GPIO1) | GS0 (GPIO0) | 0000h | |
| 52h | GPIO Pin Mask | RESERVED | | | | | | | | | | | | | | GW1 (GPIO1) | GW0 (GPIO0) | 0000h | |
| 54h | GPIO Pin Status | RESERVED | | | | | | | | | | | | | | G11 (GPIO1) | G10 (GPIO0) | 0000h | |
| 60h Page 01h | CODEC Class/Rev | RESERVED | | | CL4 | CL3 | CL2 | CL1 | CL0 | RV7 | RV6 | RV5 | RV4 | RV3 | RV2 | RV1 | RV0 | 12xxh | |
| 62h | VENDOR RESERVED | | | | | | | | | | | | | | | | | | |
| 62h Page 01h | PCI SVID | PV15 | PV14 | PV13 | PV12 | PV11 | PV10 | PV9 | PV8 | PV7 | PV6 | PV5 | PV4 | PV3 | PV2 | PV1 | PV0 | FFFFh | |
| 64h | VENDOR RESERVED | | | | | | | | | | | | | | | | | | |
| 64h Page 01h | PCI SID | PI15 | PI14 | PI13 | PI12 | PI11 | PI10 | PI9 | PI8 | PI7 | PI6 | PI5 | PI4 | PI3 | PI2 | PI1 | PI0 | FFFFh | |
| 66h | VENDOR RESERVED | | | | | | | | | | | | | | | | | | |
| 66h Page 01h | Function Select | RESERVED | | | | | | | | | | | FC3 | FC2 | FC1 | FC0 | T/R | 0000h | |
| 68h | VENDOR RESERVED | | | | | | | | | | | | | | | | | | |
| 68h Page 01h | Function Information | G4 | G3 | G2 | G1 | G0 | INV | DL4 | DL3 | DL2 | DL1 | DL0 | IV | RESERVED | | | FIP | xxxxh | |
| 6Ah | Digital Audio Control | RESERVED | | | | | | | | | | | | | SPOR | DO1 | RSVD | 0000h | |
| 6Ah Page 01h | Sense Details | ST2 | ST1 | ST0 | S4 | S3 | S2 | S1 | S0 | OR1 | OR0 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | NA | |
| 6Ch | Revision Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | x | 00xxh |

| Reg # | Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default | | |
|--------------------|-------------------------|----------|----------|-----|--------------------|--------------|----------|----|-------------|------------------------|--------------|--------------|--------|-------------------|----------------|-----------------|----------------|---------|-------|-------|
| 6Ch Page 01h | RESERVED | | | | | | | | | | | | | | | | | | | |
| 6Eh | Analog Special | RESERVED | | | AC97 ALL MIX | RESERVED | | | | MUTE FIX DISABLE | ADC slot1 | ADC slot0 | RSVD | MIC GAIN VALUE | SPLY OVR EN | SPLY OVR VAL | 1000h | | | |
| 6Eh Page 01h | RESERVED | | | | | | | | | | | | | | | | | | | |
| 70h | VENDOR RESERVED | | | | | | | | | | | | | | | | | | 0000h | |
| 72h | Analog Current Adjust | RESERVED | | | | | | | INT APOP | RESERVED | | | | | | | | | | 0000h |
| 74h | EAPD Access | EAPD | RESERVED | | | EAPD_ OEN | RESERVED | | | | | | INTDIS | GPIO ACC | GPIO SLT12 | 0800h | | | | |
| 76h | VENDOR RESERVED | | | | | | | | | | | | | | | | | | 0000h | |
| 78h | High Pass Filter Bypass | RESERVED | | | | | | | | | | | | | | | ADC HPF BYP | 0000h | | |
| 7Ah | Reserved | RESERVED | | | | | | | | | | | | | | | | | | 0000h |
| 7Ch | Vendor ID1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8384h | | |
| 7Eh | Vendor ID2 9752 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 7652h | | |

*depends upon chip ID

17. REVISION HISTORY

| Revision | Date | Description of Change |
|----------|----------------|--|
| 3.2 | October 2003 | <ul style="list-style-type: none"> -Removed "Preliminary" tag on front page. -Removed BIT_CLK as an input option from clocking table, it was incorrectly included in 3.1 version. -Added CD_GND elaboration note on connection diagram, pin list and pin out diagrams: "The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5 V. The name of the pin in the AC'97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause serious distortion. If there is no analog CD input, then this pin can be No-Connect. " |
| 3.2 | 3 October 2006 | Release in IDT format. |
| 3.3 | December 2006 | Updated part ordering information to longer orderable part number related to previously issued PCN. |

STAC9752/9753

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