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**Structure** Silicon Monolithic Integrated Circuit

**Product Name** IrDA Controller LSI built-in Ir remote control

**Model name** **BU92747GUW**

**Outer Dimension** Figure 1 Outer Dimensions

**Features**
- Data transfer speed (bps)
  IrDA SIR: 2.4kbps, 9.6kbps, 19.2kbps, 38.4kbps, 57.6kbps and 115.2kbps
  IrDA MIR: 0.576Mbps, 1.152Mbps
  IrDA FIR: 4Mbps
  IrSimple
- Interface
  16-bit data bus , Address $A_{0-3}$
- Built-in 2560 × 2byte FIFO buffer (for transmission and reception)
- Accessible as a memory device connected to the bus
- Power down mode setting possible for transmission and reception
- Input clock of 48MHz for external input clock and crystal input clock
- Ir remote control function
  Serial 2-lines SDA, and SCL

*This LSI chip is not subject to radiation-proof design.

**●Absolute Maximum Rating**

Ta=25°C unless otherwise stated

| Item | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Supply voltage[*1] | $V_{DD}$ | -0.3 | 2.5 | V |
| Interface supply voltage1[*1] | $V_{IO1}$ | -0.3 | 4.5 | V |
| Interface supply voltage2[*1] | $V_{IO2}$ | -0.3 | 4.5 | V |
| Input voltage[*1] | $V_{IN}$ | -0.3 | $V_{IO1, 2}$+0.3 | V |
| Power dissipation[*2] | Pd | - | 800 | mW |
| Operating temperature range | $T_{OPR}$ | -40 | 85 | °C |
| Storage temperature range | $T_{STG}$ | -55 | 125 | °C |

*1 It applies to all pins based on the GND pin.
*2 measured value with conformity substrate to SEMI (114.3mm×76.2mm×1.6mm、4layer)
8.0mW/℃ decrease over Ta=25℃ use

**●Operation Range**

| Item | Symbol | Minimum | Standard | Maximum | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 1.62 | 1.8 | 1.98 | V |
| Interface supply voltage1 | $V_{IO1}$ | 1.62 | 1.8 | 3.6 | V |
| Interface supply voltage2[*3] | $V_{IO2}$ | 1.62 | 1.8 | 3.6 | V |

*3 $V_{IO2}$ is connected with XIN/CLK48M, XOUT, $\overline{\text{PWDN}}$, $\overline{\text{NIRQ}}$ and $\overline{\text{RESET}}$.

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

## ●Electrical Characteristics (DC Characteristics)

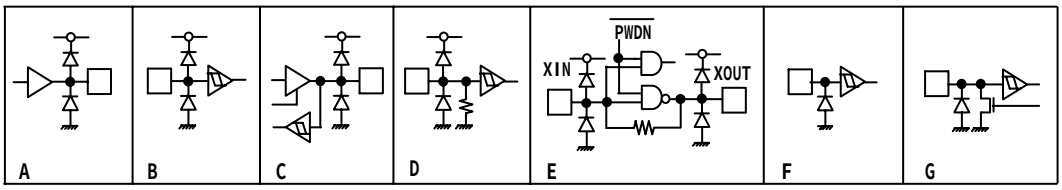
Ta=25°C, $V_{DD}$=1.8V, $V_{IO1}$=1.8V, $V_{IO2}$=1.8V and GND=0V unless otherwise stated

| Item | Symbol | Standard value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | |
| Dissipation current 1 | $I_{DD}1$ | - | 0.1 | 10 | μA | For input with no output load = 0V |
| Dissipation current 2 | $I_{DD}2$ | - | 10 | 30 | mA | For XIN = 48MHz |
| Digital high-level input voltage | $V_{IH}$ | $0.75 \times V_{IO}$ | - | - | V | |
| Digital low-level input voltage | $V_{IL}$ | - | - | $0.25 \times V_{IO}$ | V | |
| Digital high-level input current | $I_{IH}$ | - | - | 10 | μA | Input voltage level 1.8V |
| | | - | - | 100 | μA | Input voltage level 1.8V TEST1-3 |
| Digital low-level input current | $I_{IL}$ | - | - | 10 | μA | Input voltage level GND |
| Digital high-level output voltage | $V_{OH}$ | $V_{IO}$-0.6 | - | - | V | $\overline{INTR}$, $D_{0-15}$, IrDAPWDOWN, IrTX, IrRC, $\overline{NIRQ}$, CTLA IOH=-1mA |
| Digital low-level output voltage | $V_{OL}$ | - | - | 0.6 | V | $\overline{INTR}$, $D_{0-15}$, IrDAPWDOWN, IrTX, IrRC, SDA, $\overline{NIRQ}$, CTLA IOL=1mA |

## ●Pin Description

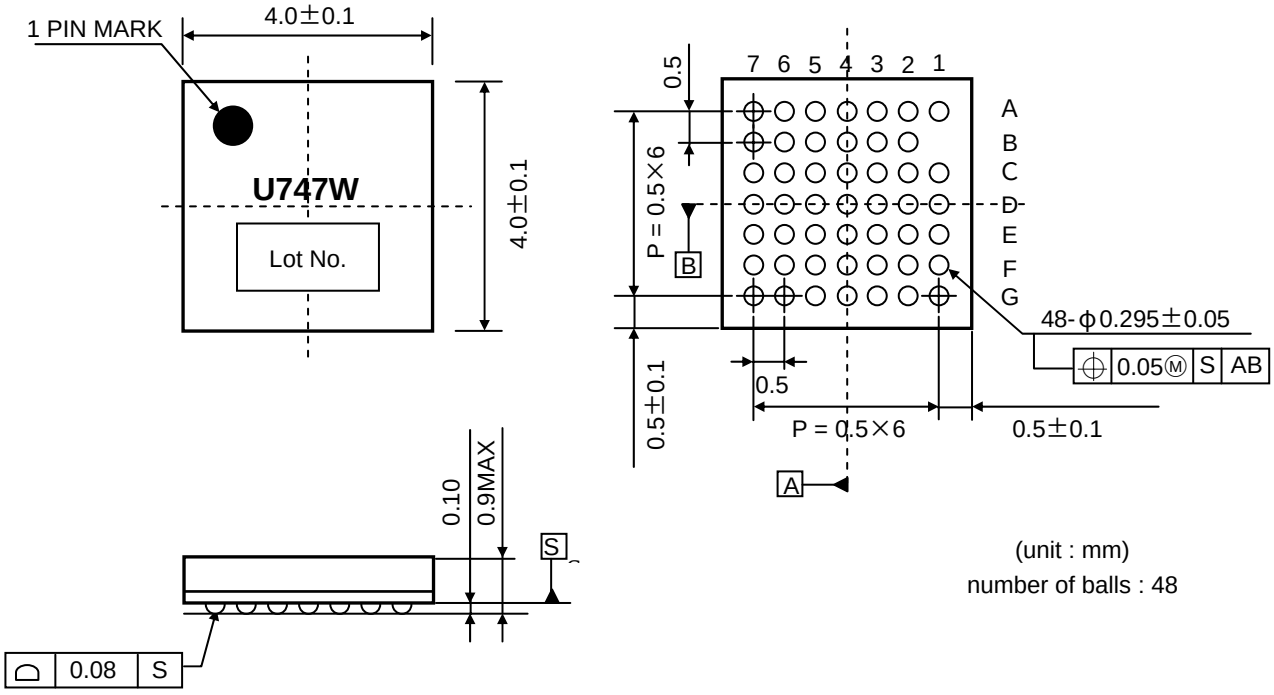
| Pin name | I / O | Condition of after reset | Pin Function | Circuit Diagram |
|---|---|---|---|---|
| IrRX | I | - | IrDA Receive Input Pin | B |
| EXTIR | I | - | Signal Input Pin in SM2="H" (Input Signal is outputted to IrTX or IrRC) | B |
| IrTX | O | L | IrDA and remote control Transmission Output Pin<br>Transmission IrDA when RC_EN= "L"<br>Transmission remote control when RC_EN="H", RC_MODE="H" | A |
| $D_{0-15}$ | I / O | Input | Data I/O Pin | C |
| $A_{0-3}$ | I | - | Address Input Pin | B |
| $\overline{CS}$ | I | - | Chip Select Pin. Low (L) Active<br>The read/write signal goes “Active” in a Low period. | B |
| $\overline{RD}$ | I | - | Read Signal Input Pin. Low (L) Active | B |
| $\overline{WR}$ | I | - | Write Signal Input Pin. Low (L) Active | B |
| $\overline{INTR}$ | O | H | CPU Interrupt Request Output Pin (IrDA controller)<br>The signal goes “Low” when an interrupt condition takes place. | A |
| $\overline{RESET}$ | I | - | Reset Input Pin. Low (L) Active<br>The signal causes the internal register settings, etc. to be initialized. | B |
| $\overline{PWDN}$ | I | - | Power Down Mode Setting. Low (L) Active<br>When set to Low (L), this signal causes the wait status and sets the low dissipation current mode. After the power down mode is removed, RESET=L must set to Low until crystal clock oscillation becomes stable (about 2 or 3 ms). After that $\overline{RESET}$ must set to High.<br>Take it into consideration that this period depends on the crystal in use. | B |
| IrRC | O | L | Remote control transmission Output pin<br>Transmission remote control when RC_EN= "H", RC_MODE= "L" | A |
| CTLA | O | L | Control Signal Output Pin | A |
| SCL | I | - | Serial clock | F |
| SDA | I/O | Input | Serial data I/O Pin | G |
| $\overline{NIRQ}$ | O | H | CPU Interrupt Request Output Pin (Ir remote control)<br>The signal goes “Low” when an interrupt condition takes place. | A |
| XIN/CLK48M | I | - | Crystal IN / External CLK Input | E |
| XOUT | O | - | Crystal OUT (N.C when external input clock is used) | E |
| TEST1-3 | I | - | Test pins (These pins must be GND during normal operation.) | D |
| IrDA PWDOWN | O | H | IrDA module control signal output pin<br>These pins must be OPEN for IrDA modules having no power-down pin. | A |
| $V_{DD}$ | - | - | Power supply pin | - |
| $V_{IO1}$ | - | - | Interface power supply voltage1 | - |
| $V_{IO2}$ | - | - | Interface power supply voltage2 | - |
| GND | - | - | Ground pin | - |

## ●Equivalent Circuit Diagram




## ●Outer Dimensions

Figure1 Outer Dimensions(VBGA048W040)




(unit : mm)
number of balls : 48

VBGA048W040 Land Matrix Table

| Land Matrix No. | Pin Name | Land Matrix No. | Pin Name | Land Matrix No. | Pin Name | Land Matrix No. | Pin Name |
|---|---|---|---|---|---|---|---|
| A1 | $\overline{PWDN}$ | C1 | $V_{IO2}$ | E1 | $A_2$ | G1 | GND |
| A2 | XOUT | C2 | $\overline{NIRQ}$ | E2 | $A_1$ | G2 | $D_5$ |
| A3 | SCL | C3 | $\overline{RESET}$ | E3 | $A_0$ | G3 | $D_4$ |
| A4 | IrRC | C4 | (NC) | E4 | $D_{15}$ | G4 | $D_3$ |
| A5 | IrTX | C5 | EXTIR | E5 | $D_{14}$ | G5 | $D_2$ |
| A6 | IrRX | C6 | $V_{IO1}$ | E6 | $D_{13}$ | G6 | $D_1$ |
| A7 | GND | C7 | $\overline{RD}$ | E7 | $D_{12}$ | G7 | $D_0$ |
| (NC) | (NC) | D1 | $V_{IO1}$ | F1 | $D_{11}$ | | |
| B2 | XIN | D2 | $A_3$ | F2 | $V_{DD}$ | | |
| B3 | SDA | D3 | TEST1 | F3 | $D_{10}$ | | |
| B4 | CTLA | D4 | TEST2 | F4 | $D_9$ | | |
| B5 | IrDAPWDN | D5 | TEST3 | F5 | $D_8$ | | |
| B6 | $V_{DD}$ | D6 | $\overline{INTR}$ | F6 | $D_7$ | | |
| B7 | $\overline{WR}$ | D7 | $\overline{CS}$ | F7 | $D_6$ | | |

**●Notes for use**

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Mutual impedance

Use short and wide wiring tracks for the power supply and ground to keep the mutual impedance as small as possible .Use a capacitor to keep ripple to a minimum.

(3) GND potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Short circuit mode between terminals and wrong mounting

In order to mount the IC on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can destroy the IC. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the IC can destroy

(5) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(7) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

(8) When power is first supplied the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously.
Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

(9) For ICs with more than one power, it is possible than rush current many flow instantaneously due to the internal powering sequence and delays.
Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

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