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USB2.0 High Speed (HS) On-the-Go (OTG) Dual Role Controller

FEATURES

- **USB 2.0 HS OTG Dual Role Controller Core**
 - Act as a USB 2.0 HS Peripheral
 - Act as a USB 2.0 HS Embedded Host Controller
 - Act as a USB 2.0 HS OTG Device
 - Supports Session Request Protocol (SRP)
 - Supports Host Negotiation Protocol (HNP)
- **Integrated USB 2.0 OTG PHY**
- **NOR FLASH - Like External Host Interface**
- **Configurable for up to 15 transmit endpoints and up to 15 receive endpoints**
 - 16 kilobyte RAM for USB endpoint FIFO shared by USB IN/OUT endpoints
 - Configurable FIFOs, including the option of dynamic FIFO sizing
 - Support for external DMA access to FIFOs
- **Power Management Module**
 - Ultra low power Idle mode for battery conscious applications
 - Support for External Charge Pump
- **TUSB6010BZQE/TUSB6010BIZQE are RoHS compliant.**
- **80 Terminal BGA Microstar Junior Package**

DESCRIPTION

The TUSB6010B is a USB 2.0 HS Dual Role USB Controller designed for seamless interface to an external Host processor through the NOR FLASH-like interface. The TUSB6010B can be used to enable the processor to implement any one of three general types of USB devices. It can be implemented as a USB high-speed peripheral (or target), as a USB high-speed, single-port, embedded host controller, or as a USB high-speed OTG device. Software on the application processor will be required to implement the chosen type of USB device.

The NOR FLASH-like interface is a multiplexed, 16-bit interface with support for burst and single read/write access. It can operate in both synchronous and asynchronous modes.

The Power Management Module provides external USB OTG Charge Pump control through the power control/status interface. The Power Management Module provides a seamless interface to the TPS65030 Power Management IC for USB-OTG.

The device also has eight user configurable general purpose I/O interface pins. The GPIO can be configured as an interrupt or wakeup source. Some GPIO have secondary NOR-flash DMA Request functionality.

The device is fully compliant with the Universal Serial Bus Specification Rev. 2.0 and On-The-Go Supplement to the USB Specification Rev. 1.3.

The ESD protection level is 2KV HBM (JESD22-A114D), 500V CDM (JESD22-C101C).

NOTE:

This product is intended for high-volume handset applications only. Contact support@ti.com for more information.

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Device Power States

TUSB6010 has three device states typically entered under normal operation:

- RESET
- IDLE
- NORMAL (ACTIVE)

RESET State

The device shall be in RESET state when the RSTn input signal is driven low. In the RESET state:

- All output ports are tri-stated or initialized to inactive state
- All bi-directional ports are configured as Inputs
- All registers are set to their reset value
- PHY Macro is enabled and its reference clock output is active

Device always enters RESET state asynchronously, but exit the state synchronously. System reset de-assertion is always synchronized with active system clock. Upon asserted system reset, device requires active system clock to exit RESET state.

IDLE State

Device enters the IDLE state when External Host sets DevIdle bit in the Device Power Management register. In the IDLE State, the device power consumption should not exceed 100 μ A, including companion Power Management device (TPS65030).

In IDLE state:

- All output signals are driven to state with minimum IO current leakage (pull-up/pull-downs are controllable through Pull-up/Pull-Down Control registers)
- All controllable bi-directional pins are placed into minimum current leakage state
- All registers and memories retain the content and any read/write registers access is disabled
- All clock sources are disabled
- PHY Macro is suspended:
 - Low power V_{BUS} sense comparator is enabled and all regular V_{BUS} comparators are disabled to minimize current consumption.
 - ID Detection circuitry is enabled
 - Remaining analog circuitry is disabled

Device stays in the IDLE state until a valid wake-up event occurs and transitions into the NORMAL (ACTIVE) State. If system reset is asserted (RSTn) device transitions to RESET state.

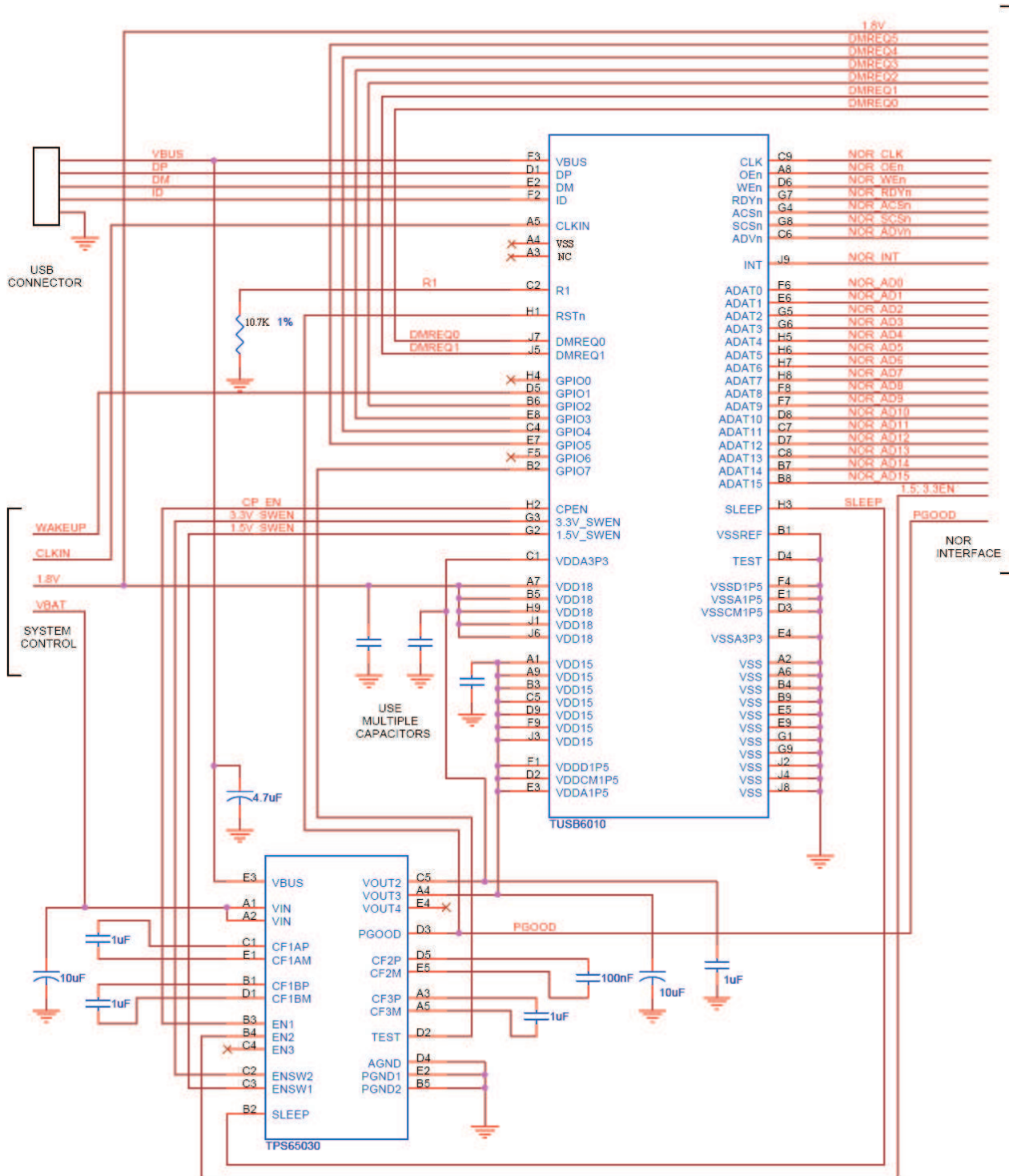
NORMAL (ACTIVE) State

A transition to the Normal state is required for normal device operation. All circuitry is enabled. In the Normal state:

- All I/O are enabled.
- All registers and memories are accessible
- Clock sources are enabled
- PHY Macro is enabled
 - Session End V_{BUS} detect circuitry shall be enabled
 - V_{BUS} detection circuitry shall be enabled
 - ID Detection circuitry shall be enabled

Application Diagram

Typical USB application utilizing the TPS65030 Power Management Device and TUSB6010. External Host connects to the NOR Interface and System Control Interface.



PRODUCT PREVIEW

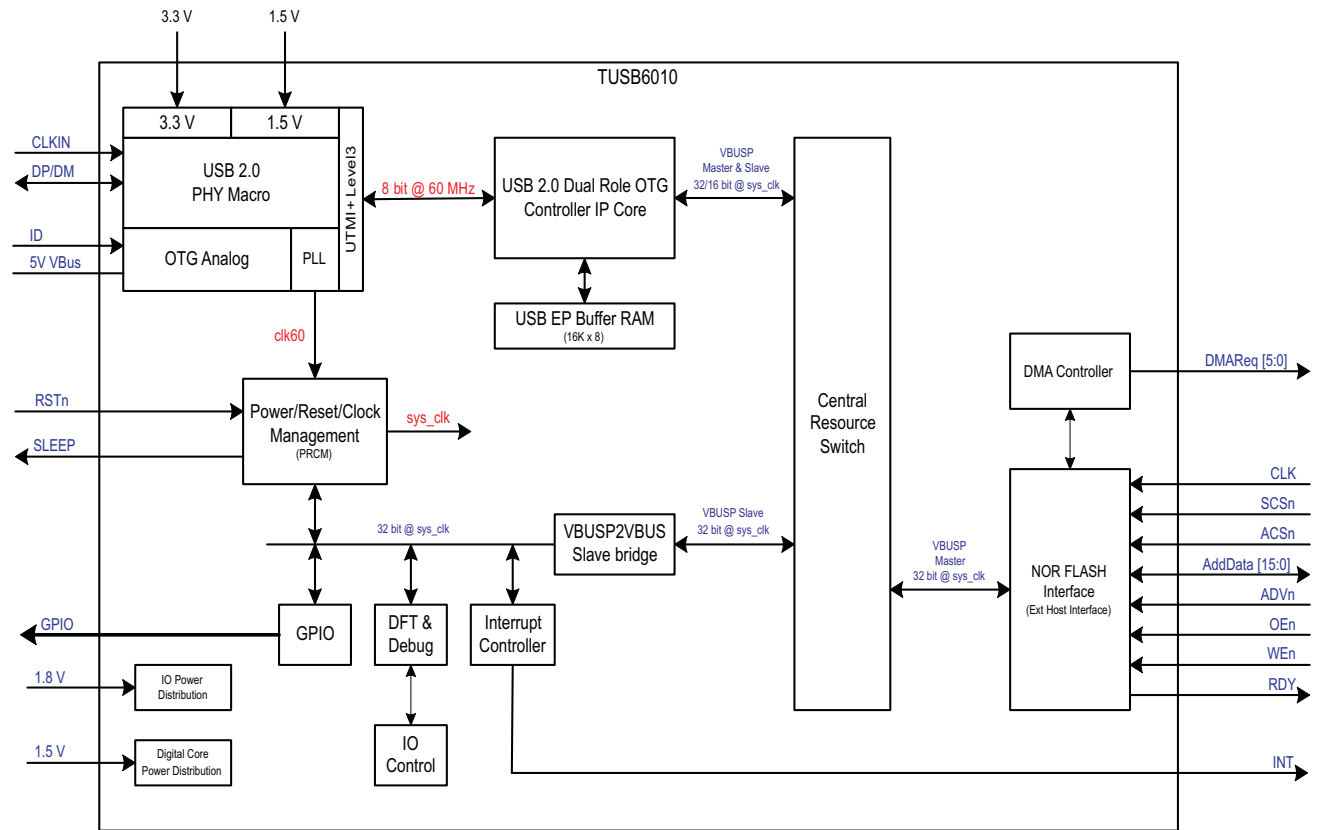


Figure 1. Device Block Diagram

PRODUCT PREVIEW

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB6010BIZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB6010BIZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	340.5	333.0	20.6

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