阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

ST-NXP Wireless

IMPORTANT NOTICE

Dear customer,

As from August 2nd 2008, the wireless operations of NXP have moved to a new company, ST-NXP Wireless.

As a result, the following changes are applicable to the attached document.

- **Company name - NXP B.V.** is replaced with **ST-NXP Wireless**.

- **Copyright** - the copyright notice at the bottom of each page "© NXP B.V. 200x. All rights reserved", shall now read: "© ST-NXP Wireless 200x - All rights reserved".

- **Web site** - http://www.nxp.com is replaced with http://www.stnwireless.com

- **Contact information** - the list of sales offices previously obtained by sending an email to salesaddresses@nxp.com , is now found at http://www.stnwireless.com under Contacts.

If you have any questions related to the document, please contact our nearest sales office. Thank you for your cooperation and understanding.

ST-NXP Wireless

ISP1505A; ISP1505C

ULPI Hi-Speed USB host and peripheral transceiver

Rev. 03 — 26 August 2008 Product data sheet

1. General description

The ISP1505 is a Universal Serial Bus (USB) high-speed host and peripheral transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0* and *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

The ISP1505 can transmit and receive USB data at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s), and provides a pin-optimized, physical layer front-end attachment to USB host, peripheral and OTG devices.

It is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) and any system chip set to interface with the physical layer of the USB through a 12-pin interface.

The ISP1505 can interface to the link with digital I/O voltages in the range of 1.65 V to 3.6 V.

The ISP1505 is available in HVQFN24 package.

2. Features

- Fully complies with:
  - *Universal Serial Bus Specification Rev. 2.0*
  - *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
- Interfaces to host and peripheral cores; optimized for stand-alone and embedded host applications with an external V_{BUS} supply; stand-alone peripheral cores, and Session Request Protocol (SRP)-capable peripheral cores
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
  - Integrated 45 Ω ± 10 % high-speed termination resistors, 1.5 kΩ ± 5 % full-speed device pull-up resistor, and 15 kΩ ± 5 % host termination resistors
  - Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - USB clock and data recovery to receive USB data up to ±500 ppm
  - Insertion of stuff bits during transmit and discarding of stuff bits during receive
  - Non-Return-to-Zero Inverted (NRZI) encoding and decoding
  - Supports bus reset, suspend, resume and high-speed detection handshake (chirp)
- Supports SRP for reduced power consumption
  - Complete control over bus resistors
  - Data line and V_{BUS} pulsing session request methods
  - Integrated V_{BUS} voltage comparators

- Highly optimized ULPI compliant
  - 60 MHz, 8-bit interface between the core and the transceiver
  - Supports 60 MHz output clock configuration
  - Integrated Phase-Locked Loop (PLL) supporting one crystal or clock frequency: 19.2 MHz (ISP1505ABS) and 26 MHz (ISP1505CBS)
  - Fully programmable ULPI-compliant register set
  - Internal Power-On Reset (POR) circuit
- Flexible system integration and very low current consumption, optimized for portable devices
  - Power-supply input range is 3.0 V to 3.6 V
  - Internal voltage regulator supplies 3.3 V and 1.8 V
  - Supports external V_{BUS} charge pump
  - External V_{BUS} source is controlled using the PSW_N pin; open-drain PSW_N allows per-port or ganged power control
  - FAULT input pin to monitor the external V_{BUS} supply status
  - Supports wide range interfacing I/O voltage of 1.65 V to 3.6 V; separate I/O voltage pins minimize crosstalk
  - Typical operating current of 10 mA to 48 mA, depending on the USB speed and bus utilization
  - Typical suspend current of 35 μA
- Full industrial grade operating temperature range from −40 °C to +85 °C
- 4 kV ElectroStatic Discharge (ESD) protection on pins DP, DM, V_{BUS} and GND
- Available in a small HVQFN24 (4 mm × 4 mm) Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

3. Applications

- Digital still camera
- Digital TV
- Digital Video Disc (DVD) recorder
- External storage device, for example:
  - Magneto-Optical (MO) drive
  - Optical drive: CD-ROM, CD-RW, DVD
  - Zip drive
- Mobile phone
- MP3 player
- PDA
- Printer
- Scanner
- Set-Top Box (STB)
- Video camera

4. Ordering information

Table 1. Ordering information

Part			Package		
Type number	**Marking**	**Crystal or clock frequency**	**Name**	**Description**	**Version**
ISP1505ABS	05A[1]	19.2 MHz	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3
ISP1505CBS	05C[1]	26 MHz	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm	SOT616-3

[1] The package marking is the first line of text on the IC package and can be used for IC identification.

5. Block diagram

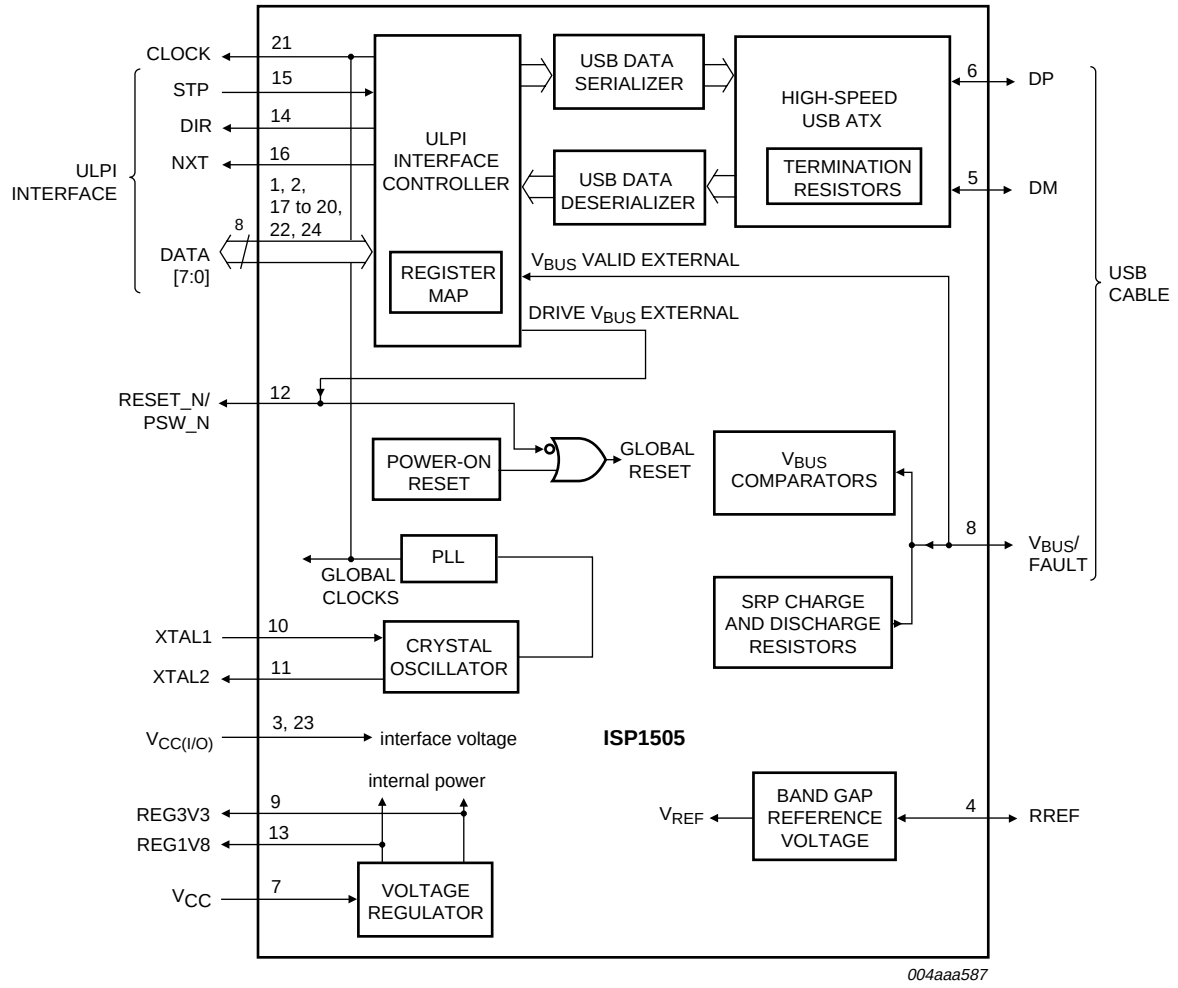


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

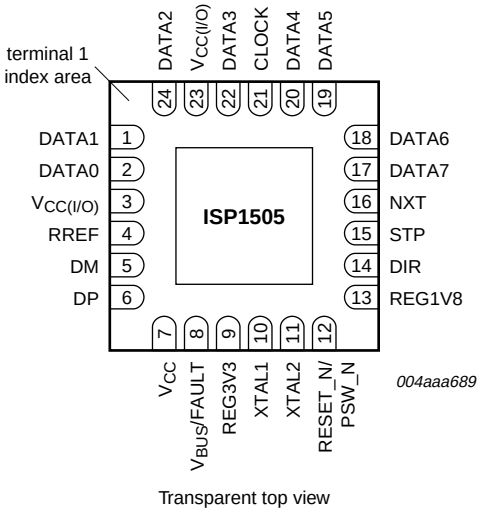


Fig 2. Pin configuration HVQFN24; top view

6.2 Pin description

Table 2. Pin description

Symbol[1][2]	Pin	Type[3]	Description[4]
DATA1	1	I/O	pin 1 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
DATA0	2	I/O	pin 0 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
$V_{CC(I/O)}$	3	P	I/O supply rail
RREF	4	AI/O	resistor reference
DM	5	AI/O	data minus (D–) pin of the USB cable
DP	6	AI/O	data plus (D+) pin of the USB cable
V_{CC}	7	P	input supply voltage or battery source
V_{BUS}/FAULT	8	AI/O	This pin has two possible functions: **V_{BUS} (analog input and output) —** V_{BUS} pin of the USB cable. **FAULT (input) —** Input pin for the external V_{BUS} digital overcurrent or fault detector signal. If this pin is not used as either V_{BUS} or FAULT, it must be connected to ground. 5 V tolerant
REG3V3	9	P	3.3 V regulator output
XTAL1	10	AI	crystal oscillator or clock input
XTAL2	11	AO	crystal oscillator output

Table 2. Pin description *...continued*

Symbol[1][2]	Pin	Type[3]	Description[4]
RESET_N/PSW_N	12	I/O	This pin has two possible functions: **RESET_N (input) —** Active LOW, asynchronous reset input. 3.3 V tolerant; plain input **PSW_N (output) —** Active LOW external V_{BUS} power switch or external charge pump enable. open-drain; 3.3 V tolerant If not used, this pin must be connected to $V_{CC(I/O)}$.
REG1V8	13	P	1.8 V regulator output
DIR	14	O	ULPI direction signal slew-rate controlled output (1 ns)
STP	15	I	ULPI stop signal plain input; programmable pull up
NXT	16	O	ULPI next signal slew-rate controlled output (1 ns)
DATA7	17	I/O	pin 7 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
DATA6	18	I/O	pin 6 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
DATA5	19	I/O	pin 5 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
DATA4	20	I/O	pin 4 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
CLOCK	21	O	60 MHz clock output slew-rate controlled output (1 ns)
DATA3	22	I/O	pin 3 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
$V_{CC(I/O)}$	23	P	I/O supply rail
DATA2	24	I/O	pin 2 of the bidirectional ULPI data bus slew-rate controlled output (1 ns); plain input; programmable pull down
GND	die pad	P	ground supply; down bonded to the exposed die pad (heat sink); to be connected to the PCB ground

[1] Symbol names ending with underscore N, for example, NAME_N, indicate active LOW signals.

[2] For details on external components required on each pin, see bill of materials and application diagrams in Section 16.

[3] I = input; O = output; I/O = digital input/output; AI = analog input; AO = analog output; AI/O = analog input/output; P = power or ground pin.

[4] A detailed description of these pins can be found in Section 7.10.

7. Functional description

7.1 ULPI interface controller

The ISP1505 provides a 12-pin interface that is compliant with *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*. This interface must be connected to the USB link.

The ULPI interface controller provides the following functions:

- ULPI-compliant interface and register set
- Allows full control over the USB peripheral, host and SRP functionality
- Parses the USB transmit and receive data
- Prioritizes the USB receive data, USB transmit data, interrupts and register operations
- Low-power mode
- External V_{BUS} source control
- V_{BUS} monitoring, charging and discharging
- 6-pin serial mode and 3-pin serial mode
- Generates RXCMDs; status updates
- Maskable interrupts

For more information on the ULPI protocol, see Section 9.

7.2 USB data serializer and deserializer

The USB data serializer prepares data to transmit on the USB bus. To transmit data, the USB link sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing and NRZI encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet, and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept any more data, the ULPI interface controller deasserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, and then performs serial-to-parallel conversion, NRZI decoding and discarding of stuff bits on the data payload. The ULPI interface controller sends data to the USB link by asserting DIR, and then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit stuff errors, elasticity buffer underrun or overrun, and byte-alignment errors.

7.3 Hi-Speed USB (USB 2.0) ATX

The Hi-Speed USB ATX block is an analog front-end containing the circuitry needed to transmit, receive and terminate the USB bus in high-speed, full-speed and low-speed, for USB peripheral, host and OTG implementations. The following circuitry is included:

- Differential drivers to transmit data at high-speed, full-speed and low-speed
- Differential and single-ended receivers to receive data at high-speed, full-speed and low-speed
- Squelch circuit to detect high-speed bus activity

- High-speed disconnect detector
- 45 Ω high-speed bus terminations on DP and DM for peripheral and host modes
- 1.5 kΩ pull-up resistor on DP for full-speed peripheral mode
- 15 kΩ bus terminations on DP and DM for host and OTG modes

For details on controlling resistor settings, see Table 7.

7.4 Voltage regulator

The ISP1505 contains a built-in voltage regulator that conditions the V_{CC} supply for use inside the ISP1505. The voltage regulator:

- Supports input supply range of 3.0 V < V_{CC} < 3.6 V
- Supplies internal circuitry with 1.8 V and 3.3 V

Remark: The REG1V8 and REG3V3 pins require external decoupling capacitors. For details, see Section 16.

7.5 Crystal oscillator and PLL

The ISP1505 has a built-in crystal oscillator and a Phase-Locked Loop (PLL) for clock generation.

The crystal oscillator takes a sine-wave input from an external crystal on the XTAL1 pin, and converts it to a square wave clock for internal use. Alternatively, a square wave clock of the same frequency can also be directly driven into the XTAL1 pin. Using an existing square wave clock can save the cost of the crystal and also reduce the board size.

The PLL takes the square wave clock from the crystal oscillator, and multiplies or divides it into various frequencies for internal use.

The PLL produces the following frequencies, irrespective of the clock source:

- 60 MHz clock for the ULPI interface controller
- 1.5 MHz for the low-speed USB data
- 12 MHz for the full-speed USB data
- 480 MHz for the high-speed USB data
- Other internal frequencies for data conversion and data recovery

7.6 V_{BUS} comparators

The ISP1505 provides three comparators, V_{BUS} valid comparator, session valid comparator and session end comparator, to detect the V_{BUS} voltage level.

7.6.1 V_{BUS} valid comparator

This comparator is used by hosts and A-devices to determine whether the voltage on V_{BUS} is at a valid level for operation. The ISP1505 minimum threshold for the V_{BUS} valid comparator is $V_{A\_VBUS\_VLD}$. Any voltage on V_{BUS} below $V_{A\_VBUS\_VLD}$ is considered a fault. During power-up, it is expected that the comparator output will be ignored.

While it is possible for the external 5 V supply to use the ISP1505 internal A_VBUS_VLD comparator, typical 5 V supplies must provide their own power fault indicator that can be connected as an input to the ISP1505 FAULT pin.

7.6.2 Session valid comparator

The session valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Peripherals, A-devices and B-devices use this comparator to detect when a session is started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold of the ISP1505 is $V_{B\_SESS\_VLD}$, with a hysteresis of $V_{hys(B\_SESS\_VLD)}$.

7.6.3 Session end comparator

The ISP1505 session end comparator determines when V_{BUS} is below the B-device session end threshold. The B-device uses this threshold to determine when a session has ended. The session end threshold of the ISP1505 is $V_{B\_SESS\_END}$.

7.7 SRP charge and discharge resistors

The ISP1505 provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore the V_{BUS} power. First, the B-device makes sure that V_{BUS} is fully discharged from the previous session by setting the DISCHRG_VBUS register bit to logic 1 and waiting for SESS_END to be logic 1. Then the B-device charges V_{BUS} by setting the CHRG_VBUS register bit to logic 1. The A-device sees that V_{BUS} is charged above the session valid threshold and starts a session by turning on the V_{BUS} power.

7.8 Band gap reference voltage

The band gap circuit provides a stable internal voltage reference to bias the analog circuitry. The band gap requires an accurate external reference resistor R_{RREF} connected between the RREF and GND pins. For details, see Section 16.

7.9 Power-on reset

The ISP1505 has an internal power-on reset circuit that resets all internal logic on power-up. The ULPI interface is also reset at power-up.

Remark: When CLOCK starts toggling after power-up, the USB link must issue a reset command over the ULPI bus to ensure correct operation of the ISP1505.

7.10 Detailed description of pins

7.10.1 DATA[7:0]

The ISP1505 is a Physical layer (PHY) containing a USB transceiver. DATA[7:0] is a bidirectional data bus. The USB link must drive DATA[7:0] to LOW when the ULPI bus is idle. When the link has data to transmit to the PHY, it drives a nonzero value.

Weak pull-down resistors are incorporated into DATA[7:0] pins as part of the interface protect feature. For details, see Section 9.3.1.

The data bus can be reconfigured to carry various data types, as given in Section 8 and Section 9.

7.10.2 $V_{CC(I/O)}$

The input power pin that sets the I/O voltage level. For details, see Section 12, Section 13 and Section 16. $V_{CC(I/O)}$ provides power to on-chip pads of the following pins:

- CLOCK
- DATA[7:0]
- DIR
- NXT
- RESET_N
- STP

7.10.3 RREF

Resistor reference analog I/O pin. A resistor, R_{RREF}, must be connected between RREF and GND, as shown in Section 16. This provides an accurate voltage reference that biases internal analog circuitry. Less accurate resistors cannot be used and will render the ISP1505 unusable.

7.10.4 DP and DM

The DP (data plus) and DM (data minus) are USB differential data pins. These must be connected to the D+ and D– pins of the USB receptacle.

7.10.5 V_{CC}

V_{CC} is the main input supply voltage for the ISP1505. Decoupling capacitors are recommended. For details, see Section 16.

7.10.6 V_{BUS}/FAULT

This pin provides two options for V_{BUS} driving and monitoring. If neither function is used, this pin must be connected to ground.

7.10.6.1 V_{BUS}

By default, this pin acts as an input to V_{BUS} comparators, and also charges and discharges V_{BUS} for SRP.

The V_{BUS} pin requires a capacitive load as shown in Section 16.

To prevent electrical overstress, it is strongly recommended that you attach a series resistor on the V_{BUS} pin (R_{VBUS}). R_{VBUS} must not be attached when using the ISP1505 internal charge pump. For details, see Section 16.

7.10.6.2 FAULT (external overcurrent or fault detector)

If an external V_{BUS} overcurrent or fault circuit is used, the output fault indicator of that circuit can be connected to the ISP1505 FAULT input pin. The ISP1505 will inform the link of V_{BUS} fault events by sending RXCMDs on the ULPI bus. To use the FAULT pin, the link must:

- Set the USE_EXT_VBUS_IND register bit to logic 1.
- Set the polarity of the external fault signal using the IND_COMPL register bit.
- Set the IND_PASSTHRU register bit to logic 1.

7.10.7 REG3V3 and REG1V8

Regulator output voltage. These supplies are used to power the ISP1505 internal digital and analog circuits, and must not be used to power external circuits.

For correct operation of the regulator, it is recommended that you connect REG3V3 and REG1V8 to decoupling capacitors. For an example, see Section 16.

7.10.8 XTAL1 and XTAL2

XTAL1 is the crystal input, and XTAL2 is the crystal output. The allowed frequency on the XTAL1 pin depends on the ISP1505 product version.

If the link requires a 60 MHz clock from the ISP1505, then either a crystal must be attached, or a clock of the same frequency must be driven into XTAL1, with XTAL2 left floating.

If a crystal is attached, it requires external load capacitors to GND on each terminal of the crystal. For details, see Section 16.

If at any time the system wants to stop the clock on XTAL1, the link must first put the ISP1505 into low-power mode. The clock on XTAL1 must be restarted before low-power mode is exited.

7.10.9 RESET_N/PSW_N

This pin provides two optional functions. If neither function is used, this pin must be connected to $V_{CC(I/O)}$.

7.10.9.1 RESET_N

An active LOW asynchronous reset pin that resets all circuits in the ISP1505. The ISP1505 contains an internal power-on reset circuit, and therefore using the RESET_N pin is optional. If RESET_N is not used, it must be connected to $V_{CC(I/O)}$.

For details on using RESET_N, see Section 9.3.2.

7.10.9.2 PSW_N

PSW_N is an active LOW, open-drain output pin. This pin can be connected to an active LOW, external V_{BUS} switch or charge pump enable circuit to control the external V_{BUS} power source. An external pull-up resistor, R_{pullup}, is required when PSW_N is used. This pin is open-drain, allowing ganged-mode power control for multiple USB ports. For application details, see Section 16.

To use the PSW_N pin, the link must disable the reset input by setting the IGNORE_RESET bit in the Power Control register to logic 1. This will ensure that PSW_N is not misinterpreted as a reset.

If the link is in host mode, it can enable the external V_{BUS} power source by setting the DRV_VBUS_EXT bit in the OTG Control register to logic 1. The ISP1505 will drive PSW_N to LOW to enable the external V_{BUS} power source. If the link detects an overcurrent condition (the V_{BUS} state in RXCMD is not 11b), it must disable the external V_{BUS} supply by setting DRV_VBUS_EXT to logic 0.

7.10.10 DIR

ULPI direction output pin. Controls the direction of the data bus. By default, the ISP1505 holds DIR at LOW, causing the data bus to be an input. When DIR is LOW, the ISP1505 listens for data from the link. The ISP1505 pulls DIR to HIGH only when it has data to send to the link, which is for one of two reasons:

- To send the USB receive data, RXCMD status updates and register reads data to the link.
- To block the link from driving the data bus during power-up, reset and low-power mode (suspend).

For details on DIR usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.10.11 STP

ULPI stop input pin. The link must assert STP to signal the end of a USB transmit packet or a register write operation. When DIR is asserted, the link can optionally assert STP to abort the ISP1505, causing it to deassert DIR in the next clock cycle. A weak pull-up resistor is incorporated into the STP pin as part of the interface protect feature. For details, see Section 9.3.1.

For details on STP usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.10.12 NXT

ULPI next data output pin. The ISP1505 holds NXT at LOW, by default. When DIR is LOW and the link is sending data to the ISP1505, NXT will be asserted to notify the link to provide the next data byte. When DIR is at HIGH and the ISP1505 is sending data to the link, NXT will be asserted to notify the link that another valid byte is on the bus. NXT is not used for the register read data or the RXCMD status update.

For details on NXT usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.10.13 CLOCK

A 60 MHz interface clock to synchronize the ULPI bus. The ISP1505 provides two clocking options:

- A crystal is attached between the XTAL1 and XTAL2 pins.
- A clock is driven into the XTAL1 pin, with the XTAL2 pin left floating.

For details on CLOCK usage, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

7.10.14 GND (die pad)

Global ground signal. The die pad is exposed on the underside of the package as a ground plate. This acts as a ground to all circuits in the ISP1505. To ensure correct operation of the ISP1505, GND must be soldered to the cleanest ground available.

8. Modes of operation

8.1 ULPI modes

The ISP1505 ULPI bus can be programmed to operate in four modes. Each mode reconfigures the signals on the data bus as described in the following subsections. Setting more than one mode will lead to undefined behavior.

8.1.1 Synchronous mode

This is default mode. At power-up, and when CLOCK is stable, the ISP1505 will enter synchronous mode. The link must synchronize all ULPI signals to CLOCK, meeting the set-up and hold times as defined in Section 15. A description of the ULPI pin behavior in synchronous mode is given in Table 3.

This mode is used by the link to perform the following tasks:

- High-speed detection handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RXCMDs)

For more information on various synchronous mode protocols, see Section 9.

Table 3. ULPI signal description

Signal name	Direction on ISP1505	Signal description
CLOCK	O	**60 MHz interface clock**. If a crystal is attached or a clock is driven into the XTAL1 pin, the ISP1505 will drive a 60 MHz output clock.
DATA[7:0]	I/O	**8-bit data bus**. In synchronous mode, the link drives DATA[7:0] to LOW by default. The link initiates transfers by sending a nonzero data pattern called TXCMD (transmit command). In synchronous mode, the direction of DATA[7:0] is controlled by DIR. Contents of DATA[7:0] lines must be ignored for exactly one clock cycle whenever DIR changes value. This is called the turnaround cycle. Data lines have fixed direction and different meaning in low-power and serial modes.

Table 3. ULPI signal description *…continued*

Signal name	Direction on ISP1505	Signal description
DIR	O	**Direction**: Controls the direction of data bus DATA[7:0]. In synchronous mode, the ISP1505 drives DIR to LOW by default, making the data bus an input so that the ISP1505 can listen for TXCMDs from the link. The ISP1505 drives DIR to HIGH only when it has data for the link. When DIR and NXT are HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called RXCMD (receive command). The only exception to this rule is when the PHY returns register read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which DATA[7:0] is not valid and must be ignored by the link. DIR is always asserted during low-power and serial modes.
STP	I	**Stop**: In synchronous mode, the link drives STP to HIGH for one cycle after the last byte of data is sent to the ISP1505. The link can optionally assert STP to force DIR to be deasserted. In low-power and serial modes, the link holds STP at HIGH to wake up the ISP1505, causing the ULPI bus to return to synchronous mode.
NXT	O	**Next**: In synchronous mode, the ISP1505 drives NXT to HIGH to throttle data. If DIR is LOW, the ISP1505 asserts NXT to notify the link to place the next data byte on DATA[7:0] in the following clock cycle. If DIR is HIGH, the ISP1505 asserts NXT to notify the link that a valid USB data byte is on DATA[7:0] in the current cycle. The ISP1505 always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register read data is to be returned to the link in the current cycle. NXT is not used in low-power or serial mode.

8.1.2 Low-power mode

When the USB is idle, the link can place the ISP1505 into low-power mode (also called suspend mode). In low-power mode, the data bus definition changes to that shown in Table 4. To enter low-power mode, the link sets the SUSPENDM bit in the Function Control register to logic 0. To exit low-power mode, the link asserts the STP signal. The ISP1505 will draw only suspend current from the V_{CC} supply (see Table 44).

During low-power mode, the clock on XTAL1 may be stopped. The clock must be started again before asserting STP to exit low-power mode. After exiting low-power mode, the ISP1505 will send an RXCMD to the link if a change was detected in any interrupt source, and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

For more information on low-power mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 4. Signal mapping during low-power mode

Signal	Maps to	Direction	Description
LINESTATE0	DATA0	O	combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	DATA1	O	combinatorial LINESTATE1 directly driven by the analog receiver

Table 4. Signal mapping during low-power mode *…continued*

Signal	Maps to	Direction	Description
Reserved	DATA2	O	reserved; the ISP1505 will drive this pin to LOW
INT	DATA3	O	active HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1505 will drive these pins to LOW

8.1.3 6-pin full-speed or low-speed serial mode

If the link requires a 6-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1505 to 6-pin serial mode. In 6-pin serial mode, the DATA[7:0] bus definition changes to that shown in Table 5. To enter 6-pin serial mode, the link sets the 6PIN_FSLS_SERIAL bit in the Interface Control register to logic 1. To exit 6-pin serial mode, the link asserts STP. This is provided primarily for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1.

For more information on 6-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 5. Signal mapping for 6-pin serial mode

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	active HIGH transmit enable
TX_DAT	DATA1	I	transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	active HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DM
RX_RCV	DATA6	O	differential receive data from DP and DM
Reserved	DATA7	O	reserved; the ISP1505 will drive this pin to LOW

8.1.4 3-pin full-speed or low-speed serial mode

If the link requires a 3-pin serial interface to transmit and receive full-speed or low-speed USB data, it can set the ISP1505 to 3-pin serial mode. In 3-pin serial mode, the data bus definition changes to that shown in Table 6. To enter 3-pin serial mode, the link sets the 3PIN_FSLS_SERIAL bit in the Interface Control register to logic 1. To exit 3-pin serial mode, the link asserts STP. This is primarily provided for links that contain legacy full-speed or low-speed functionality, providing a more cost-effective upgrade path to high-speed. An interrupt pin is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLOCK_SUSPENDM register bit must be set to logic 1.

For more information on 3-pin serial mode enter and exit protocols, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

Table 6. Signal mapping for 3-pin serial mode

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	active HIGH transmit enable
DAT	DATA1	I/O	transmit differential data on DP and DM when TX_ENABLE is HIGH receive differential data from DP and DM when TX_ENABLE is LOW
SE0	DATA2	I/O	transmit single-ended zero on DP and DM when TX_ENABLE is HIGH receive single-ended zero from DP and DM when TX_ENABLE is LOW
INT	DATA3	O	active HIGH interrupt indication; will be asserted whenever any unmasked interrupt occurs
Reserved	DATA[7:4]	O	reserved; the ISP1505 will drive these pins to LOW

8.2 USB and OTG state transitions

A Hi-Speed USB peripheral, host or OTG device handles more than one electrical state as defined in *Universal Serial Bus Specification Rev. 2.0* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*. The ISP1505 accommodates the various states through register bit settings of XCVRSELECT[1:0], TERMSELECT, OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN.

Table 7 summarizes operating states. The values of register settings in Table 7 will force resistor settings as also given in Table 7. Resistor setting signals are defined as follows:

- RPU_DP_EN enables the 1.5 kΩ pull-up resistor on DP
- RPD_DP_EN enables the 15 kΩ pull-down resistor on DP
- RPD_DM_EN enables the 15 kΩ pull-down resistor on DM
- HSTERM_EN enables the 45 Ω termination resistors on DP and DM

It is up to the link to set the desired register settings.

Table 7. Operating states and their corresponding resistor settings

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_PULL DOWN	DM_PULL DOWN	RPU_ DP_EN	RPD_ DP_EN	RPD_ DM_EN	HSTERM _EN
General settings									
3-state drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b
Power-up or $V_{BUS} < V_{B\_SESS\_END}$	01b	0b	00b	1b	1b	0b	1b	1b	0b
Host settings									
Host chirp	00b	0b	10b	1b	1b	0b	1b	1b	1b
Host high-speed	00b	0b	00b	1b	1b	0b	1b	1b	1b
Host full-speed	X1b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed suspend	01b	1b	00b	1b	1b	0b	1b	1b	0b
Host high-speed or full-speed resume	01b	1b	10b	1b	1b	0b	1b	1b	0b
Host low-speed	10b	1b	00b	1b	1b	0b	1b	1b	0b

Table 7. Operating states and their corresponding resistor settings *…continued*

Signaling mode	Register settings					Internal resistor settings			
	XCVR SELECT [1:0]	TERM SELECT	OPMODE [1:0]	DP_PULL DOWN	DM_PULL DOWN	RPU_ DP_EN	RPD_ DP_EN	RPD_ DM_EN	HSTERM _EN
Host low-speed suspend	10b	1b	00b	1b	1b	0b	1b	1b	0b
Host low-speed resume	10b	1b	10b	1b	1b	0b	1b	1b	0b
Host Test J or Test K	00b	0b	10b	1b	1b	0b	1b	1b	1b
Peripheral settings									
Peripheral chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral high-speed	00b	0b	00b	0b	0b	0b	0b	0b	1b
Peripheral full-speed	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b
Peripheral high-speed or full-speed resume	01b	1b	10b	0b	0b	1b	0b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b	0b	0b	0b	1b
OTG settings									
OTG device peripheral chirp	00b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed	00b	0b	00b	0b	1b	0b	0b	1b	1b
OTG device peripheral full-speed	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed suspend	01b	1b	00b	0b	1b	1b	0b	1b	0b
OTG device peripheral high-speed and full-speed resume	01b	1b	10b	0b	1b	1b	0b	1b	0b
OTG device peripheral Test J or Test K	00b	0b	10b	0b	1b	0b	0b	1b	1b

9. Protocol description

The following subsections describe the protocol for using the ISP1505.

9.1 ULPI references

The ISP1505 provides a 12-pin ULPI interface to communicate with the link. It is highly recommended that you read *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and *UTMI+ Specification Rev. 1.0*.

9.2 Power-On Reset (POR)

An internal POR is generated when REG1V8 rises above $V_{POR(trip)}$, for at least $t_{w(REG1V8\_H)}$. The internal POR pulse will also be generated whenever REG1V8 drops below $V_{POR(trip)}$ for more than $t_{w(REG1V8\_L)}$, and then rises above $V_{POR(trip)}$ again. The voltage on REG1V8 is generated from V_{CC}.

To give a better view of the functionality, Figure 3 shows a possible curve of REG1V8. The internal POR starts with logic 0 at t0. At t1, the detector will see the passing of the trip level so that POR turns to logic 1 and a delay element will add another t_{PORP} before it drops to logic 0. If REG1V8 dips from t2 to t3 for > $t_{w(REG1V8\_L)}$, another POR pulse is generated. If the dip at t4 to t5 is too short, that is, < $t_{w(REG1V8\_L)}$, the internal POR pulse will not react and will remain LOW.

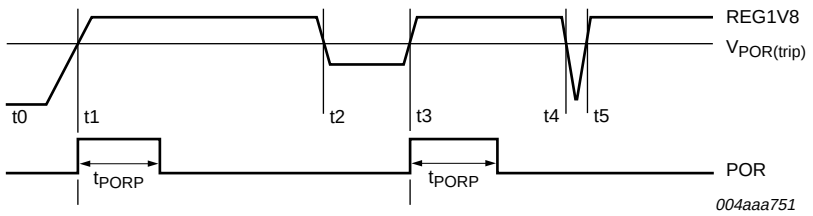


Fig 3. Internal power-on reset timing

9.3 Power-up, reset and bus idle sequence

Figure 4 shows a typical start-up sequence.

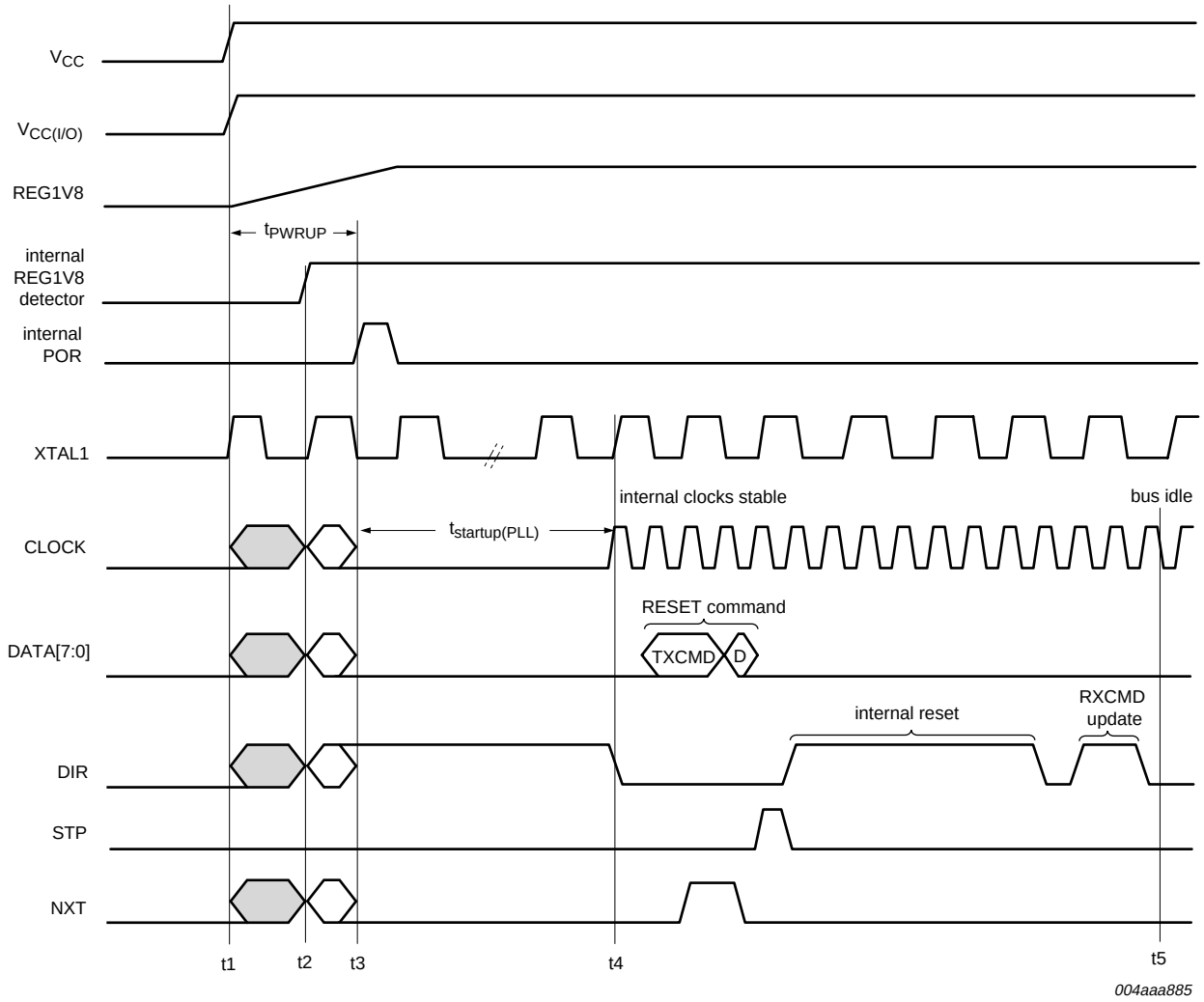
On power-up, the ISP1505 performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the ISP1505 deasserts DIR. The power-up time depends on the V_{CC} supply rise time, the crystal start-up time, and PLL start-up time $t_{startup(o)(CLOCK)}$. Whenever DIR is asserted, the ISP1505 drives the NXT pin to LOW and drives DATA[7:0] with RXCMD values. When DIR is deasserted, the link must drive the data bus to a valid level. By default, the link must drive data to LOW. When the ISP1505 initially deasserts DIR on power-up, the link must ignore all RXCMDs until it resets the ISP1505. Before beginning USB packets, the link must set the RESET bit in the Function Control register to reset the ISP1505. After the RESET bit is set, the ISP1505 will assert DIR until the internal reset completes. The ISP1505 will automatically deassert DIR and clear the RESET bit when reset has completed. After every reset, an RXCMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

If a crystal is attached or a clock is driven into the XTAL1 pin, the ISP1505 will drive a 60 MHz clock out from the CLOCK pin when DIR deasserts. This is shown as CLOCK in Figure 4.

The recommended power-up sequence for the link is as follows:

1. The link waits for 1 ms, ignoring all the ULPI pin status.
2. The link may start to detect DIR status level. If DIR is detected as LOW for three clock cycles, the link may send a RESET command.

The ULPI interface is ready for use.



t1 = V_{CC} and $V_{CC(I/O)}$ are applied to the ISP1505. The ISP1505 regulator starts to turn on.

t2 = ULPI pads detect REG1V8 rising above the REG1V8 regulator threshold and are not in 3-state. These pads may drive either LOW or HIGH. It is recommended that the link ignores the ULPI pins status during t_{PWRUP}.

t3 = The POR threshold is reached and a POR pulse is generated. After the POR pulse, ULPI pins are driven to a defined level. DIR is driven to HIGH and the other pins are driven to LOW.

t4 = The internal PLL is stabilized after $t_{startup(PLL)}$. If the 19.2 MHz or 26 MHz clock is started before POR, the internal PLL will be stabilized after $t_{startup(PLL)}$ from POR. The CLOCK pin starts to output 60 MHz. The DIR pin will transition from HIGH to LOW. The DIR pin will remain LOW before the link issues a RESET command to the ISP1505.

t5 = The power-up sequence is completed and the ULPI bus interface is ready for use.

Fig 4. Power-up and reset sequence required before the ULPI bus is ready for use

9.3.1 Interface protection

By default, the ISP1505 enables a weak pull-up resistor on STP. If the STP pin is unexpectedly HIGH at any time, the ISP1505 will protect the ULPI interface by enabling weak pull-down resistors on DATA[7:0].

The interface protect feature prevents unwanted activity of the ISP1505 whenever the ULPI interface is not correctly driven by the link. For example, when the link powers up more slowly than the ISP1505.

The interface protect feature can be disabled by setting the INTF_PROT_DIS bit to logic 1.

9.3.2 Interface behavior with respect to RESET_N

The use of the RESET_N pin is optional. When RESET_N is asserted (LOW), the ISP1505 will assert DIR. All logic in the ISP1505 will be reset, including the analog circuitry and ULPI registers. During reset, the link must drive DATA[7:0] and STP to LOW; otherwise undefined behavior may result. When RESET_N is deasserted (HIGH), the DIR output will deassert (LOW) four or five clock cycles later. Figure 5 shows the ULPI interface behavior when RESET_N is asserted (LOW), and subsequently deasserted (HIGH). If RESET_N is not used, it must be connected to $V_{CC(I/O)}$.

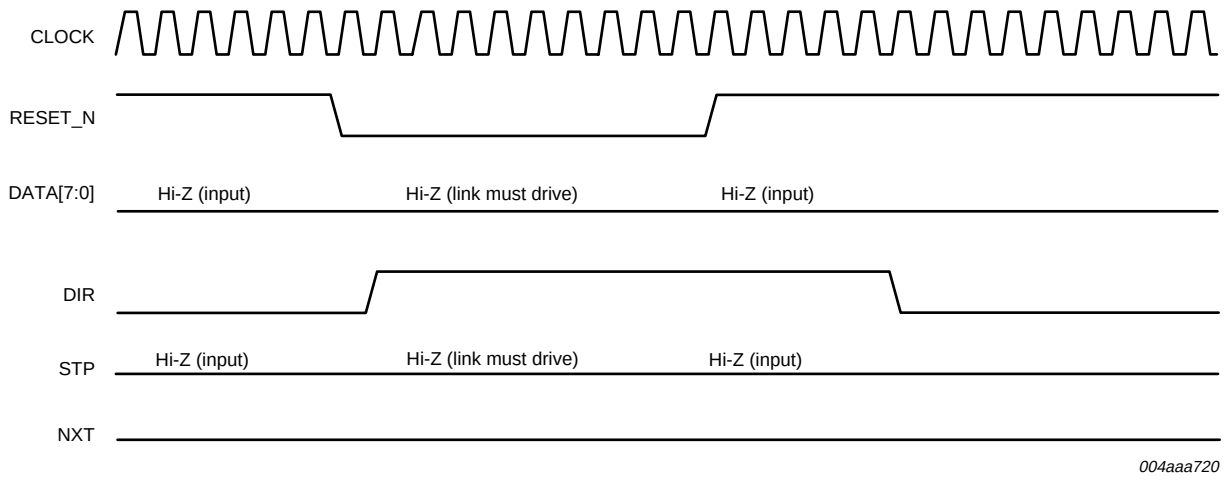


Fig 5. Interface behavior with respect to RESET_N

9.4 V_{BUS} power and fault detection

9.4.1 Driving 5 V on V_{BUS}

The ISP1505 supports external 5 V supplies. The ISP1505 can control the external supply using the active-LOW PSW_N open-drain output pin. To enable the external supply by driving PSW_N to LOW, the link must set the DRV_VBUS_EXT bit in the OTG Control register to logic 1. When the DRV_VBUS_EXT bit is set, the DRV_VBUS bit can be set to any value and will be ignored.

9.4.2 Fault detection

The ISP1505 supports external V_{BUS} fault detector circuits. An overcurrent detection circuit is required for host applications that supply more than 100 mA on V_{BUS} for voltages between 4.75 V to 5.25 V. For low-power applications supplying less than 100 mA, the V_{BUS} power line can directly be connected to the V_{BUS}/FAULT pin on the ISP1505 and the link can utilize the internal A_VBUS_VLD comparator.

The ISP1505 supports external V_{BUS} fault detector circuits that output a digital fault indicator signal. The indicator signal must be connected to the V_{BUS}/FAULT pin. To enable the ISP1505 to monitor the digital fault input, the link must set the USE_EXT_VBUS_IND bit in the OTG Control register and the IND_PASSTHRU bit in the Interface Control register to logic 1. For details, see Figure 7.

The FAULT input pin is mapped to the A_VBUS_VLD bit in RXCMD. Any changes for the FAULT input will trigger RXCMD carrying the FAULT condition with A_VBUS_VLD.

9.5 TXCMD and RXCMD

Commands between the ISP1505 and the link are described in the following subsections.

9.5.1 TXCMD

By default, the link must drive the ULPI bus to its idle state of 00h. To send commands and USB packets, the link drives a nonzero value on DATA[7:0] to the ISP1505 by sending a byte called TXCMD. Commands include USB packet transmissions, and register reads and writes. Once the TXCMD is interpreted and accepted by the ISP1505, the NXT signal is asserted and the link can follow up with the required number of data bytes. The TXCMD byte format is given in Table 8. Any values other than those in Table 8 are illegal and may result in undefined behavior.

Various TXCMD packet and register sequences are shown in later sections.

Table 8. TXCMD byte format

Command type name	Command code DATA[7:6]	Command payload DATA[5:0]	Command name	Command description
Idle	00b	00 0000b	NOOP	No operation. 00h is the idle value of the data bus. The link must drive NOOP by default.
Packet transmit	01b	00 0000b	NOPID	Transmit USB data that does not have a PID, such as chirp and resume signaling. The ISP1505 starts transmitting only after accepting the next data byte.
		00 XXXXb	PID	Transmit USB packet. DATA[3:0] indicates USB packet identifier PID[3:0].
Register write	10b	10 1111b	EXTW	Extended register write command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGW	Register write command with 6-bit immediate address.
Register read	11b	10 1111b	EXTR	Extended register read command (optional). The 8-bit address must be provided after the command is accepted.
		XX XXXXb	REGR	Register read command with 6-bit immediate address.

9.5.2 RXCMD

The ISP1505 communicates status information to the link by asserting DIR and sending an RXCMD byte on the data bus. The RXCMD data byte format is given in Table 9.

The ISP1505 will automatically send an RXCMD whenever there is a change in any of the RXCMD data fields. The link must be able to accept an RXCMD at any time; including single RXCMDs, back-to-back RXCMDs, and RXCMDs at any time during USB receive packets when NXT is LOW. An example is shown in Figure 6. For details and diagrams, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

An RXCMD may not be sent when exiting low-power mode or serial mode, if the interrupt condition is removed before exiting.

Table 9. RXCMD byte format

DATA	Name	Description and value
1 to 0	LINESTATE	**LINESTATE signals**: For a definition of LINESTATE, see Section 9.5.2.1. **DATA0 —** LINESTATE[0] **DATA1 —** LINESTATE[1]
3 to 2	V_{BUS} state	**Encoded V_{BUS} voltage state**: For an explanation of the V_{BUS} state, see Section 9.5.2.2.
5 to 4	RxEvent	**Encoded USB event signals**: For an explanation of RxEvent, see Section 9.5.2.4.
6	reserved	-
7	ALT_INT	By default, this signal is not used and is not needed in typical designs. Optionally, the link can enable the BVALID_RISE and/or BVALID_FALL bits in the Power Control register. Corresponding changes in BVALID will cause an RXCMD to be sent to the link with the ALT_INT bit asserted.

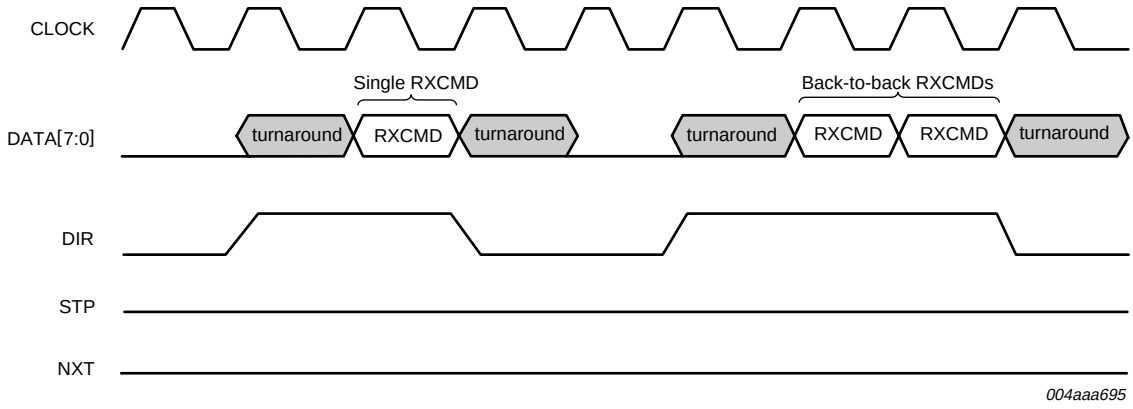


Fig 6. Single and back-to-back RXCMDs from the ISP1505 to the link

9.5.2.1 Linestate encoding

LINESTATE[1:0] reflects the current state of DP and DM. Whenever the ISP1505 detects a change in DP or DM, an RXCMD will be sent to the link with the new LINESTATE[1:0] value. The value given on LINESTATE[1:0] depends on the setting of various registers.

Table 10 shows the LINESTATE[1:0] encoding for upstream facing ports, which applies to peripherals. Table 11 shows the LINESTATE[1:0] encoding for downstream facing ports, which applies to host controllers. Dual-role devices must choose the correct table, depending on whether it is in peripheral or host mode.

Table 10. LINESTATE[1:0] encoding for upstream facing ports: peripheral
DP_PULLDOWN = 0.[1]

Mode		Full-speed	High-speed	Chirp
XCVRSELECT[1:0]		01, 11	00	00
TERMSELECT		1	0	1
LINESTATE[1:0]	00	SE0	squelch	squelch
	01	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

Table 11. LINESTATE[1:0] encoding for downstream facing ports: host
DP_PULLDOWN and DM_PULLDOWN = 1.[1]

Mode		Low-speed	Full-speed	High-speed	Chirp
XCVRSELECT[1:0]		10	01, 11	00	00
TERMSELECT		1	1	0	0
OPMODE[1:0]		X	X	00, 01, 11	10
LINESTATE[1:0]	00	SE0	SE0	squelch	squelch
	01	LS-K	FS-J	!squelch	!squelch and HS_Differential_Receiver_Output
	10	LS-J	FS-K	invalid	!squelch and !HS_Differential_Receiver_Output
	11	SE1	SE1	invalid	invalid

[1] !squelch indicates inactive squelch. !HS_Differential_Receiver_Output indicates inactive HS_Differential_Receiver_Output.

9.5.2.2 V_{BUS} state encoding

USB devices must monitor the V_{BUS} voltage for purposes such as overcurrent detection, starting a session and SRP. The V_{BUS} state field in the RXCMD is an encoding of the voltage level on V_{BUS}.

The A_VBUS_VLD, SESS_VLD and SESS_END indicators in the V_{BUS} state are directly taken from internal comparators built-in to the ISP1505, and encoded as shown in Table 9 and Table 12.

An RXCMD may not be sent when exiting low-power mode or serial mode, if the interrupt condition is removed before exiting.

Table 12. Encoded V_{BUS} voltage state

Value	V_{BUS} voltage	SESS_END	SESS_VLD	A_VBUS_VLD
00	$V_{BUS} < V_{B\_SESS\_END}$	1	0	0
01	$V_{B\_SESS\_END} \leq V_{BUS} < V_{B\_SESS\_VLD}$	0	0	0
10	$V_{B\_SESS\_VLD} \leq V_{BUS} < V_{A\_VBUS\_VLD}$	X	1	0
11	$V_{BUS} \geq V_{A\_VBUS\_VLD}$	X	X	1

Note that V_{BUS} and FAULT share the same pin and cannot be simultaneously used. A_VBUS_VLD and FAULT will be interpreted by the ISP1505 as shown in Figure 7.

A description on how to use and select the V_{BUS} state encoding is given in Section 9.5.2.3.

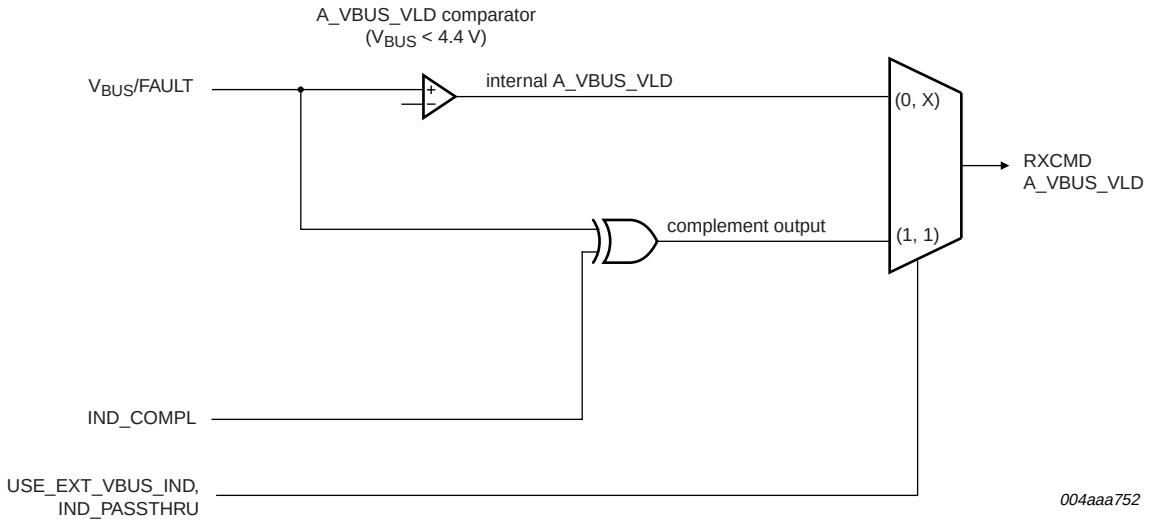


Fig 7. RXCMD A_VBUS_VLD indicator source

9.5.2.3 Using and selecting the V_{BUS} state encoding

The V_{BUS} state encoding is shown in Table 9. The ISP1505 will send an RXCMD to the link whenever there is a change in the V_{BUS} state. To receive V_{BUS} state updates, the link must first enable the corresponding interrupts in the USB Interrupt Enable Rising Edge and USB Interrupt Enable Falling Edge registers.

The link can use the V_{BUS} state to monitor V_{BUS} and take appropriate action. Table 13 shows the recommended usage for typical applications.

Table 13. V_{BUS} indicators in RXCMD required for typical applications

Application	A_VBUS_VLD	SESS_VLD	SESS_END
Standard host	yes	no	no
Standard peripheral	no	yes	no
OTG A-device	yes	yes	no
OTG B-device	no	yes	yes

Standard USB host controllers: For standard hosts, the system must be able to provide 500 mA on V_{BUS} in the range of 4.75 V to 5.25 V. An external circuit must be used to detect overcurrent conditions. If the external overcurrent detector provides a digital fault signal, then the fault signal must be connected to the ISP1505 FAULT input pin, and the link must do the following:

1. Set the IND_COMPL bit in the Interface Control register to logic 0 or logic 1, depending on the polarity of the external fault signal.
2. Set the IND_PASSTHRU bit in the Interface Control register to logic 1.
3. Set the USE_EXT_VBUS_IND bit in the OTG Control register to logic 1.

Standard USB peripheral controllers: Standard peripherals must be able to detect when V_{BUS} is at a sufficient level for operation. SESS_VLD must be enabled to detect the start and end of USB peripheral operations. Detection of A_VBUS_VLD and SESS_END thresholds is not needed for standard peripherals.

OTG devices: The ISP1505 provides partial OTG support. A low-power OTG A-device that supplies less than 100 mA on V_{BUS} can connect the V_{BUS} power to the ISP1505 V_{BUS} pin. The internal A_VBUS_VLD comparator can be used. If the OTG A-device provides more than 100 mA on V_{BUS}, an overcurrent detector must be used and Section "Standard USB host controllers" on page 25 applies. The OTG A-device also uses SESS_VLD to detect when an OTG B-device is initiating V_{BUS} pulsing SRP.

When an OTG device is configured as an OTG B-device, SESS_VLD must be used to detect when V_{BUS} is at a sufficient level for operation. SESS_END must be used to detect when V_{BUS} has dropped to a LOW level, allowing the B-device to safely initiate V_{BUS} pulsing SRP.

9.5.2.4 RxEvent encoding

The RxEvent field (see Table 14) of the RXCMD informs the link of information related packets received on the USB bus. RxActive and RxError are defined in *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05*. HostDisconnect is defined in *UTMI+ Specification Rev. 1.0*. A short definition is also given in the following subsections.

Table 14. Encoded USB event signals

Value	RxActive	RxError	HostDisconnect
00	0	0	0
01	1	0	0
11	1	1	0
10	X	X	1

RxActive: When the ISP1505 has detected a SYNC pattern on the USB bus, it signals an RxActive event to the link. An RxActive event can be communicated using two methods. The first method is for the ISP1505 to simultaneously assert DIR and NXT. The second method is for the ISP1505 to send an RXCMD to the link with the RxActive field in RxEvent bits set to logic 1. The link must be able to detect both methods. RxActive frames the receive packet from the first byte to the last byte.

The link must assume that RxActive is set to logic 0 when indicated in an RXCMD or when DIR is deasserted, whichever occurs first.

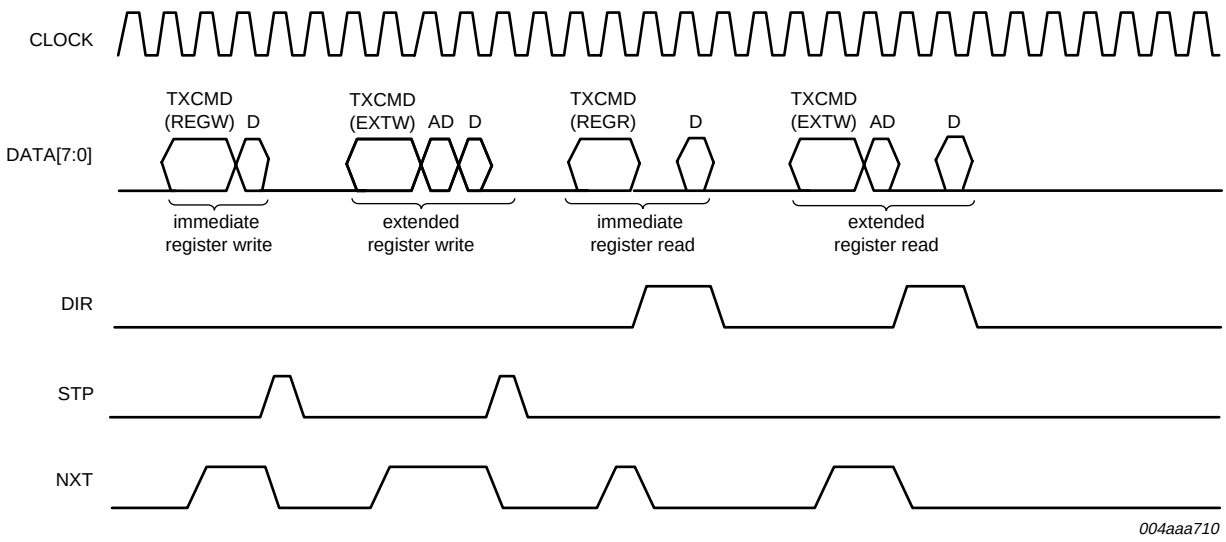
The link uses RxActive to time high-speed packets and ensure that bus turnaround times are met. For more information on the USB packet timing, see Section 9.8.1.

RxError: When the ISP1505 has detected an error while receiving a USB packet, it deasserts NXT and sends an RXCMD with the RxError field set to logic 1. The received packet is no longer valid and must be dropped by the link.

HostDisconnect: HostDisconnect is encoded into the RxEvent field of the RXCMD. HostDisconnect is valid only when the ISP1505 is configured as a host (both DP_PULLDOWN and DM_PULLDOWN are set to logic 1), and indicates to the host controller when a peripheral is connected or disconnected. The host controller must enable HostDisconnect by setting the HOST_DISCON_R and HOST_DISCON_F bits in the USB Interrupt Enable Rising Edge and USB Interrupt Enable Falling Edge registers, respectively. Changes in HostDisconnect will cause the PHY to send an RXCMD to the link with the updated value.

9.6 Register read and write operations

Figure 8 shows register read and write sequences. The ISP1505 supports immediate addressing and extended addressing register operations. Extended register addressing is optional for links. Note that register operations will be aborted if the ISP1505 unexpectedly asserts DIR during the operation. When a register operation is aborted, the link must retry until successful. For more information on register operations, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.



AD indicates the address byte, and D indicates the data byte.

Fig 8. Example of register write, register read, extended register write and extended register read

9.7 USB reset and high-speed detection handshake (chirp)

Figure 9 shows the sequence of events for USB reset and high-speed detection handshake (chirp). The sequence is shown for hosts and peripherals. Figure 9 does not show all RXCMD updates and timing is not to scale. The sequence is as follows:

1. USB reset: The host detects a peripheral attachment as low-speed if DM is HIGH and as full-speed if DP is HIGH. If a host detects a low-speed peripheral, it does not follow the remainder of this protocol. If a host detects a full-speed peripheral, it resets the peripheral by writing to the Function Control register and setting XCVRSELECT[1:0] = 00b (high-speed) and TERMSELECT = 0b, which drives SE0 on the bus (DP and DM connected to ground through 45 Ω). The host also sets OPMODE[1:0] = 10b for correct chirp transmit and receive. The start of SE0 is labeled T_0.

   Remark: To receive chirp signaling, the host must also consider the high-speed differential receiver output. The host controller must interpret LINESTATE[1:0] as shown in Table 11.

2. High-speed detection handshake (chirp)

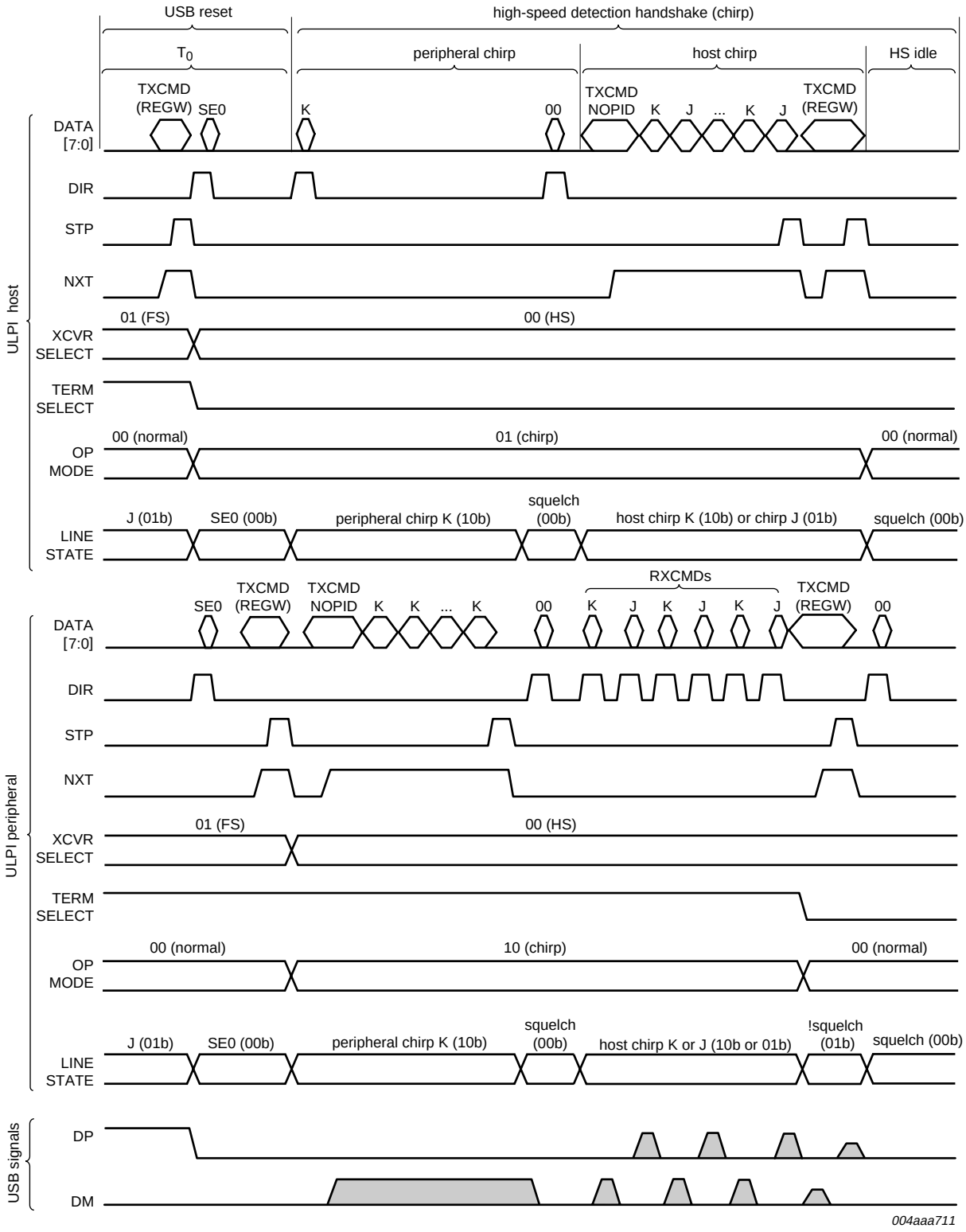
   a. Peripheral chirp: After detecting SE0 for no less than 2.5 µs, if the peripheral is capable of high-speed, it sets XCVRSELECT[1:0] = 00b (high-speed) and OPMODE[1:0] = 10b (chirp). The peripheral immediately follows this with a TXCMD (NOPID), transmitting a Chirp K for no less than 1 ms and ending no more

than 7 ms after reset time T_0. If the peripheral is in low-power mode, it must wake up its clock within 5.6 ms, leaving 200 µs for the link to start transmitting the Chirp K, and 1.2 ms for the Chirp K to complete (worst case with 10 % slow clock).

b. Host chirp: If the host does not detect the peripheral chirp, it must continue asserting SE0 until the end of reset. If the host detects the peripheral Chirp K for no less than 2.5 µs, then no more than 100 µs after the bus leaves the Chirp K state, the host sends a TXCMD (NOPID) with an alternating sequence of Chirp Ks and Js. Each Chirp K or Chirp J must last for no less than 40 µs and no longer than 60 µs.

c. High-speed idle: The peripheral must detect a minimum of Chirp K-J-K-J-K-J. Each Chirp K and Chirp J must be detected for at least 2.5 µs. After seeing that minimum sequence, the peripheral sets TERMSELECT = 0b and OPMODE[1:0] = 00b. The peripheral is now in high-speed mode and sees !squelch (01b on LINESTATE). When the peripheral sees squelch (10b on LINESTATE), it knows that the host has completed chirp and waits for Hi-Speed USB traffic to begin. After transmitting the chirp sequence, the host changes OPMODE[1:0] to 00b and begins sending USB packets.

For more information, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.



Timing is not to scale.

Fig 9. USB reset and high-speed detection handshake (chirp) sequence

9.8 USB packet transmit and receive

An example of a packet transmit and receive is shown in Figure 10. For details on USB packets, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*.

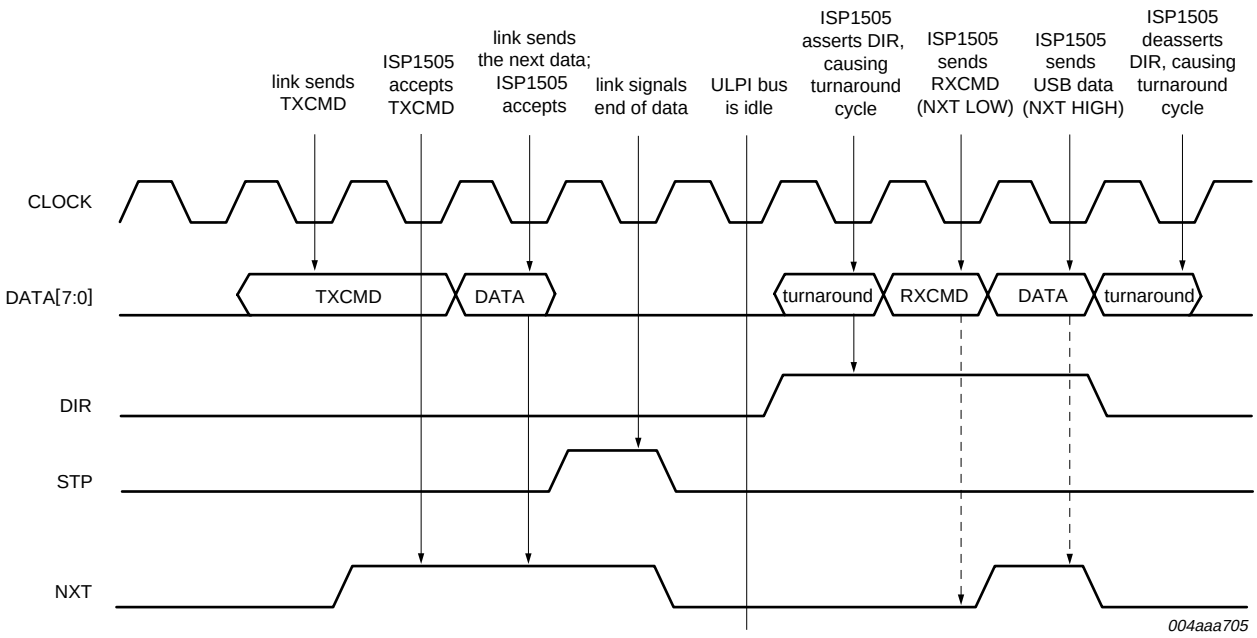


Fig 10. Example of using the ISP1505 to transmit and receive USB data

9.8.1 USB packet timing

9.8.1.1 ISP1505 pipeline delays

The ISP1505 delays are shown in Table 15. For a detailed description, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.2*.

Table 15. PHY pipeline delays

Parameter name	High-speed PHY delay	Full-speed PHY delay	Low-speed PHY delay
RXCMD delay (J and K)	4	4	4
RXCMD delay (SE0)	4	4 to 6	16 to 18
TX start delay	1 to 2	6 to 10	74 to 75
TX end delay (packets)	3 to 4	not applicable	not applicable
TX end delay (SOF)	6 to 9	not applicable	not applicable
RX start delay	5 to 6	not applicable	not applicable
RX end delay	5 to 6	17 to 18	122 to 123

9.8.1.2 Allowed link decision time

The amount of clock cycles allocated to the link to respond to a received packet and correctly receive back-to-back packets is given in Table 16. Link designs must follow values given in Table 16 for correct USB system operation. Examples of high-speed packet sequences and timing are shown in Figure 11 and Figure 12. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.2.6.3*.

Table 16. Link decision times

Packet sequence	High-speed link delay	Full-speed link delay	Low-speed link delay	Definition
Transmit-Transmit (host only)	15 to 24	7 to 18	77 to 247	Number of clock cycles a host link must wait before driving the TXCMD for the second packet. In high-speed, the link starts counting from the assertion of STP for the first packet. In full-speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the first packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Transmit (host or peripheral)	1 to 14	7 to 18	77 to 247	Number of clock cycles the link must wait before driving the TXCMD for the transmit packet. In high-speed, the link starts counting from the end of the receive packet; deassertion of DIR or an RXCMD, indicating RxActive is LOW. In full-speed or low-speed, the link starts counting from the RXCMD, indicating LINESTATE has changed from SE0 to J for the receive packet. The timing given ensures inter-packet delays of 2 bit times to 6.5 bit times.
Receive-Receive (peripheral only)	1	1	1	Minimum number of clock cycles between consecutive receive packets. The link must be able to receive both packets.
Transmit-Receive (host or peripheral)	92	80	718	Host or peripheral transmits a packet and will time-out after this number of clock cycles if a response is not received. Any subsequent transmission can occur after this time.

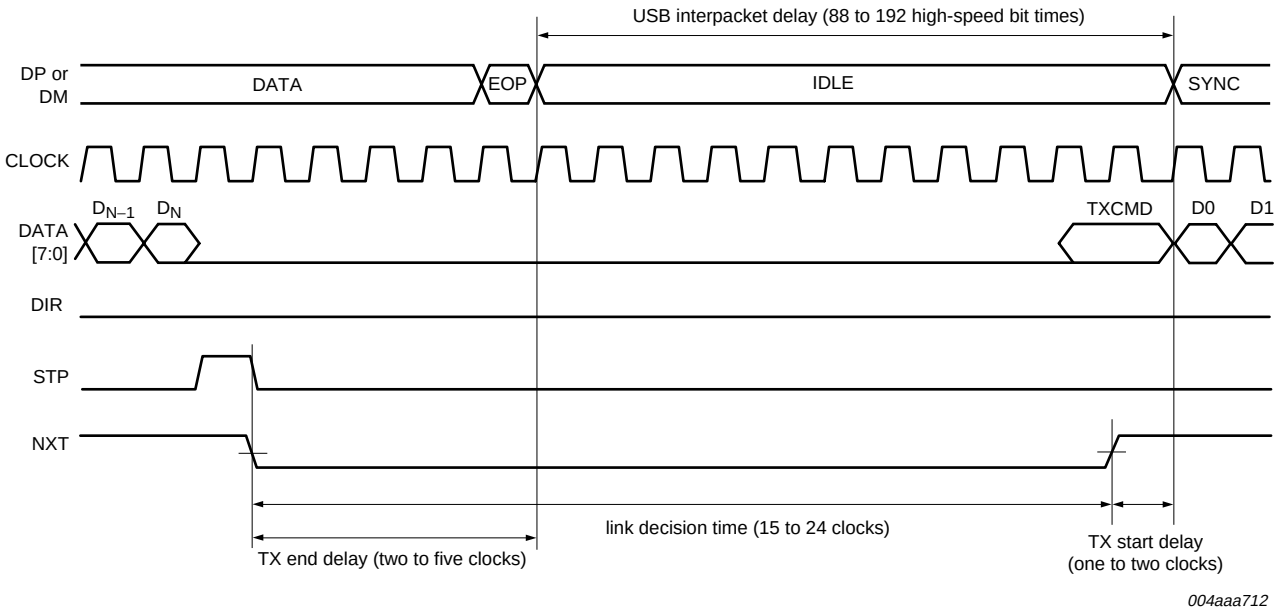


Fig 11. High-speed transmit-to-transmit packet timing

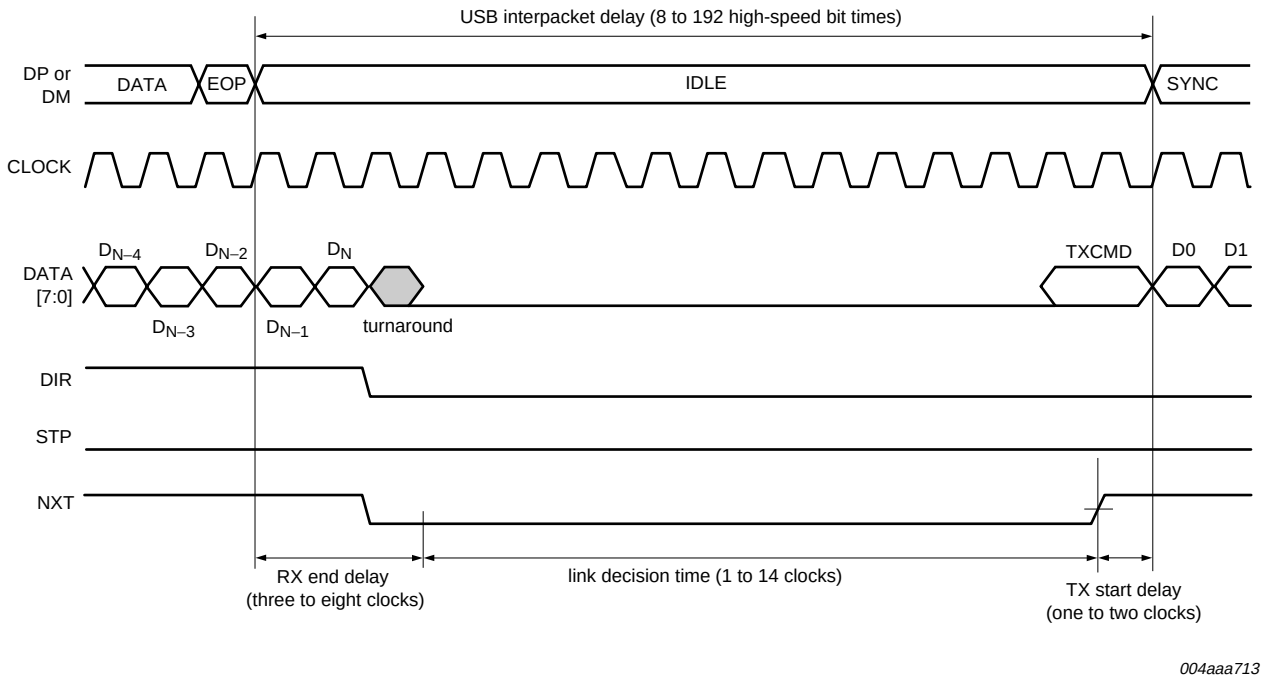
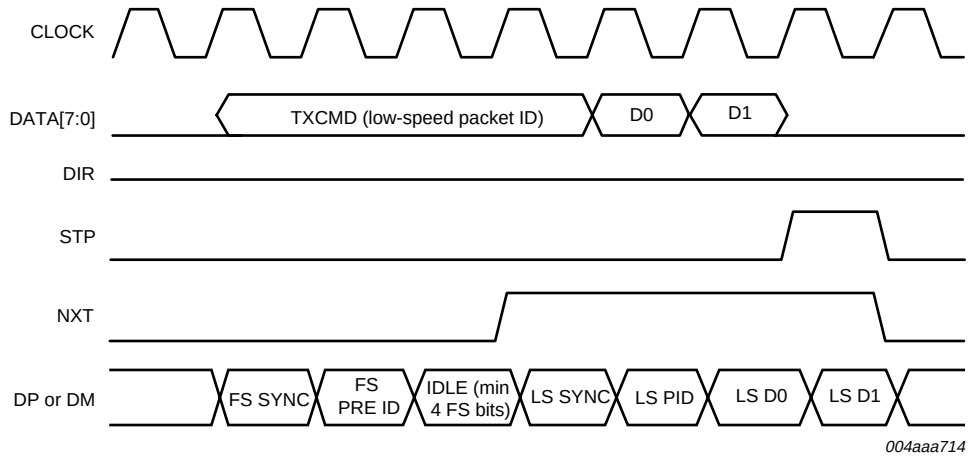


Fig 12. High-speed receive-to-transmit packet timing

9.9 Preamble

Preamble packets are headers to low-speed packets that must travel over a full-speed bus, between a host and a hub. To enter preamble mode, the link sets XCVRSELECT[1:0] = 11b in the Function Control register. When in preamble mode, the ISP1505 operates just as in full-speed mode, and sends all data with the full-speed rise time and fall time. Whenever the link transmits a USB packet in preamble mode, the ISP1505 will automatically send a preamble header at full-speed bit rate before sending the link packet at low-speed bit rate. The ISP1505 will ensure a minimum gap of four full-speed bit times between the last bit of the full-speed PRE PID and the first bit of the low-speed packet SYNC. The ISP1505 will drive a J for at least one full-speed bit time after sending the PRE PID, after which the pull-up resistor can hold the J state on the bus. An example transmit packet is shown in Figure 13.

In preamble mode, the ISP1505 can also receive low-speed packets from the full-speed bus.



DP and DM timing is not to scale.

Fig 13. Preamble sequence

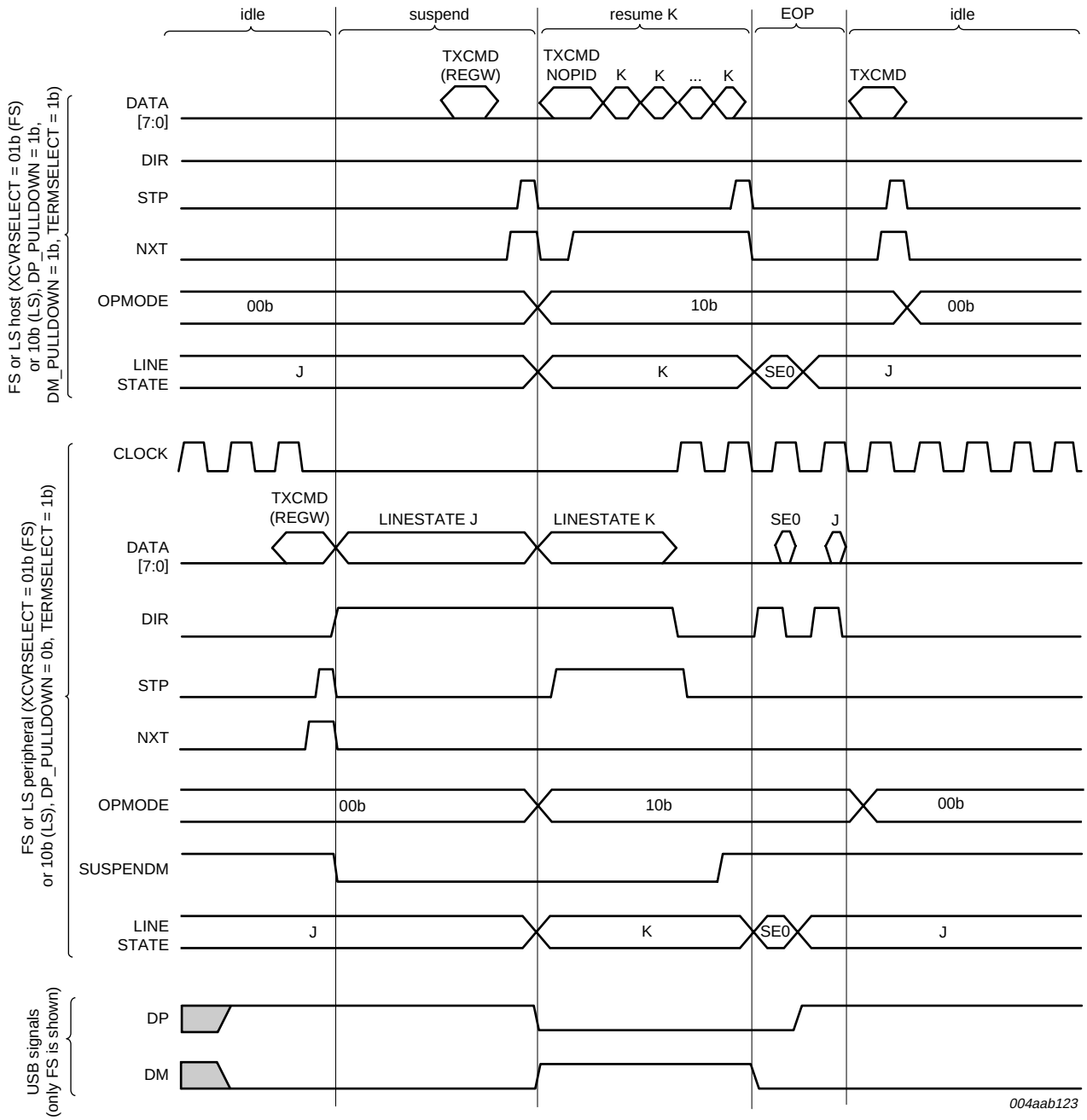
9.10 USB suspend and resume

9.10.1 Full-speed and low-speed host-initiated suspend and resume

Figure 14 illustrates how a host or a hub places a full-speed or low-speed peripheral into suspend and sometime later initiates resume signaling to wake up the downstream peripheral. Note that Figure 14 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events for a host and a peripheral, both with ISP1505, is as follows:

1. Idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations disabled (TERMSELECT is set to 1b). The peripheral has the 1.5 kΩ pull-up resistor connected to DP for full-speed or DM for low-speed (TERMSELECT is set to 1b).
2. Suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the PHY into low-power mode by clearing the SUSPENDM bit in the Function Control register, causing the PHY to draw only suspend current. The host may or may not be powered down.
3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE[1:0] to 10b and transmits a K for at least 20 ms. The peripheral link sees the resume K on LINESTATE, and asserts STP to wake up the PHY.
4. EOP: When STP is asserted, the ISP1505 on the host side automatically appends an EOP of two bits of SE0 at low-speed bit rate, followed by one bit of J. The ISP1505 on the host side knows to add the EOP because DP_PULLDOWN and DM_PULLDOWN are set to 1b for a host. After the EOP is completed, the host link sets OPMODE[1:0] to 00b for normal operation. The peripheral link sees the EOP and also resumes normal operation.



Timing is not to scale.

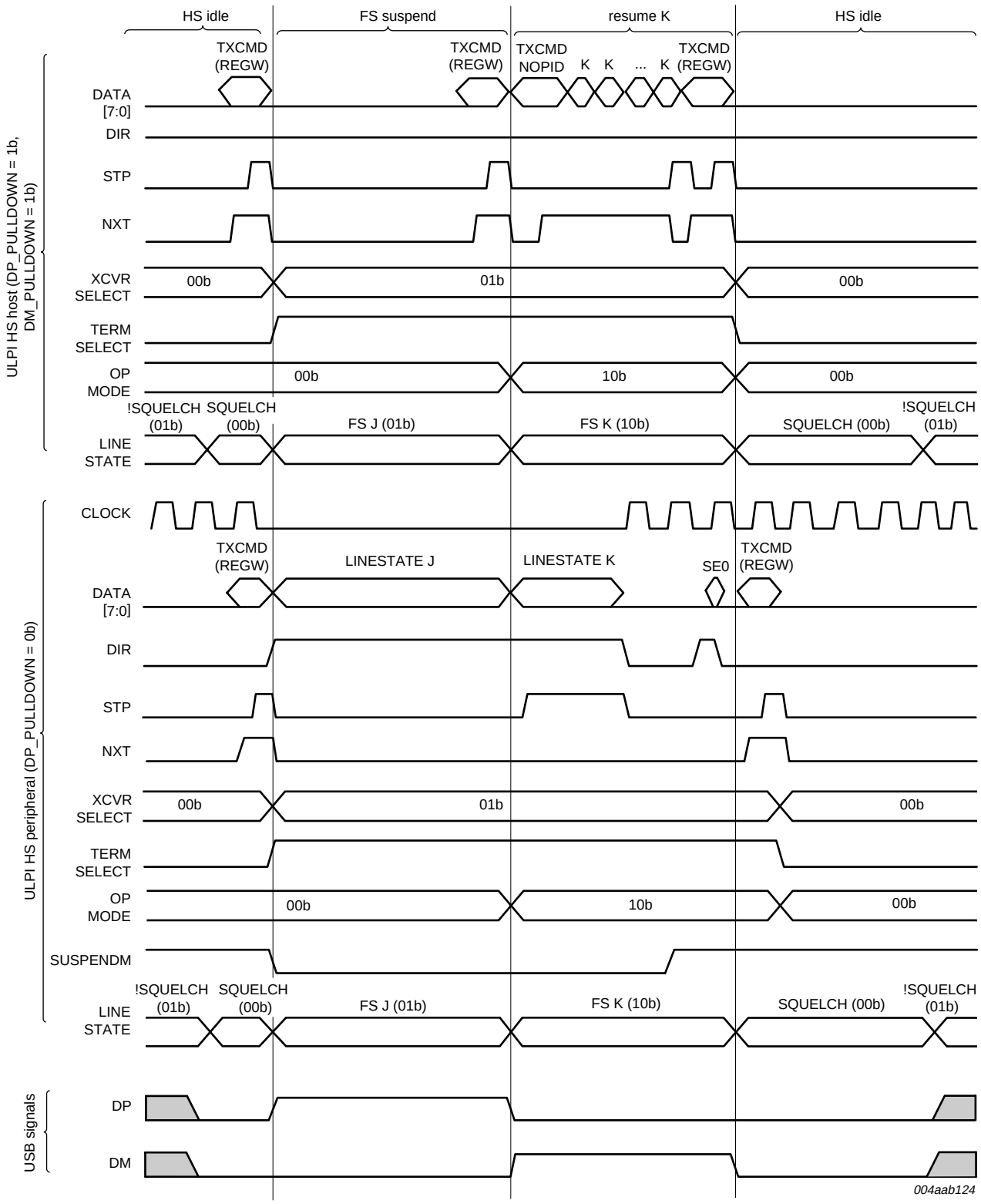
Fig 14. Full-speed suspend and resume

9.10.2 High-speed suspend and resume

Figure 15 illustrates how a host or a hub places a high-speed enabled peripheral into suspend and then initiates resume signaling. The high-speed peripheral will wake up and return to high-speed operations. Note that Figure 15 timing is not to scale, and does not show all RXCMD LINESTATE updates.

The sequence of events related to a host and a peripheral, both with ISP1505, is as follows:

1. High-speed idle: Initially, the host and the peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN and DM_PULLDOWN are set to 1b) and 45 Ω terminations enabled (TERMSELECT is set to 0b). The peripheral has its 45 Ω terminations enabled (TERMSELECT is set to 0b).
2. Full-speed suspend: When the peripheral sees no bus activity for 3 ms, it enters the suspend state. The peripheral link places the ISP1505 into full-speed mode (XCVRSELECT is set to 01b), removes 45 Ω terminations, and enables the 1.5 kΩ pull-up resistor on DP (TERMSELECT is set to 1b). The peripheral link then places the ISP1505 into low-power mode by clearing SUSPENDM, causing the ISP1505 to draw only suspend current. The host also changes the ISP1505 to full-speed (XCVRSELECT is set to 01b), removes 45 Ω terminations (TERMSELECT is set to 1b), and then may or may not be powered down.
3. Resume K: When the host wants to wake up the peripheral, it sets OPMODE to 10b and transmits a full-speed K for at least 20 ms. The peripheral link sees the resume K (10b) on LINESTATE, and asserts STP to wake up the ISP1505.
4. High-speed traffic: The host link sets high-speed (XCVRSELECT is set to 00b) and enables its 45 Ω terminations (TERMSELECT is set to 0b). The peripheral link sees SE0 on LINESTATE and also sets high-speed (XCVRSELECT is set to 00b), and enables its 45 Ω terminations (TERMSELECT is set to 0b). The host link sets OPMODE to 00b for normal high-speed operation.



Timing is not to scale.

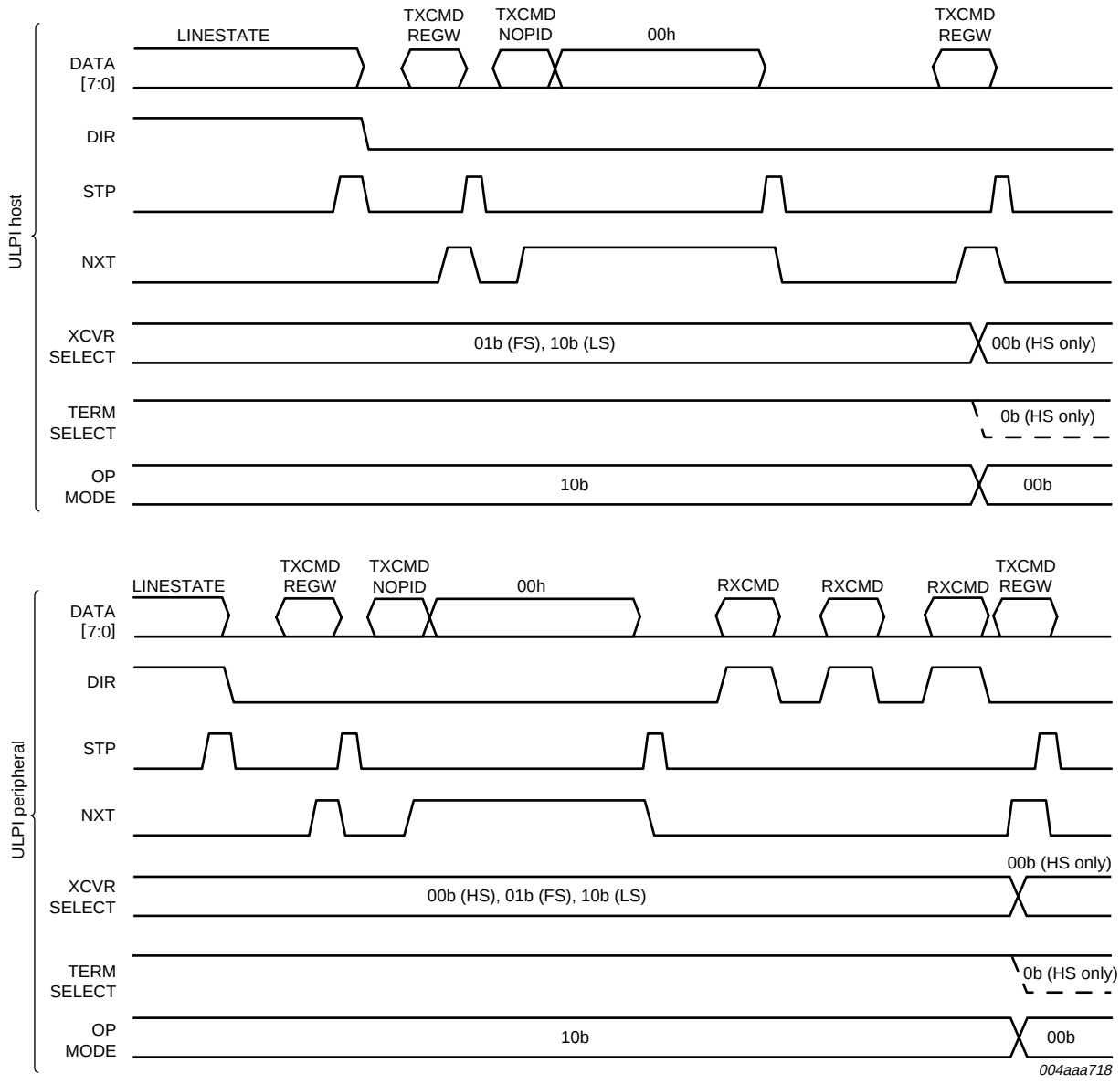
Fig 15. High-speed suspend and resume

9.10.3 Remote wake-up

The ISP1505 supports peripherals that initiate remote wake-up resume. When placed into USB suspend, the peripheral link remembers at what speed it was originally operating. Depending on the original speed, the link follows one of the protocols detailed here. In Figure 16, timing is not to scale, and not all RXCMD LINESTATE updates are shown.

The sequence of events related to a host and a peripheral, both with ISP1505, is as follows:

1. Both the host and the peripheral are assumed to be in low-power mode.
2. The peripheral begins remote wake-up by re-enabling its clock and setting its SUSPENDM bit to 1b.
3. The peripheral begins driving K on the bus to signal resume. Note that the peripheral link must assume that LINESTATE is K (01b) while transmitting because it will not receive any RXCMDs.
4. The host recognizes the resume, re-enables its clock and sets its SUSPENDM bit.
5. The host takes over resume driving within 1 ms of detecting the remote wake-up.
6. The peripheral stops driving resume.
7. The peripheral sees the host continuing to drive resume.
8. The host stops driving resume and the ISP1505 automatically adds the EOP to the end of resume. The peripheral recognizes the EOP as the end of resume.
9. Both the host and the peripheral revert to normal operation by writing 00b to OPMODE. If the host or the peripheral was previously in high-speed mode, it must revert to high-speed before the SE0 of the EOP is completed. This can be achieved by writing XCVRSELECT[1:0] = 00b and TERMSELECT = 0b after LINESTATE indicates SE0.



Timing is not to scale.

Fig 16. Remote wake-up from low-power mode

9.11 No automatic SYNC and EOP generation (optional)

This setting allows the link to turn off the automatic SYNC and EOP generation, and must be used for high-speed packets only. It is provided for backward compatibility with legacy controllers that include SYNC and EOP bytes in the data payload when transmitting packets. The ISP1505 will not automatically generate the SYNC and EOP patterns when OPMODE[1:0] is set to 11b. The ISP1505 will still NRZI encode data and perform bit stuffing. An example of a sequence is shown in Figure 17. The link must always send packets using the TXCMD (NOPID) type. The ISP1505 does not provide a mechanism to control bit stuffing in individual bytes, but will automatically turn off bit stuffing for EOP when STP is asserted with data set to FEh. If data is set to 00h when STP is asserted, the

PHY will not transmit any EOP. The ISP1505 will also detect if the PID byte is A5h, indicating an SOF packet, and automatically send a long EOP when STP is asserted. To transmit chirp and resume signaling, the link must set OPMODE[1:0] to 10b.

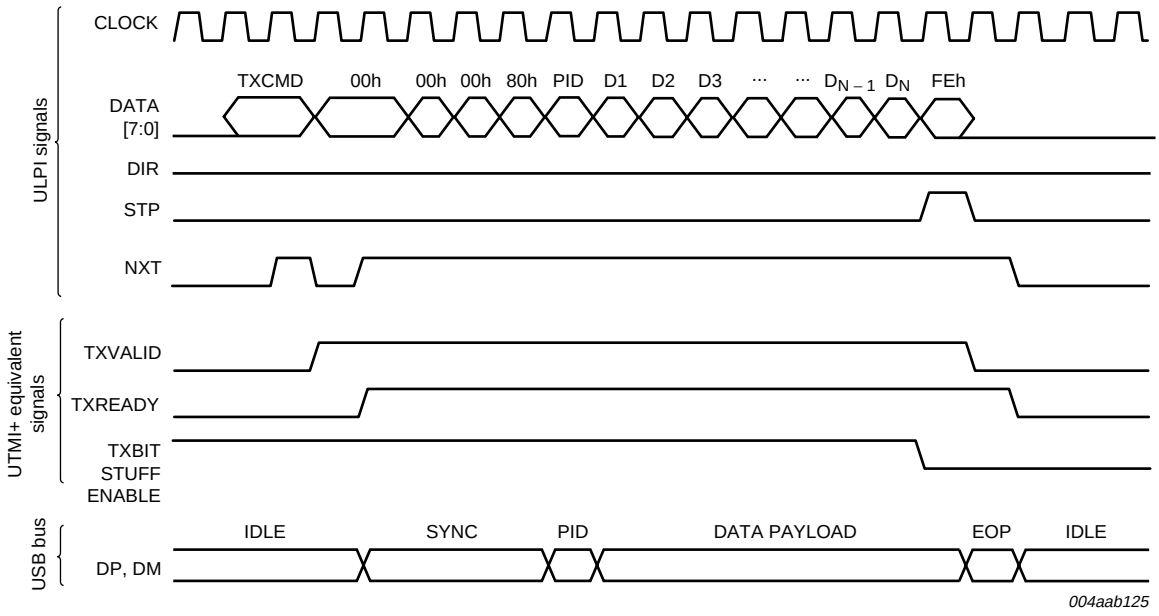


Fig 17. Transmitting USB packets without the automatic SYNC and EOP generation

9.12 On-The-Go operations

On-The-Go (OTG) is a supplement to *Universal Serial Bus Specification Rev. 2.0* that allows a portable USB device to assume the role of a limited USB host by defining improvements, such as a small connector and low power. Non-portable devices, such as standard hosts and embedded hosts, can also benefit from OTG features.

The ISP1505 OTG PHY is designed to support all the tasks specified in the OTG supplement. The ISP1505 provides the front-end analog support for Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices. The supporting components include:

- Voltage comparators
  - A_VBUS_VLD
  - SESS_VLD (session valid, can be used for both A-session and B-session valid)
  - SESS_END (session end)
- Pull-up and pull-down resistors on DP and DM
- Charge and discharge resistors on V_{BUS}

For complete OTG support, the system designer must add a V_{BUS} power supply and detect the value on the ID pin of the USB cable. This is not provided on the ISP1505.

The following subsections describe how to use the ISP1505 OTG components.

9.12.1 OTG comparators

The ISP1505 provides comparators that conform to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3* requirements of $V_{A\_VBUS\_VLD}$, $V_{A\_SESS\_VLD}$, $V_{B\_SESS\_VLD}$ and $V_{B\_SESS\_END}$. In this data sheet, $V_{A\_SESS\_VLD}$ and $V_{B\_SESS\_VLD}$ are combined into $V_{B\_SESS\_VLD}$. Comparators are described in Section 7.6. Changes in comparator values are communicated to the link by RXCMDs as described in Section 9.5.2.2. Control over comparators is described in Section 10.1.5 to Section 10.1.8.

9.12.2 Pull-up and pull-down resistors

The USB resistors on DP and DM can be used to initiate data-line pulsing SRP. The link must set the required bus state using mode settings given in Table 7.

9.12.3 V_{BUS} charge and discharge resistors

A pull-up resistor, $R_{UP(VBUS)}$, is provided to perform V_{BUS} pulsing SRP. A B-device is allowed to charge V_{BUS} above the session valid threshold to request the host to turn on the V_{BUS} power.

A pull-down resistor, $R_{DN(VBUS)}$, is provided for a B-device to discharge V_{BUS}. This is done whenever the A-device turns off the V_{BUS} power. The B-device can use the pull-down resistor to ensure V_{BUS} is below $V_{B\_SESS\_END}$ before starting a session.

For details, refer to *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*.

9.13 Serial modes

The ISP1505 supports both 6-pin serial mode and 3-pin serial mode, controlled by bits 6PIN_FSLS_SERIAL and 3PIN_FSLS_SERIAL of the Interface Control register. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.10*.

Figure 18 and Figure 19 provide examples of 6-pin serial mode and 3-pin serial mode, respectively.

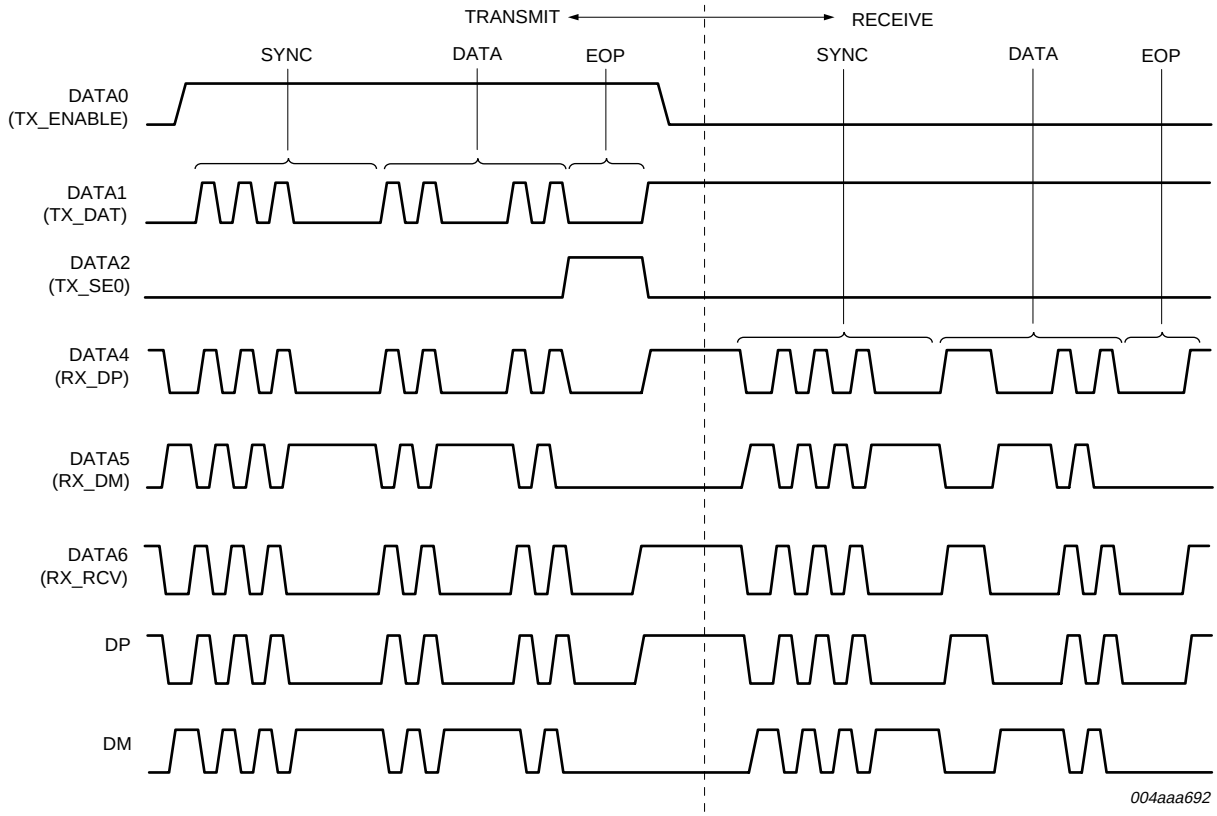


Fig 18. Example of transmit followed by receive in 6-pin serial mode

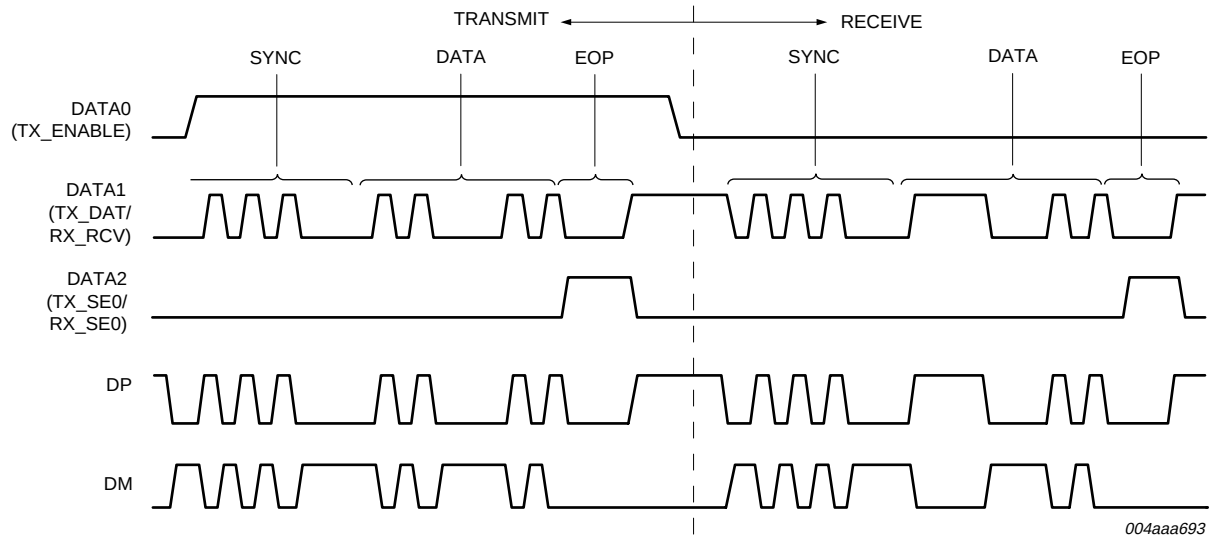


Fig 19. Example of transmit followed by receive in 3-pin serial mode

9.14 Aborting transfers

The ISP1505 supports aborting transfers on the ULPI bus. For details, refer to *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1, Section 3.8.4*.

9.15 Avoiding contention on the ULPI data bus

Because the ULPI data bus is bidirectional, avoid situations in which both the link and the PHY simultaneously drive the data bus.

The following points must be considered while implementing the data bus drive control on the link.

After power-up and clock stabilization, default states are as follows:

- The ISP1505 drives DIR to LOW.
- The data bus is input to the ISP1505.
- The ULPI link data bus is output, with all data bus lines driven to LOW.

When the ISP1505 wants to take control of the data bus to initiate a data transfer, it changes the DIR value from LOW to HIGH.

At this point, the link must disable its output buffers. This must be as fast as possible so the link must use a combinational path from DIR.

The ISP1505 will not immediately enable its output buffers, but will delay the enabling of its buffers until the next clock edge, avoiding bus contention.

When the data transfer is no longer required by the ISP1505, it changes DIR from HIGH to LOW and starts to immediately turn off its output drivers. The link senses the change of DIR from HIGH to LOW, but delays enabling its output buffers for one CLOCK cycle, avoiding data bus contention.

10. Register map

Table 17. Immediate register set overview

Field name	Size (bit)	Address (6 bit)				References
		R[1]	W[2]	S[3]	C[4]	
Immediate register set						
Vendor ID Low register	8	00h	-	-	-	Section 10.1.1 on page 44
Vendor ID High register	8	01h	-	-	-	
Product ID Low register	8	02h	-	-	-	
Product ID High register	8	03h	-	-	-	
Function Control register	8	04h to 06h	04h	05h	06h	Section 10.1.2 on page 44
Interface Control register	8	07h to 09h	07h	08h	09h	Section 10.1.3 on page 45
OTG Control register	8	0Ah to 0Ch	0Ah	0Bh	0Ch	Section 10.1.4 on page 46
USB Interrupt Enable Rising Edge register	8	0Dh to 0Fh	0Dh	0Eh	0Fh	Section 10.1.5 on page 47
USB Interrupt Enable Falling Edge register	8	10h to 12h	10h	11h	12h	Section 10.1.6 on page 48
USB Interrupt Status register	8	13h	-	-	-	Section 10.1.7 on page 48
USB Interrupt Latch register	8	14h	-	-	-	Section 10.1.8 on page 49
Debug register	8	15h	-	-	-	Section 10.1.9 on page 49
Scratch register	8	16h to 18h	16h	17h	18h	Section 10.1.10 on page 50
Reserved (do not use)	-	19h to 2Eh				Section 10.1.11 on page 50
Access extended register set	8	-	2Fh	-	-	Section 10.1.12 on page 50
Vendor-specific registers	8	30h to 3Ch				Section 10.1.13 on page 50
Power Control register	8	3Dh to 3Fh				Section 10.1.14 on page 50

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

Table 18. Extended register set overview

Field name	Size (bit)	Address (6 bit)				References
		R[1]	W[2]	S[3]	C[4]	
Maps to immediate register set above	8	00h to 3Fh				Section 10.2 on page 51
Reserved (do not use)	8	40h to FFh				

[1] Read (R): A register can be read. Read-only if this is the only mode given.

[2] Write (W): The pattern on the data bus will be written over all bits of a register.

[3] Set (S): The pattern on the data bus is OR-ed with and written to a register.

[4] Clear (C): The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

10.1 Immediate register set

10.1.1 Vendor ID and Product ID registers

10.1.1.1 Vendor ID Low register

Table 19 shows the bit description of the register.

Table 19. Vendor ID Low register (address R = 00h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_LOW[7:0]	R	CCh	**Vendor ID Low**: Lower byte of the NXP vendor ID supplied by USB-IF; has a fixed value of CCh

10.1.1.2 Vendor ID High register

The bit description of the register is given in Table 20.

Table 20. Vendor ID High register (address R = 01h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	VENDOR_ID_HIGH[7:0]	R	04h	**Vendor ID High**: Upper byte of the NXP vendor ID supplied by USB-IF; has a fixed value of 04h

10.1.1.3 Product ID Low register

The bit description of the Product ID Low register is given in Table 21.

Table 21. Product ID Low register (address R = 02h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_LOW[7:0]	R	05h	**Product ID Low**: Lower byte of the NXP product ID number; has a fixed value of 05h

10.1.1.4 Product ID High register

The bit description of the register is given in Table 22.

Table 22. Product ID High register (address R = 03h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	PRODUCT_ID_HIGH[7:0]	R	15h	**Product ID High**: Upper byte of the NXP product ID number; has a fixed value of 15h

10.1.2 Function Control register

This register controls UTMI function settings of the PHY. The bit allocation of the register is given in Table 23.

Table 23. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	SUSPENDM	RESET	OPMODE[1:0]		TERM SELECT	XCVRSELECT[1:0]	
Reset	0	1	0	0	0	0	0	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 24. Function Control register (address R = 04h to 06h, W = 04h, S = 05h, C = 06h) bit description

Bit	Symbol	Description
7	-	reserved
6	SUSPENDM	**Suspend LOW**: Active LOW PHY suspend. Places the PHY into low-power mode. The PHY will power down all blocks, except the full-speed receiver, OTG comparators and ULPI interface pins. To come out of low-power mode, the link must assert STP. The PHY will automatically clear this bit when it exits low-power mode. **0b —** Low-power mode **1b —** Powered (default)
5	RESET	**Reset**: Active HIGH transceiver reset. After the link sets this bit, the PHY will assert DIR and reset the digital core. This does not reset the ULPI interface or the ULPI register set. When reset is completed, the PHY will deassert DIR and automatically clear this bit, followed by an RXCMD update to the link. **0b —** Do not reset (default) **1b —** Reset The link must wait for DIR to deassert before using the ULPI bus. Does not reset the ULPI interface or the ULPI register set.
4 to 3	OPMODE[1:0]	**Operation Mode**: Selects the required bit-encoding style during transmit. **00b —** Normal operation (default) **01b —** Non-driving **10b —** Disable bit-stuffing and NRZI encoding **11b —** Do not automatically add SYNC and EOP when transmitting; must be used only for high-speed packets
2	TERMSELECT	**Termination Select**: Controls the internal 1.5 kΩ full-speed pull-up resistor and 45 Ω high-speed terminations. Control over bus resistors changes, depending on XCVRSELECT[1:0], OPMODE[1:0], DP_PULLDOWN and DM_PULLDOWN, as shown in Table 7.
1 to 0	XCVRSELECT[1:0]	**Transceiver Select**: Selects the required transceiver speed. **00b —** Enable the high-speed transceiver **01b —** Enable the full-speed transceiver **10b —** Enable the low-speed transceiver **11b —** Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)

10.1.3 Interface Control register

The Interface Control register enables alternative interfaces. All of these modes are optional features provided for legacy link cores. Setting more than one of these fields results in undefined behavior. Table 25 provides the bit allocation of the register.

Table 25. Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	INTF_ PROT_DIS	IND_PASS THRU	IND_ COMPL	reserved	CLOCK_ SUSPENDM	reserved	3PIN_FSLS _SERIAL	6PIN_FSLS _SERIAL
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 26. Interface Control register (address R = 07h to 09h, W = 07h, S = 08h, C = 09h) bit description

Bit	Symbol	Description
7	INTF_PROT_DIS	**Interface Protect Disable**: Controls circuitry built into the ISP1505 to protect the ULPI interface when the link 3-states STP and DATA[7:0]. When this bit is enabled, the ISP1505 will automatically detect when the link stops driving STP. **0b —** Enables the interface protect circuit (default). The ISP1505 attaches a weak pull-up resistor on STP. If STP is unexpectedly HIGH, the ISP1505 attaches weak pull-down resistors on DATA[7:0], protecting data inputs. **1b —** Disables the interface protect circuit, detaches weak pull-down resistors on DATA[7:0], and a weak pull-up resistor on STP.
6	IND_PASSTHRU	**Indicator Pass-through**: The ISP1505 does not support the qualification of an external FAULT with the internal $V_{A\_VBUS\_VLD}$ comparator. Either a digital FAULT is input on the V_{BUS}/FAULT pin or the V_{BUS} power is connected to the V_{BUS}/FAULT pin, not both. This bit must always be set to logic 1. **0b —** Not supported. **1b —** The complement output signal is not qualified with the internal A_VBUS_VLD comparator. The link must always set this bit to logic 1.
5	IND_COMPL	**Indicator Complement**: Informs the PHY to invert the FAULT input signal, generating the complement output. For details, see Section 9.5.2.2. **0b —** The ISP1505 will not invert the FAULT signal (default). **1b —** The ISP1505 will invert the FAULT signal.
4	-	reserved
3	CLOCK_SUSPENDM	**Clock Suspend LOW**: Active LOW clock suspend. Powers down the internal clock circuitry only. By default, the clock will not be powered in 6-pin serial mode or 3-pin serial mode. Valid only in 6-pin serial mode and 3-pin serial mode. Valid only when SUSPENDM is set to logic 1, otherwise this bit is ignored. **0b —** Clock will not be powered in 3-pin or 6-pin serial mode. **1b —** Clock will be powered in 3-pin and 6-pin serial modes.
2	-	reserved
1	3PIN_FSLS_SERIAL	**3-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 3-bit serial interface. The PHY will automatically clear this bit when 3-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 3-pin serial interface.
0	6PIN_FSLS_SERIAL	**6-Pin Full-Speed Low-Speed Serial Mode**: Changes the ULPI interface to a 6-bit serial interface. The PHY will automatically clear this bit when 6-pin serial mode is exited. **0b —** Full-speed or low-speed packets are sent using the parallel interface. **1b —** Full-speed or low-speed packets are sent using the 6-pin serial interface.

10.1.4 OTG Control register

This register controls various OTG functions of the ISP1505. The bit allocation of the OTG Control register is given in Table 27.

Table 27. OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USE_EXT_VBUS_IND	DRV_VBUS_EXT	DRV_VBUS	CHRG_VBUS	DISCHRG_VBUS	DM_PULLDOWN	DP_PULLDOWN	reserved
Reset	0	0	0	0	0	1	1	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 28. OTG Control register (address R = 0Ah to 0Ch, W = 0Ah, S = 0Bh, C = 0Ch) bit description

Bit	Symbol	Description
7	USE_EXT_VBUS_IND	**Use External V_{BUS} Indicator**: Informs the PHY to use an external V_{BUS} overcurrent indicator. **0b —** Use the internal OTG comparator. **1b —** Use the external V_{BUS} valid indicator signal input from the FAULT pin.
6	DRV_VBUS_EXT	**Drive V_{BUS} External**: Controls the external V_{BUS} supply through the RESET_N/PSW_N pin. **0b —** Do not drive PSW_N to LOW, disabling V_{BUS}. **1b —** Drive PSW_N to LOW, enabling V_{BUS}.
5	DRV_VBUS	**Drive V_{BUS}**: Signals the ISP1505 to drive 5 V on V_{BUS}. If DRV_VBUS_EXT is set to logic 1, then setting DRV_VBUS is optional.
4	CHRG_VBUS	**Charge V_{BUS}**: Charges V_{BUS} through a resistor. Used for the V_{BUS} pulsing SRP. The link must first check that V_{BUS} is discharged (see the DISCHRG_VBUS bit), and that both the DP and DM data lines have been LOW (SE0) for 2 ms. **0b —** Do not charge V_{BUS}. **1b —** Charge V_{BUS}.
3	DISCHRG_VBUS	**Discharge V_{BUS}**: Discharges V_{BUS} through a resistor. If the link sets this bit to logic 1, it waits for an RXCMD indicating that SESS_END has changed from 0 to 1, and then resets this bit to 0 to stop the discharge. **0b —** Do not discharge V_{BUS}. **1b —** Discharge V_{BUS}.
2	DM_PULLDOWN	**DM Pull Down**: Enables the 15 kΩ pull-down resistor on DM. **0b —** Pull-down resistor is not connected to DM. **1b —** Pull-down resistor is connected to DM.
1	DP_PULLDOWN	**DP Pull Down**: Enables the 15 kΩ pull-down resistor on DP. **0b —** Pull-down resistor is not connected to DP. **1b —** Pull-down resistor is connected to DP.
0	-	reserved; writing logic 1 will give undefined results

10.1.5 USB Interrupt Enable Rising Edge register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB Interrupt Status register change from logic 0 to logic 1. By default, all transitions are enabled. Table 29 shows the bit allocation of the register.

Table 29. USB Interrupt Enable Rising Edge register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END_R	SESS_VALID_R	VBUS_VALID_R	HOST_DISCON_R
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 30. USB Interrupt Enable Rising Edge register (address R = 0Dh to 0Fh, W = 0Dh, S = 0Eh, C = 0Fh) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END_R	**Session End Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_END.
2	SESS_VALID_R	**Session Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on SESS_VLD.
1	VBUS_VALID_R	**V_{BUS} Valid Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on A_VBUS_VLD.
0	HOST_DISCON_R	**Host Disconnect Rise**: Enables interrupts and RXCMDs for logic 0 to logic 1 transitions on HOST_DISCON.

10.1.6 USB Interrupt Enable Falling Edge register

The bits in this register enable interrupts and RXCMDs to be sent when the corresponding bits in the USB Interrupt Status register change from logic 1 to logic 0. By default, all transitions are enabled. See Table 31.

Table 31. USB Interrupt Enable Falling Edge register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END_F	SESS_VALID_F	VBUS_VALID_F	HOST_DISCON_F
Reset	0	0	0	1	1	1	1	1
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 32. USB Interrupt Enable Falling Edge register (address R = 10h to 12h, W = 10h, S = 11h, C = 12h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END_F	**Session End Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_END.
2	SESS_VALID_F	**Session Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on SESS_VLD.
1	VBUS_VALID_F	**V_{BUS} Valid Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on A_VBUS_VLD.
0	HOST_DISCON_F	**Host Disconnect Fall**: Enables interrupts and RXCMDs for logic 1 to logic 0 transitions on HOST_DISCON.

10.1.7 USB Interrupt Status register

This register (see Table 33) indicates the current value of the interrupt source signal.

Table 33. USB Interrupt Status register (address R = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END	SESS_VALID	VBUS_VALID	HOST_DISCON
Reset	X	X	X	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 34. USB Interrupt Status register (address R = 13h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END	**Session End**: Reflects the current value of the session end voltage comparator.
2	SESS_VALID	**Session Valid**: Reflects the current value of the session valid voltage comparator.
1	VBUS_VALID	**V_{BUS} Valid**: Reflects the current value of the V_{BUS} valid voltage comparator.
0	HOST_DISCON	**Host Disconnect**: Reflects the current value of the host disconnect detector.

10.1.8 USB Interrupt Latch register

The bits of the USB Interrupt Latch register are automatically set by the ISP1505 when an unmasked change occurs on the corresponding interrupt source signal. The ISP1505 will automatically clear all bits when the link reads this register, or when the PHY enters low-power mode.

Remark: It is optional for the link to read this register when the clock is running because all signal information will automatically be sent to the link through the RXCMD byte.

The bit allocation of this register is given in Table 35.

Table 35. USB Interrupt Latch register (address R = 14h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				SESS_END_L	SESS_VALID_L	VBUS_VALID_L	HOST_DISCON_L
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 36. USB Interrupt Latch register (address R = 14h) bit description

Bit	Symbol	Description
7 to 4	-	reserved
3	SESS_END_L	**Session End Latch**: Automatically set when an unmasked event occurs on SESS_END. Cleared when this register is read.
2	SESS_VALID_L	**Session Valid Latch**: Automatically set when an unmasked event occurs on SESS_VLD. Cleared when this register is read.
1	VBUS_VALID_L	**V_{BUS} Valid Latch**: Automatically set when an unmasked event occurs on A_VBUS_VLD. Cleared when this register is read.
0	HOST_DISCON_L	**Host Disconnect Latch**: Automatically set when an unmasked event occurs on HOST_DISCON. Cleared when this register is read.

10.1.9 Debug register

The bit allocation of the Debug register is given in Table 37. This register indicates the current value of signals useful for debugging.

Table 37. Debug register (address R = 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						LINE STATE1	LINE STATE0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 38. Debug register (address R = 15h) bit description

Bit	Symbol	Description
7 to 2	-	reserved
1	LINESTATE1	**Line State 1**: Contains the current value of LINESTATE 1
0	LINESTATE0	**Line State 0**: Contains the current value of LINESTATE 0

10.1.10 Scratch register

Table 39 shows the bit description of the Scratch register. It is an empty register for testing purposes.

Table 39. Scratch register (address R = 16h to 18h, W = 16h, S = 17h, C = 18h) bit description

Bit	Symbol	Access	Value	Description
7 to 0	SCRATCH [7:0]	R/W/S/C	00h	**Scratch**: This is an empty register byte for testing purposes. Software can read, write, set and clear this register. The functionality of the PHY will not be affected.

10.1.11 Reserved

Registers 19h to 2Eh are not implemented. Operating on these addresses will have no effect on the PHY.

10.1.12 Access extended register set

Address 2Fh does not contain register data. Instead it links to the extended register set. The immediate register set maps to the lower end of the extended register set.

10.1.13 Vendor-specific registers

Addresses 30h to 3Fh contain vendor-specific registers.

10.1.14 Power Control register

Table 40 provides the bit allocation of the Power Control register.

Table 40. Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved				BVALID_ FALL	BVALID_ RISE	reserved	IGNORE_ RESET
Reset	0	0	0	0	0	0	0	0
Access	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C	R/W/S/C

Table 41. Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description

Bit	Symbol	Description
7 to 4	-	reserved; the link must never write logic 1 to these bits.
3	BVALID_FALL	**BVALID Fall**: Enables RXCMDs for HIGH-to-LOW transitions on BVALID. When BVALID changes from HIGH to LOW, the ISP1505 will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. The session valid comparator should be used instead.
2	BVALID_RISE	**BVALID Rise**: Enables RXCMDs for LOW-to-HIGH transitions on BVALID. When BVALID changes from LOW to HIGH, the ISP1505 will send an RXCMD to the link with the ALT_INT bit set to logic 1. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. The session valid comparator should be used instead.
1	-	reserved
0	IGNORE_RESET	**Ignore Reset**: Selects between the RESET_N and PSW_N functions of the RESET_N/PSW_N pin. The link must set this bit to logic 1, if PSW_N is used in a ganged mode configuration. **0b —** The RESET_N/PSW_N pin behaves as an active-LOW reset input (RESET_N). This is the default setting. **1b —** The RESET_N/PSW_N pin behaves as an active-LOW power switch output (PSW_N).

10.2 Extended register set

Addresses 00h to 3Fh of the extended register set directly map to the immediate set. This means a read, write, set or clear operation to these extended addresses will operate on the immediate register set.

Addresses 40h to FFh are not implemented. Operating on these addresses may result in undefined behavior of the PHY.

11. ElectroStatic Discharge (ESD)

11.1 ESD protection

The pins that are connected to the USB connector (DP, DM, V_{BUS} and GND) have a minimum of ±4 kV ESD protection. Capacitors 0.1 µF and 1 µF must be connected in parallel from V_{BUS} to GND to achieve this ±4 kV ESD protection (see Figure 20).

Remark: Capacitors 0.1 µF and 1 µF are also required by *Universal Serial Bus Specification Rev. 2.0*. For details on the requirements for C_{VBUS}, see Section 16.

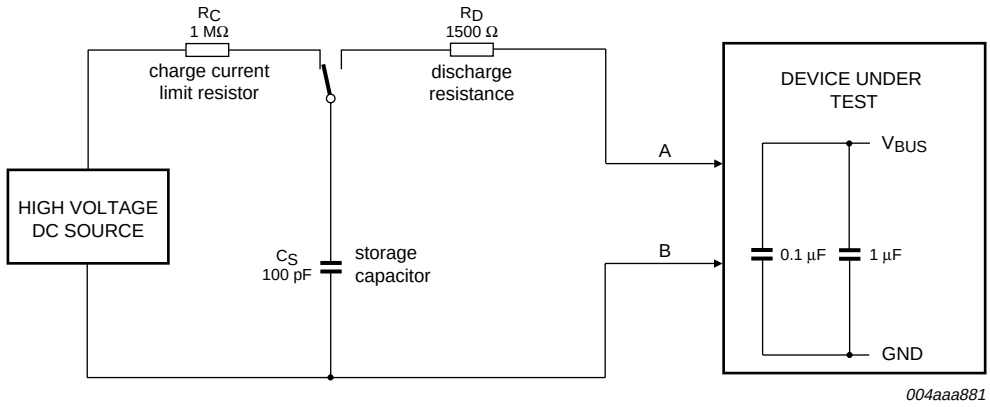


Fig 20. Human body ESD test model

11.2 ESD test conditions

A detailed report on test setup and results is available on request.

12. Limiting values

Table 42. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage	on pins STP, DATA[7:0] and RESET_N/PSW_N		–0.5	$V_{CC(I/O)}$ + 0.5	V
		on pin V_{BUS}/FAULT		–0.5	+6.0	V
		on pin XTAL1		–0.5	+2.5	V
		on pins DP and DM	[1]	–0.5	+4.6	V
V_{ESD}	electrostatic discharge voltage	on pins DP, DM, V_{BUS} and GND; I_{LI} < 1 µA	[2]	–4	+4	kV
		on all other pins; I_{LI} < 1 µA		–2	+2	kV
I_{lu}	latch-up current			–100	+100	mA
V_{lu}	latch-up voltage			-	4.6	V
T_{stg}	storage temperature			–40	+125	°C

[1] The ISP1505 has been tested according to the additional requirements listed in *Universal Serial Bus Specification Rev. 2.0, Section 7.1.1*. The short circuit withstand test and the AC stress test were performed for 24 hours, and the ISP1505 was found to be fully operational after the test completed.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model JESD22-A114D).

13. Recommended operating conditions

Table 43. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			3.0	3.3	3.6	V
$V_{CC(I/O)}$	input/output supply voltage		[1]	1.65	-	3.6	V
V_I	input voltage	on pins STP, DATA[7:0] and RESET_N/PSW_N		0	-	$V_{CC(I/O)}$	V
		on pin V_{BUS}/FAULT		0	-	5.5	V
		on pins DP and DM		0	-	3.6	V
		on pin XTAL1		0	-	1.95	V
T_{amb}	ambient temperature			–40	+25	+85	°C
T_j	junction temperature			–40	-	+125	°C

[1] $V_{CC(I/O)}$ must be less than or equal to V_{CC}.

14. Static characteristics

Table 44. Static characteristics: supply pins

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(REG3V3)}$	voltage on pin REG3V3			3.0	3.3	3.6	V
$V_{(REG1V8)}$	voltage on pin REG1V8			1.65	1.8	1.95	V
$V_{POR(trip)}$	power-on reset trip voltage			1.0	-	1.5	V
I_{CC}	supply current	low-power mode; V_{BUS} valid detector disabled; 1.5 kΩ pull-up resistor on pin DP disconnected		-	30	85	µA
		low-power mode; V_{BUS} valid detector disabled; 1.5 kΩ pull-up resistor on pin DP connected		-	215	280	µA
		full-speed idle; no USB activity		-	10	-	mA
		high-speed idle; no USB activity		-	19	-	mA
		full-speed continuous data transmit; 50 pF load on pins DP and DM	[1]	-	15	-	mA
		full-speed continuous data receive	[1]	-	11	-	mA
		high-speed continuous data transmit; 45 Ω load on pins DP and DM to ground	[1]	-	48	-	mA
		high-speed continuous data receive	[1]	-	28	-	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	static current; I/O pins are idle		-	-	1	µA

[1] A continuous stream of 1 kB packets with minimum inter-packet gap and all data bits set to logic 0 for continuous toggling.

Table 45. Static characteristics: digital pins (CLOCK, DIR, STP, NXT, DATA[7:0], RESET_N/PSW_N)

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3 \times V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.7 \times V_{CC(I/O)}$	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{CC(I/O)}$	-	-	1	µA
I_{LI}	input leakage current		−1	+0.1	+1	µA
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = +2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	$V_{CC(I/O)} - 0.4$	-	-	V
I_{OH}	HIGH-level output current	$V_O = V_{CC(I/O)} - 0.4$ V	−4.8	-	-	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	4.2	-	-	mA
I_{OZ}	off-state output current	$0 V < V_O < V_{CC(I/O)}$	-	-	1	µA

Table 45. Static characteristics: digital pins (CLOCK, DIR, STP, NXT, DATA[7:0], RESET_N/PSW_N) *...continued*

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Impedance						
Z_L	load impedance		45	-	65	Ω
Pull-up and pull-down						
I_{pd}	pull-down current	interface protect enabled; DATA[7:0] pins only; $V_I = V_{CC(I/O)}$	25	50	90	µA
I_{pu}	pull-up current	interface protect enabled; STP pin only; V_I = 0 V	–30	–50	–80	µA
Capacitance						
C_{in}	input capacitance	pins STP, RESET_N, DATA[7:0]	-	-	3.5	pF

Table 46. Static characteristics: pin V_{BUS}/FAULT

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Applicable only when pin V_{BUS}/FAULT is used as FAULT.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	µA
I_{IH}	HIGH-level input current	$V_I = V_{CC(I/O)}$	-	-	1	µA

Table 47. Static characteristics: analog I/O pins (DP, DM)

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Original USB transceiver (low-speed and full-speed)						
Input levels (differential receiver)						
V_{DI}	differential input sensitivity voltage	$\lvert V_{DP} - V_{DM} \rvert$	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	pull-up on pin DP; R_L = 1.5 kΩ to 3.6 V	0.0	0.18	0.3	V
V_{OH}	HIGH-level output voltage	pull-down on pins DP and DM; R_L = 15 kΩ to GND	2.8	3.2	3.6	V

Table 47. Static characteristics: analog I/O pins (DP, DM) *…continued*

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Termination							
V_{TERM}	termination voltage for upstream facing port pull-up	for 1.5 kΩ pull-up resistor		3.0	-	3.6	V
Resistance							
$R_{UP(DP)}$	pull-up resistance on pin DP			1425	1500	1575	Ω
High-speed USB transceiver							
Input levels (differential receiver)							
V_{HSSQ}	high-speed squelch detection threshold voltage (differential signal amplitude)			100	-	150	mV
V_{HSDSC}	high-speed disconnect detection threshold voltage (differential signal amplitude)			525	-	625	mV
V_{HSDI}	high-speed differential input sensitivity	$\lvert V_{DP} - V_{DM} \rvert$		300	-	-	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)	includes V_{DI} range		−50	-	+500	mV
V_{HSOI}	high-speed idle level voltage			−10	-	+10	mV
V_{HSOL}	high-speed data signaling LOW-level voltage			−10	-	+10	mV
Output levels							
V_{HSOH}	high-speed data signaling HIGH-level voltage			360	-	440	mV
V_{CHIRPJ}	Chirp J level (differential voltage)			700	-	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)			−900	-	−500	mV
Leakage current							
I_{LZ}	off-state leakage current			−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	5	pF
Resistance							
$R_{DN(DP)}$	pull-down resistance on pin DP			14.25	15	15.75	kΩ
$R_{DN(DM)}$	pull-down resistance on pin DM			14.25	15	15.75	kΩ
Termination							
$Z_{O(drv)(DP)}$	driver output impedance on pin DP	steady-state drive	[1]	40.5	45	49.5	Ω
$Z_{O(drv)(DM)}$	driver output impedance on pin DM	steady-state drive	[1]	40.5	45	49.5	Ω
Z_{INP}	input impedance exclusive of pull-up/pull-down (for low-/full-speed)			10	-	-	MΩ

[1] For high-speed USB and full-speed USB.

Table 48. Static characteristics: V_{BUS} comparators

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	4.5	4.65	V
$V_{B\_SESS\_VLD}$	B-device session valid voltage	for A-device and B-device	0.8	1.6	2.0	V
$V_{hys(B\_SESS\_VLD)}$	B-device session valid hysteresis voltage		70	140	200	mV
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	0.5	0.8	V

Table 49. Static characteristics: V_{BUS} resistors

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to pin REG3V3 when CHRG_VBUS is logic 1	281	680	-	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when DISCHRG_VBUS is logic 1	656	850	-	Ω
$R_{I(idle)(VBUS)}$	idle input resistance on pin V_{BUS}		40	57	80	kΩ

Table 50. Static characteristics: resistor reference

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(RREF)}$	output voltage on pin RREF	SUSPENDM is logic 1	-	1.22	-	V

15. Dynamic characteristics

Table 51. Dynamic characteristics: reset and clock

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.
Typical values are at V_{CC} = 3.3 V; $V_{CC(I/O)}$ = 3.3 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset							
$t_{W(POR)}$	internal power-on reset pulse width			0.2	-	-	µs
$t_{w(REG1V8\_H)}$	REG1V8 HIGH pulse width			2	-	-	µs
$t_{w(REG1V8\_L)}$	REG1V8 LOW pulse width			11	-	-	µs
$t_{W(RESET\_N)}$	external RESET_N pulse width			200	-	-	ns
t_{PWRUP}	regulator start-up time	4.7 µF ± 20 % capacitor each on pins REG1V8 and REG3V3		-	-	1	ms
Crystal or clock applied to XTAL1							
$f_{i(XTAL1)}$	input frequency on pin XTAL1	ISP1505ABS		-	19.2	-	MHz
		ISP1505CBS		-	26	-	MHz
$t_{jit(i)(XTAL1)RMS}$	RMS input jitter on pin XTAL1	ISP1505ABS		-	-	200	ps
		ISP1505CBS		-	-	300	ps
$\delta_{i(XTAL1)}$	input duty cycle on pin XTAL1	applicable only when clock is applied on pin XTAL1	[1]	-	50	-	%
$\Delta f_{i(XTAL1)}$	input frequency tolerance on pin XTAL1			-	50	200	ppm
$t_{r(XTAL1)}$	rise time on pin XTAL1	only for square wave input		-	-	5	ns
$t_{f(XTAL1)}$	fall time on pin XTAL1	only for square wave input		-	-	5	ns
$V_{(XTAL1)(p-p)}$	peak-to-peak voltage on pin XTAL1	only for square wave input		0.566	-	1.95	V
Output CLOCK characteristics							
$f_{o(CLOCK)}$	output frequency on pin CLOCK			-	60	-	MHz
$t_{jit(o)(CLOCK)RMS}$	RMS output jitter on pin CLOCK			-	-	500	ps
$\delta_{o(CLOCK)}$	output clock duty cycle on pin CLOCK			45	50	55	%
$t_{startup(PLL)}$	PLL startup time			-	650	-	µs
$t_{startup(o)(CLOCK)}$	output CLOCK start-up time	measured from power good or assertion of pin STP		450	650	900	µs

[1] The internal PLL is triggered only on the positive edge from the crystal oscillator. Therefore, the duty cycle is not critical.

Table 52. Dynamic characteristics: digital I/O pins

V_{CC} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 V to 1.95 V						
$t_{su(DATA)}$	DATA set-up time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	5.7	-	-	ns
$t_{h(DATA)}$	DATA hold time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	0	-	-	ns

Table 52. Dynamic characteristics: digital I/O pins *...continued*

V_{CC} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(DATA)}$	DATA output delay with respect to the rising edge of pin CLOCK	20 pF total external load per pin	-	-	7.8	ns
$t_{su(STP)}$	STP set-up time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	4.5	-	-	ns
$t_{h(STP)}$	STP hold time with respect to the rising edge of pin CLOCK	20 pF total external load per pin	0	-	-	ns
$t_{d(DIR)}$	DIR output delay with respect to the rising edge of pin CLOCK	20 pF total external load per pin	-	-	8.9	ns
$t_{d(NXT)}$	NXT output delay with respect to the rising edge of pin CLOCK	20 pF total external load per pin	-	-	8.9	ns
$V_{CC(I/O)}$ = 3.0 V to 3.6 V						
$t_{su(DATA)}$	DATA set-up time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	3.3	-	-	ns
$t_{h(DATA)}$	DATA hold time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	0.8	-	-	ns
$t_{d(DATA)}$	DATA output delay with respect to the rising edge of pin CLOCK	30 pF total external load per pin	-	-	5.5	ns
$t_{su(STP)}$	STP set-up time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	3.4	-	-	ns
$t_{h(STP)}$	STP hold time with respect to the rising edge of pin CLOCK	30 pF total external load per pin	0.8	-	-	ns
$t_{d(DIR)}$	DIR output delay with respect to the rising edge of pin CLOCK	30 pF total external load per pin	-	-	6.6	ns
$t_{d(NXT)}$	NXT output delay with respect to the rising edge of pin CLOCK	30 pF total external load per pin	-	-	6.6	ns

Table 53. Dynamic characteristics: analog I/O pins (DP, DM)

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed driver						
t_{HSR}	rise time (10 % to 90 %)		500	-	-	ps
t_{HSF}	fall time (10 % to 90 %)		500	-	-	ps
Full-speed driver						
t_{FR}	rise time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	excluding the first transition from the idle state	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state	1.3	-	2.0	V
Low-speed driver						
t_{LR}	transition time: rise time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns

Table 53. Dynamic characteristics: analog I/O pins (DP, DM) *…continued*

V_{CC} = 3.0 V to 3.6 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LF}	transition time: fall time	C_L = 200 pF to 600 pF; 1.5 kΩ pull-up on pin DM enabled; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRFM}	rise and fall time matching	t_{LR}/t_{LF}; excluding the first transition from the idle state	80	-	125	%
Driver timing						
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	TX_DAT, TX_SE0 to DP, DM; see Figure 22	-	-	11	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	TX_DAT, TX_SE0 to DP, DM; see Figure 22	-	-	11	ns
t_{PHZ}	driver disable delay from HIGH level	TX_ENABLE to DP, DM; see Figure 23	-	-	12	ns
t_{PLZ}	driver disable delay from LOW level	TX_ENABLE to DP, DM; see Figure 23	-	-	12	ns
t_{PZH}	driver enable delay to HIGH level	TX_ENABLE to DP, DM; see Figure 23	-	-	20	ns
t_{PZL}	driver enable delay to LOW level	TX_ENABLE to DP, DM; see Figure 23	-	-	20	ns
Receiver timing						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 24	-	-	17	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 24	-	-	17	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 24	-	-	17	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to RX_RCV, RX_DP and RX_DM; see Figure 24	-	-	17	ns

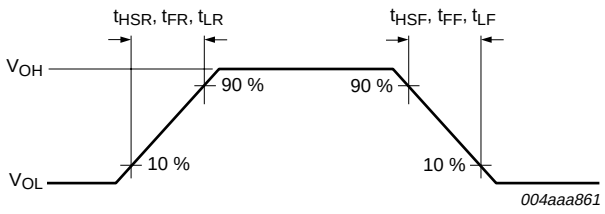


Fig 21. Rise time and fall time

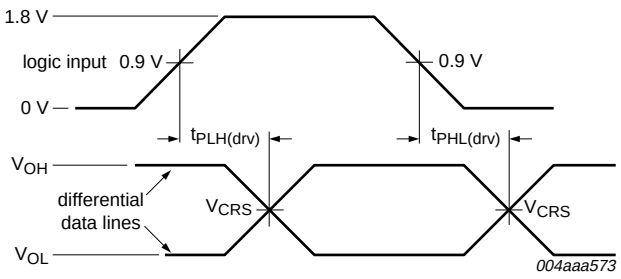


Fig 22. Timing of TX_DAT and TX_SE0 to DP and DM

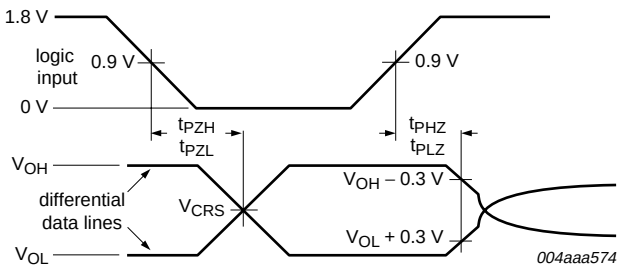


Fig 23. Timing of TX_ENABLE to DP and DM

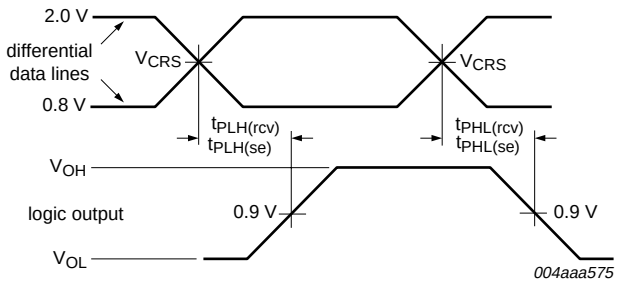


Fig 24. Timing of DP and DM to RX_RCV, RX_DP and RX_DM

15.1 ULPI timing

ULPI interface timing requirements are given in Figure 25. This timing applies to synchronous mode only. All timing is measured with respect to the ISP1505 CLOCK pin. All signals are clocked on the rising edge of CLOCK.

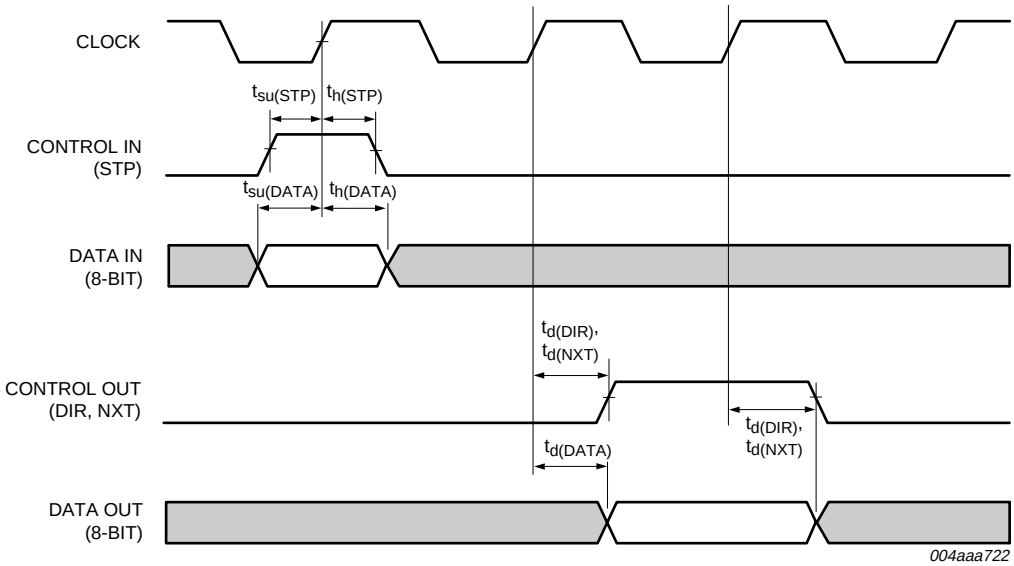


Fig 25. ULPI interface timing

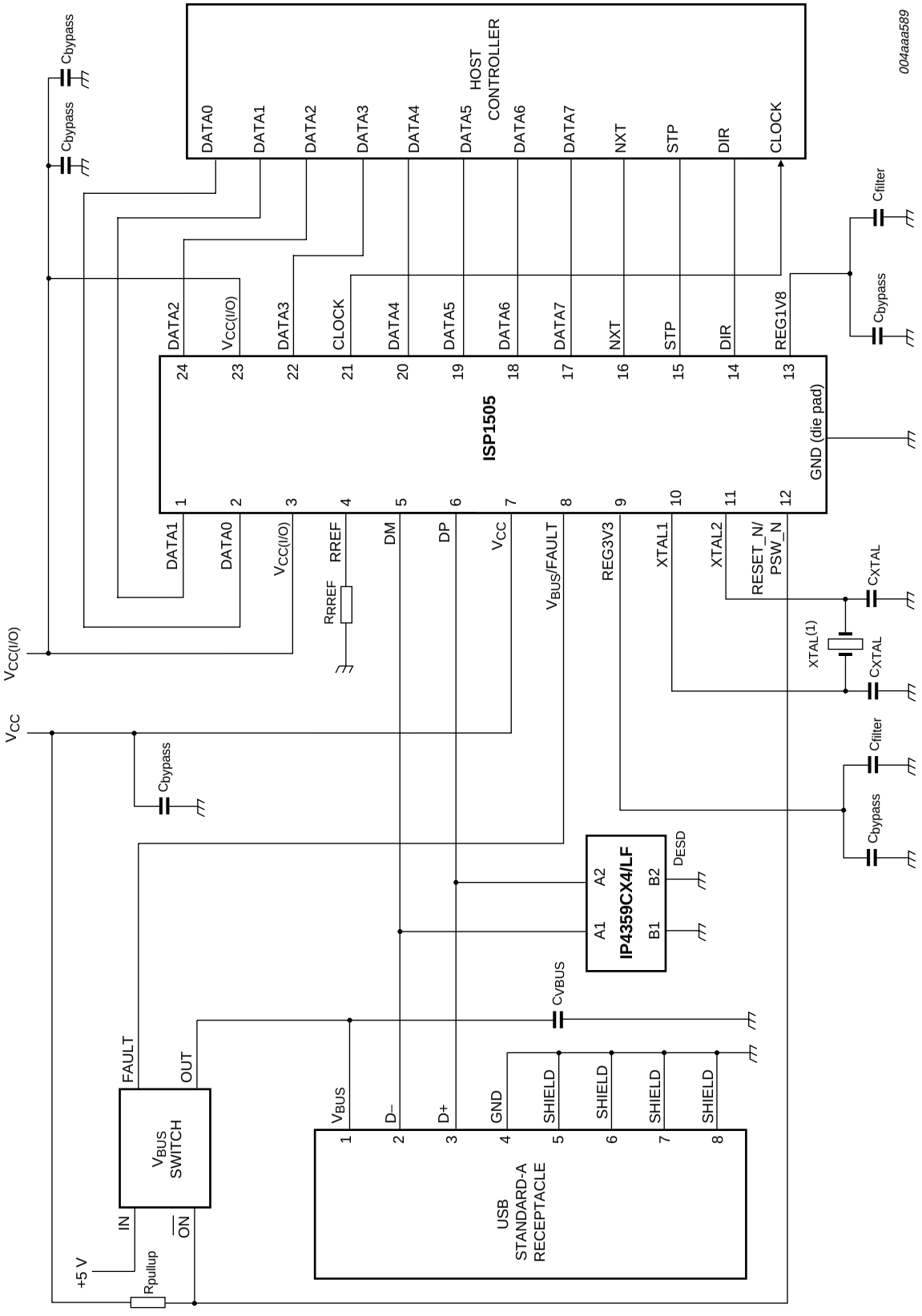
16. Application information

Table 54. Recommended bill of materials

Designator[1]	Application	Value	Comment
C_{bypass}	highly recommended for all applications	0.1 µF	-
C_{filter}	highly recommended for all applications	4.7 µF ± 20 %; use a LOW ESR capacitor (0.2 Ω to 2 Ω) for best performance	-
C_{VBUS}	mandatory for peripherals	0.1 µF and 1 µF to 10 µF in parallel	-
	mandatory for host	0.1 µF and 120 µF ± 20 % (min) in parallel	-
	mandatory for OTG	0.1 µF and 1 µF to 6.5 µF in parallel	-
D_{ESD}	recommended for all ESD-sensitive applications	-	IP4359CX4/LF; Wafer-Level Chip-Scale Package (WLCSP); ESD IEC 61000-4-2 level 4; ±15 kV contact; ±15 kV air discharge compliant protection
R_{pullup}	recommended; for applications with an external V_{BUS} supply controlled by PSW_N	4.7 kΩ (recommended)	maximum value is determined by the voltage drop on PSW_N caused by leakage into PSW_N and the external supply control pin
R_{RREF}	mandatory in all applications	12 kΩ ± 1 %	-
R_{VBUS}	strongly recommended for peripheral or external 5 V applications only	1 kΩ ± 5 %	-
R_{XTAL}	required only for applications driving a square wave into the XTAL1 pin	47 kΩ ± 5 %	used to avoid floating input on the XTAL1 pin
XTAL	crystal is used	19.2 MHz	C_L = 10 pF; R_S < 220 Ω; C_{XTAL} = 18 pF
		26 MHz	C_L = 10 pF; R_S < 130 Ω; C_{XTAL} = 18 pF
		-	CSTCE26M0XK2***-R0[2] C_{XTAL} is not required
$C_{(XTAL)SQ}$	required only for applications driving a square wave into the XTAL1 pin that has a DC offset	100 pF	used to AC couple the input square wave to the XTAL1 pin

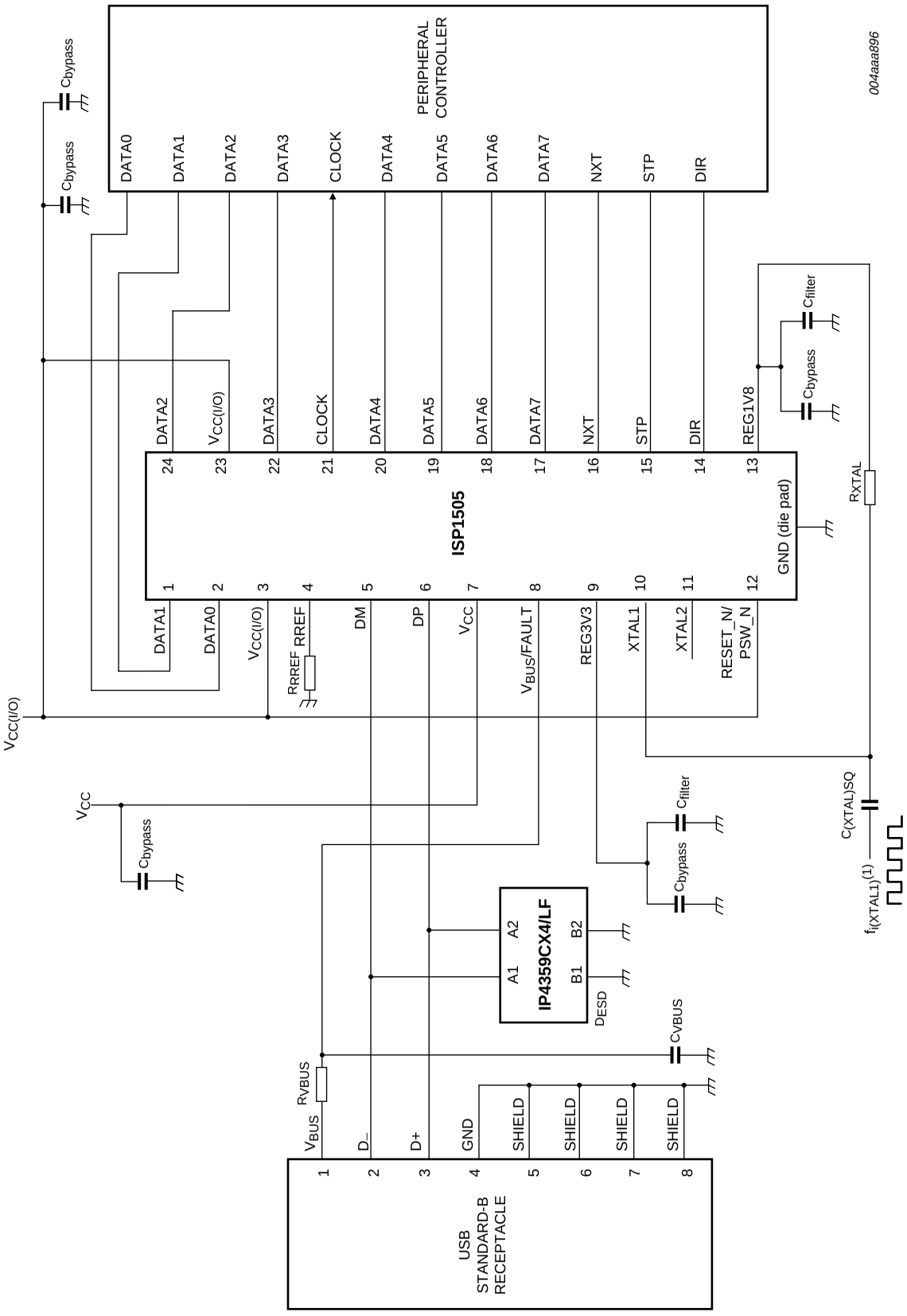
[1] For detailed information and alternative interface options, refer to the *Interfacing to the ISP1504/5/6 (AN10048)* application note.

[2] For more information, contact Murata.



(1) Frequency is version dependent: ISP1505ABS: 19.2 MHz; ISP1505CBS: 26 MHz.

Fig 26. Using the ISP1505 with a USB host controller; external 5 V source with built-in FAULT and external crystal

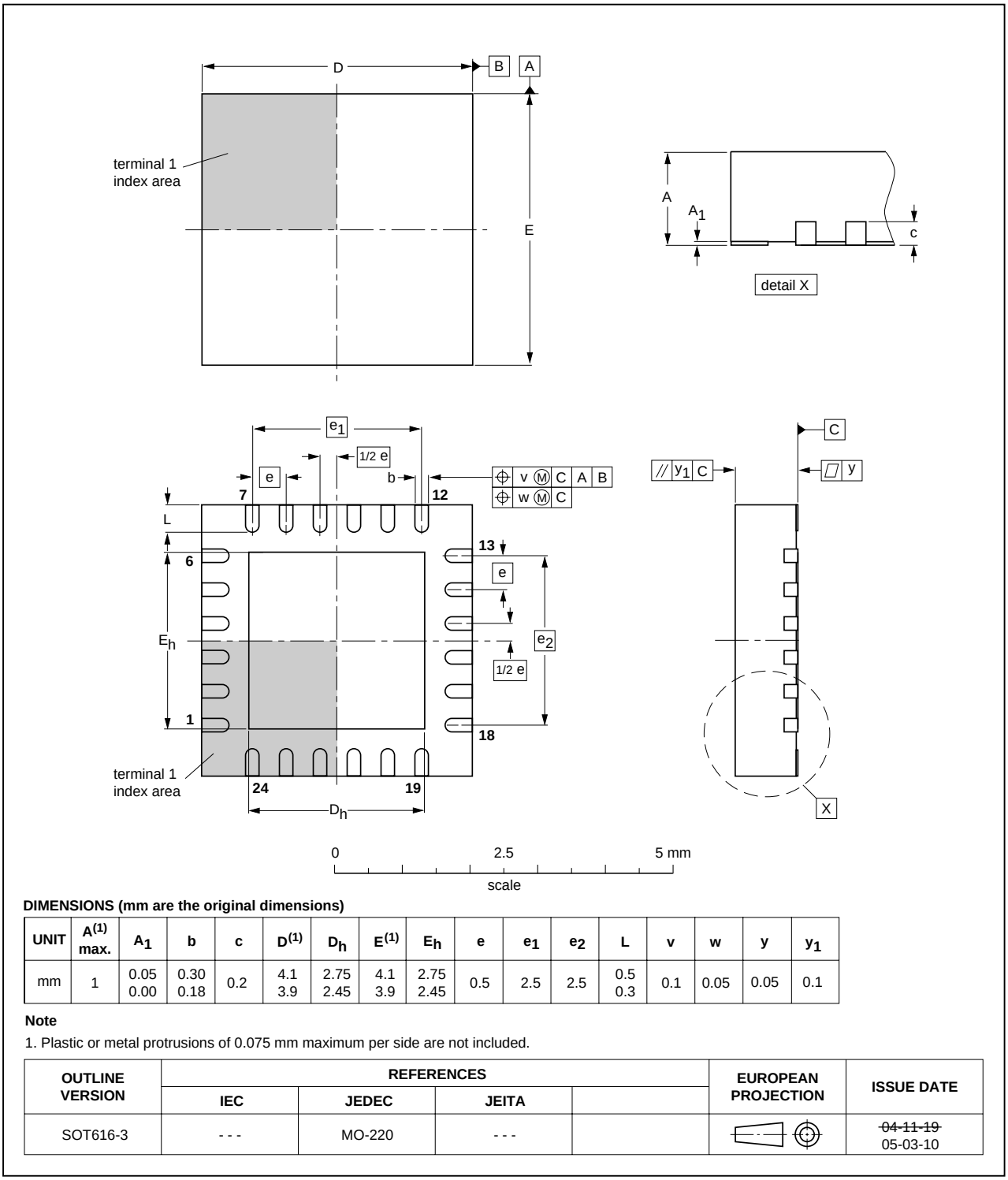


(1) Frequency is version dependent: ISP1505ABS: 19.2 MHz; ISP1505CBS: 26 MHz.

Fig 27. Using the ISP1505 with a peripheral controller; external square wave input on pin XTAL1

17. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.75 2.45	4.1 3.9	2.75 2.45	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-3	- - -	MO-220	- - -			~~04-11-19~~ 05-03-10

Fig 28. Package outline SOT616-3 (HVQFN24)

18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 29) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 55 and 56

Table 55. SnPb eutectic process (from J-STD-020C)

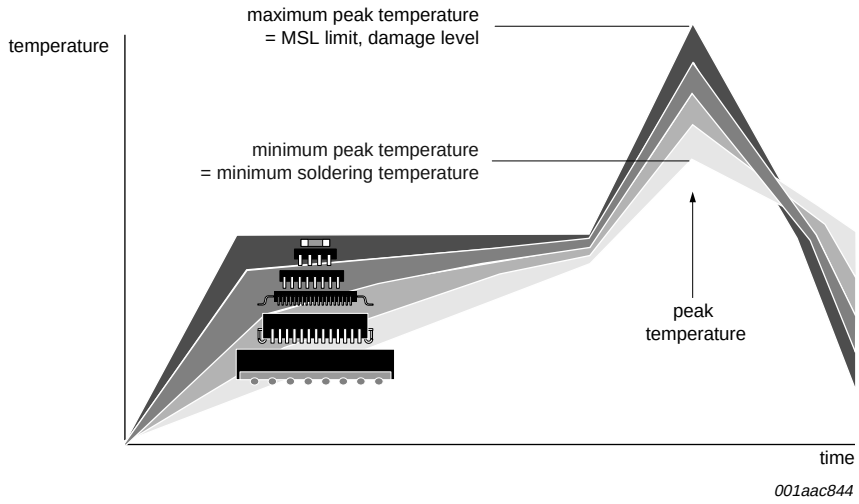
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 56. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 29.



MSL: Moisture Sensitivity Level

Fig 29. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

19. Abbreviations

Table 57. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
ATX	Analog USB Transceiver
CD-RW	Compact Disc-ReWritable
EOP	End-Of-Packet
ESD	ElectroStatic Discharge
ESR	Effective Series Resistance
FS	Full-Speed
HBM	Human Body Model
HNP	Host Negotiation Protocol
HS	High-Speed
ID	Identification
IEC	International Electrotechnical Commission
LS	Low-Speed
MO	Magneto-Optical
NRZI	Non-Return-to-Zero Inverted
OTG	On-The-Go
PCB	Printed-Circuit Board
PDA	Personal Digital Assistant
PHY	Physical Layer

Table 57. Abbreviations *...continued*

Acronym	Description
PID	Packet Identifier
PLD	Programmable Logic Device
PLL	Phase-Locked Loop
POR	Power-On Reset
RoHS	Restriction of Hazardous Substances
RXCMD	Receive Command
SE0	Single-Ended Zero
SOF	Start-Of-Frame
SRP	Session Request Protocol
STB	Set-Top Box
SYNC	Synchronous
TTL	Transistor-Transistor Logic
TXCMD	Transmit Command
USB	Universal Serial Bus
USB-IF	USB Implementers Forum
ULPI	UTMI+ Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
UTMI+	USB 2.0 Transceiver Macrocell Interface Plus

20. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3

[3] UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1

[4] UTMI+ Specification Rev. 1.0

[5] USB 2.0 Transceiver Macrocell Interface (UTMI) Specification Ver. 1.05

[6] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

[7] Interfacing to the ISP1504/5/6 (AN10048)

21. Revision history

Table 58. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1505A_ISP1505C_3	20080826	Product data sheet	-	ISP1505A_ISP1505C_2
Modifications:	• Changed *On-The-Go Supplement to the USB 2.0 Specification* from Rev. 1.2 to Rev. 1.3. • Section 2 “Features”: updated. • Section 8.2 “USB and OTG state transitions”: updated the first sentence. • Section “OTG devices”: updated the last sentence. • Section 9.10.1 “Full-speed and low-speed host-initiated suspend and resume”: updated the second list item. • Section 9.10.2 “High-speed suspend and resume”: updated the second list item. • Table 41 “Power Control register (address R = 3Dh to 3Fh, W = 3Dh, S = 3Eh, C = 3Fh) bit description”: updated description for bits 3 and 2. • Removed reference to input clock mode from the following sections: – Section 2 “Features” – Section 5 “Block diagram” – Table 2 “Pin description” – Section 7.5 “Crystal oscillator and PLL” – Section 7.10.2 “$V_{CC(I/O)}$” – Section 7.10.8 “XTAL1 and XTAL2” – Section 7.10.13 “CLOCK” – Table 3 “ULPI signal description” – Section 9.3 “Power-up, reset and bus idle sequence” – Table 42 “Limiting values” – Table 43 “Recommended operating conditions” – Table 45 “Static characteristics: digital pins (CLOCK, DIR, STP, NXT, DATA[7:0], RESET_N/PSW_N)” – Table 51 “Dynamic characteristics: reset and clock” – Table 52 “Dynamic characteristics: digital I/O pins” – Section 16 “Application information”			
ISP1505A_ISP1505C_2	20070913	Product data sheet	-	ISP1505A_ISP1505C_1
Modifications:	• Section 9.4.2 “Fault detection”: updated. • Section “Standard USB host controllers”: updated the first list item. • Section 10.2 “Extended register set”: updated the second paragraph. • Table 42 “Limiting values”: added V_I on the DP and DM pins, and added Table note 1. • Table 51 “Dynamic characteristics: reset and clock”: added $\delta_{i(XTAL1)}$ and Table note 1. • Table 52 “Dynamic characteristics: digital I/O pins”: updated. • Section 16 “Application information”: updated.			
ISP1505A_ISP1505C_1	20061019	Product data sheet	-	-

22. Legal information

22.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

22.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

22.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

22.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

23. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

24. Tables

25. Figures

26. Contents

continued >>

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 August 2008
Document identifier: ISP1505A_ISP1505C_3