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ST-NXP Wireless

ISP1102A

Advanced Universal Serial Bus transceiver

Rev. 01 — 15 February 2007 Product data sheet

1. General description

The ISP1102A Universal Serial Bus (USB) transceiver is fully compliant with Ref. 1 “Universal Serial Bus Specification Rev. 2.0”. The ISP1102A can transmit and receive USB data at full-speed (12 Mbit/s).

The transceiver allows USB Application-Specific Integrated Circuits (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65 V to 3.6 V to interface with the physical layer of the USB. The transceiver has an integrated 5 V-to-3.3 V voltage regulator for direct powering through USB supply line V_{BUS}. The transceiver has an integrated voltage detector to detect the presence of the V_{BUS} voltage ($V_{CC(5V0)}$). When $V_{CC(5V0)}$ or VREG3V3 is lost, the DP and DM pins can be shared with other serial protocols.

The transceiver is a bidirectional differential interface and is available in HBCC16 package.

The transceiver is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, Personal Digital Assistants (PDAs) and Information Appliances (IAs).

2. Features

- Complies with Ref. 1 “Universal Serial Bus Specification Rev. 2.0”
- Supports data transfer at full-speed (12 Mbit/s)
- Integrated 5 V-to-3.3 V voltage regulator to power through USB line V_{BUS}
- V_{BUS} voltage presence indication on pin VBUSDET
- VP and VM pins function in bidirectional mode, allowing pin count saving for the ASIC interface
- Used as USB device transceiver or USB host transceiver
- Stable RCV output during Single-Ended Zero (SE0) condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports I/O voltage range from 1.65 V to 3.6 V
- ±12 kV ElectroStatic Discharge (ESD) protection at the DP, DM, $V_{CC(5V0)}$ and GND pins
- Full industrial operating temperature range from –40 °C to +85 °C
- Available in HBCC16 lead-free and halogen-free package

3. Applications

- Portable electronic devices, such as:
  - Mobile phone
  - Digital still camera
  - Personal Digital Assistant (PDA)
  - Information Appliance (IA)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ISP1102AW	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

5. Block diagram

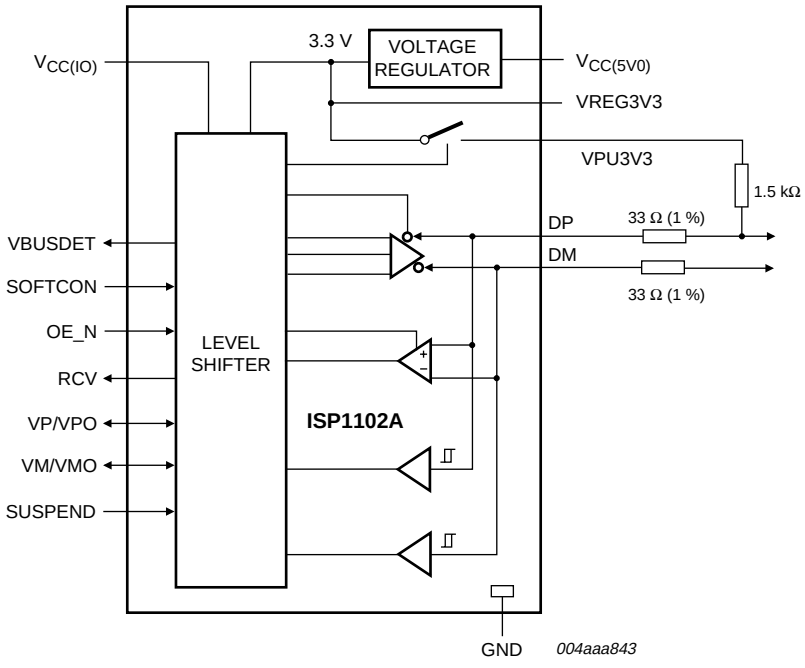


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

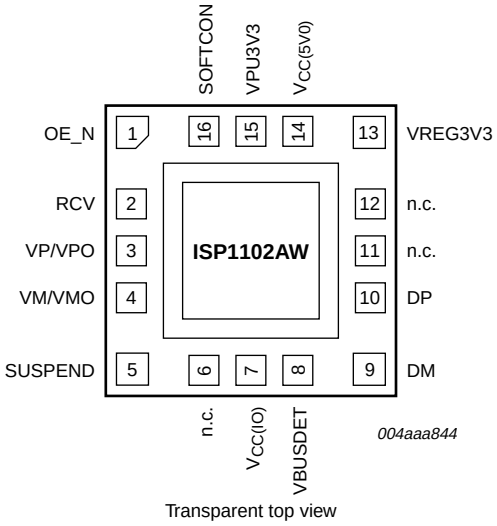


Fig 2. Pin configuration HBCC16 (top view)

6.2 Pin description

Table 2. Pin description

Symbol[1]	Pin	Type[2]	Description
OE_N	1	I	input for output enable (CMOS level with respect to $V_{CC(IO)}$, active LOW); enables the transceiver to transmit data on the USB bus input pad; push pull; CMOS
RCV	2	O	differential data receiver output (CMOS level with respect to $V_{CC(IO)}$); driven LOW when input SUSPEND is HIGH; the output state of RCV is preserved and stable during an SE0 condition output pad; push pull; 4 mA output drive; CMOS
VP/VPO	3	I/O	single-ended DP receiver output VP (CMOS level with respect to $V_{CC(IO)}$); for external detection of SE0, error conditions, speed of connected device; this pin also acts as drive data input VPO; see Table 3 and Table 4 bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
VM/VMO	4	I/O	single-ended DM receiver output VM (CMOS level with respect to $V_{CC(IO)}$); for external detection of SE0, error conditions, speed of connected device; this pin also acts as drive data input VMO; see Table 3 and Table 4 bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
SUSPEND	5	I	suspend input (CMOS level with respect to $V_{CC(IO)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level input pad; push pull; CMOS
n.c.	6	-	not connected

Table 2. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description
$V_{CC(IO)}$	7	-	supply voltage for digital I/O pins (1.65 V to 3.6 V); when $V_{CC(IO)}$ is not connected, the DP and DM pins are in 3-state; this supply pin is totally independent of $V_{CC(5V0)}$ and VREG3V3 and must never exceed the VREG3V3 voltage
VBUSDET	8	O	V_{BUS} indicator output (CMOS level with respect to $V_{CC(IO)}$) • When V_{BUS} > 4.1 V, then VBUSDET = HIGH • When V_{BUS} < 3.6 V, then VBUSDET = LOW • When SUSPEND = HIGH, then the VBUSDET function is invalid Connect a 1 µF-to-10 µF decoupling capacitor (4.7 µF capacitor is used on the ISP1102 evaluation board) output pad; push pull; 4 mA output drive; CMOS
DM	9	AI/O	negative USB data bus connection (analog, differential)
DP	10	AI/O	positive USB data bus connection (analog, differential)
n.c.	11	-	not connected
n.c.	12	-	not connected
VREG3V3	13	-	**internal regulator option:** regulated supply voltage output (3.0 V to 3.6 V) during 5 V operation; a decoupling capacitor of at least 0.1 µF is required **regulator bypass option:** used as a supply voltage input (3.3 V ± 10 %) for 3.3 V operation
$V_{CC(5V0)}$	14	-	**internal regulator option:** supply voltage input (4.0 V to 5.5 V); can directly be connected to USB line V_{BUS} **regulator bypass option:** connect to VREG3V3
VPU3V3	15	-	pull-up supply voltage (3.3 V ± 10 %); connect an external 1.5 kΩ resistor on DP (full-speed) This pin function is controlled by the SOFTCON input: **SOFTCON = LOW —** VPU3V3 floating (high-Z); ensures zero pull-up current **SOFTCON = HIGH —** VPU3V3 = 3.3 V; internally connected to VREG3V3
SOFTCON	16	I	software controlled USB connection input; a HIGH level applies 3.3 V to pin VPU3V3, which is connected to an external 1.5 kΩ pull-up resistor; this allows USB connect or disconnect signaling to be controlled by software input pad; push pull; CMOS
GND	exposed die pad	-	ground supply; down bonded to the exposed die pad (heat sink); to be connected to the PCB ground

[1] Symbol names with an underscore N (for example, OE_N) indicate active LOW signals.

[2] I = input; O = output; I/O = digital input/output; AI/O = analog input/output.

7. Functional description

7.1 Function selection

Table 3. Function selection

SUSPEND	OE_N	DP, DM	RCV	VP/VPO	VM/VMO	Function
LOW	LOW	driving or receiving	active	VPO input	VMO input	normal driving (differential receiver active)
LOW	HIGH	receiving[1]	active	VP output	VM output	receiving
HIGH	LOW	driving	inactive[2]	VPO input	VMO input	driving during suspend (differential receiver inactive)
HIGH	HIGH	high-Z[1]	inactive[2]	VP output	VM output	low-power state

[1] Signal levels on the DP and DM pins are determined by other USB devices and external pull-up or pull-down resistors.

[2] In suspend mode (SUSPEND = HIGH), the differential receiver is inactive and output RCV is always LOW. The resume signaling is detected through single-ended receivers VP/VPO and VM/VMO.

7.2 Operating functions

Table 4. Driving function using differential input data interface (pin OE_N = LOW)

VM/VMO	VP/VPO	Data
LOW	LOW	SE0
LOW	HIGH	differential logic 1
HIGH	LOW	differential logic 0
HIGH	HIGH	illegal state

Table 5. Receiving function (pin OE_N = HIGH)

DP, DM	RCV	VP/VPO	VM/VMO
Differential logic 0	LOW	LOW	HIGH
Differential logic 1	HIGH	HIGH	LOW
SE0	RCV*[1]	LOW	LOW

[1] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

7.3 Power supply configurations

The ISP1102A can be used with various power supply configurations, which can be changed dynamically. Table 7 provides an overview of the power supply configurations.

Normal mode — $V_{CC(IO)}$ is connected. $V_{CC(5V0)}$ is connected only, or $V_{CC(5V0)}$ and VREG3V3 are connected.

For the 5 V operation, $V_{CC(5V0)}$ is connected to a 5 V source (4.0 V to 5.5 V). The internal voltage regulator then produces 3.3 V for USB connections.

For the 3.3 V operation, both $V_{CC(5V0)}$ and VREG3V3 are connected to a 3.3 V source (3.0 V to 3.6 V).

$V_{CC(IO)}$ is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.

Sharing mode — $V_{CC(IO)}$ is connected only, $V_{CC(5V0)}$ is < 3.6 V, and VREG3V3 is < 2.4 V. In this mode, the DP and DM pins are 3-stated and the ISP1102A allows external signals of up to 3.6 V to share the DP and DM lines. The internal circuits of the ISP1102A ensure that virtually no current (maximum 10 μA) is drawn through the DP and DM lines. The power consumption through pin $V_{CC(IO)}$ drops to the low-power (suspended) state level.

Pins VBUSDET and RCV are driven to LOW to indicate this mode. The VBUSDET function is ignored during suspend mode of the ISP1102A.

Some hysteresis is built into the detection of VREG3V3 lost.

Remark: Sharing mode is not possible in the regulator bypass option.

Table 6. Pin states in sharing modes

Pin	Sharing mode
$V_{CC(5V0)}$	< 3.6 V
VREG3V3	< 2.4 V
$V_{CC(IO)}$	1.65 V to 3.6 V input
VPU3V3	high-Z (off)
DP, DM	high-Z
VP/VPO, VM/VMO[1]	LOW
RCV	LOW
VBUSDET	LOW
OE_N, SUSPEND, SOFTCON	high-Z

[1] VP/VPO and VM/VMO are bidirectional pins.

Table 7. Power supply configuration overview

$V_{CC(5V0)}$	$V_{CC(IO)}$	Configuration	Special characteristics
Connected	connected	normal mode	-
< 3.6 V	connected	sharing mode	DP, DM and VPU3V3: high-Z VP/VPO and VM/VMO: driven LOW RCV: driven LOW VBUSDET: driven LOW

7.4 Power supply input options

The ISP1102A has two power supply input options.

Internal regulator — Pin $V_{CC(5V0)}$ is connected to 4.0 V to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). The VREG3V3 pin becomes a 3.3 V output reference.

Regulator bypass — Pins $V_{CC(5V0)}$ and VREG3V3 are connected to the same supply. The internal regulator is bypassed and the internal circuitry is supplied directly from pin VREG3V3. The voltage range is 3.0 V to 3.6 V to comply with Ref. 1 “Universal Serial Bus Specification Rev. 2.0”.

The supply voltage range for each input option is specified in Table 8.

Table 8. Power supply input options

Input option	$V_{CC(5V0)}$	VREG3V3	$V_{CC(IO)}$
Internal regulator	supply input for internal regulator (4.0 V to 5.5 V)	voltage reference output (3.3 V, 300 µA)	supply input for digital I/O pins (1.65 V to 3.6 V)
Regulator bypass	connected to VREG3V3 with maximum voltage drop of 0.3 V (2.7 V to 3.6 V)	supply input (3.0 V to 3.6 V)	supply input for digital I/O pins (1.65 V to 3.6 V)

8. ElectroStatic Discharge (ESD)

8.1 ESD protection

For the HBCC package, the pins that are connected to the USB connector (DP, DM, $V_{CC(5V0)}$ and GND) have a minimum of ±12 kV ESD protection. The ±12 kV measurement is limited by the test equipment. Capacitors of 4.7 µF connected from VREG3V3 to GND and $V_{CC(5V0)}$ to GND are required to achieve this ±12 kV ESD protection (see Figure 3).

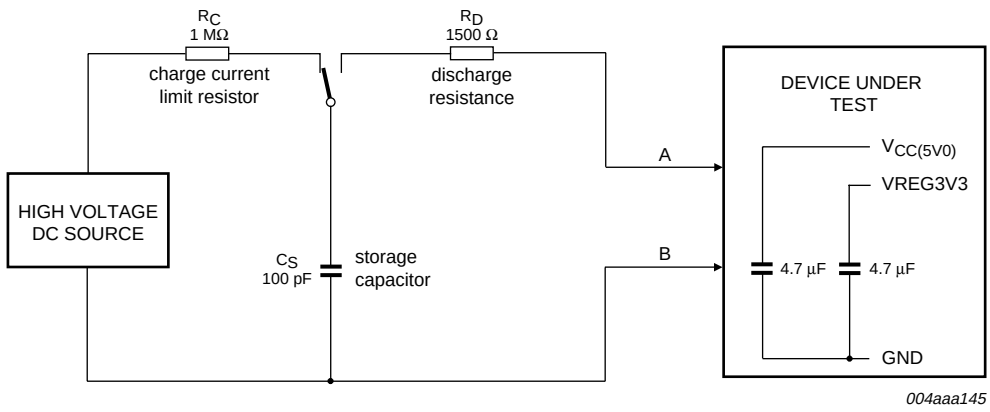


Fig 3. Human body ESD test model

8.2 ESD test conditions

A detailed report on test set up and results is available on request.

9. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)			–0.5	+6.0	V
$V_{CC(IO)}$	IO supply voltage			–0.5	+4.6	V
V_I	input voltage			–0.5	$V_{CC(IO)}$ + 0.5 V	V
I_{lu}	latch-up current	V_I = –1.8 V to +5.4 V		-	100	mA
V_{esd}	electrostatic discharge voltage	pins DP, DM, $V_{CC(5V0)}$ and GND; I_{LI} < 3 µA	[1][2]	–12000	+12000	V
		all other pins; I_{LI} < 1 µA	[2]	–2000	+2000	V
T_{stg}	storage temperature			–40	+125	°C

[1] Testing equipment limits measurement to only ±12 kV. Capacitors needed on $V_{CC(5V0)}$ and VREG3V3 (see Section 8).

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

10. Recommended operating conditions

Table 10. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		4.0	5.0	5.5	V
$V_{CC(IO)}$	IO supply voltage		1.65	-	3.6	V
V_I	input voltage		0	-	$V_{CC(IO)}$	V
$V_{IA(I/O)}$	input voltage on analog I/O pins	on pins DP and DM	0	-	3.6	V
T_j	junction temperature		–40	-	+125	°C
T_{amb}	ambient temperature		–40	-	+85	°C

11. Static characteristics

Table 11. Static characteristics: supply pins

$V_{CC(5V0)}$ = 4.0 V to 5.5 V or $V_{(VREG3V3)}$ = 3.0 V to 3.6 V; $V_{CC(IO)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; see Table 8 for valid voltage level combinations; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(VREG3V3)}$	voltage on pin VREG3V3	internal regulator option; I_{load} ≤ 300 µA	[1][2]	3.0	3.3	3.6	V
I_{CC}	supply current	transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins DP and DM	[3]	-	4	8	mA
$I_{CC(IO)}$	supply current on pin $V_{CC(IO)}$	transmitting and receiving at 12 Mbit/s	[3]	-	1	2	mA
$I_{CC(idle)}$	idle and SE0 supply current	idle: V_{DP} > 2.7 V, V_{DM} < 0.3 V; SE0: V_{DP} < 0.3 V, V_{DM} < 0.3 V	[4]	-	-	300	µA
$I_{CC(IO)static}$	static supply current on pin $V_{CC(IO)}$	idle, SE0 or suspend		-	-	20	µA
$I_{CC(susp)}$	suspend supply current	SUSPEND = HIGH	[4]	-	-	20	µA

Table 11. Static characteristics: supply pins *…continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V or $V_{(VREG3V3)}$ = 3.0 V to 3.6 V; $V_{CC(IO)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; see Table 8 for valid voltage level combinations; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{CC(IO)sharing}$	sharing mode supply current on pin $V_{CC(IO)}$	$V_{CC(5V0)}$ < 3.6 V		-	-	20	µA
$I_{load(sharing)DM}$	sharing mode load current on pin DM	$V_{CC(5V0)}$ < 3.6 V; SOFTCON = LOW; V_{DM} = 3.6 V		-	-	10	µA
$I_{load(sharing)DP}$	sharing mode load current on pin DP	$V_{CC(5V0)}$ < 3.6 V; SOFTCON = LOW; V_{DP} = 3.6 V		-	-	10	µA
$V_{CC(5V0)th}$	supply voltage detection threshold (5.0 V)	1.65 V ≤ $V_{CC(IO)}$ ≤ 3.6 V					
		supply lost		-	-	3.6	V
		supply present		4.1	-	-	V
$V_{CC(5V0)hys}$	supply voltage detection hysteresis (5.0 V)	$V_{CC(IO)}$ = 1.8 V		-	70	-	mV
$V_{CC(IO)th}$	supply voltage detection threshold on pin $V_{CC(IO)}$	$V_{(VREG3V3)}$ = 2.7 V to 3.6 V					
		supply lost		-	-	0.5	V
		supply present		1.4	-	-	V
$V_{CC(IO)hys}$	supply voltage detection hysteresis on pin $V_{CC(IO)}$	$V_{(VREG3V3)}$ = 3.3 V		-	0.45	-	V
$V_{REG(3V3)th}$	regulated supply voltage detection threshold (3.3 V)	1.65 V ≤ $V_{CC(IO)}$ ≤ $V_{(VREG3V3)}$; 2.7 V ≤ $V_{(VREG3V3)}$ ≤ 3.6 V					
		supply lost		-	-	0.8	V
		supply present	[5]	2.4	-	-	V
$V_{REG(3V3)hys}$	regulated supply voltage detection hysteresis (3.3 V)	$V_{CC(IO)}$ = 1.8 V		-	0.45	-	V

[1] I_{load} includes the pull-up resistor current through pin VPU3V3.

[2] The minimum voltage is 2.7 V in suspend mode.

[3] Maximum value characterized only, not tested in production.

[4] Excluding any load current and VPU3V3 or V_{SW} source current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typ.).

[5] When $V_{CC(IO)}$ < 2.7 V, the minimum value for $V_{REG(3V3)th}$ = 2.0 V for supply present condition.

Table 12. Static characteristics: digital pins

$V_{CC(IO)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(IO)}$ = 1.65 V to 3.6 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(IO)}$	V
V_{IH}	HIGH-level input voltage		$0.6V_{CC(IO)}$	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	$V_{CC(IO)}$ − 0.15 V	-	-	V
		I_{OH} = 2 mA	$V_{CC(IO)}$ − 0.4 V	-	-	V

Table 12. Static characteristics: digital pins *...continued*

$V_{CC(IO)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	10	pF
Example 1: $V_{CC(IO)}$ = 1.8 V ± 0.15 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	0.5	V
V_{IH}	HIGH-level input voltage			1.2	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA		1.5	-	-	V
		I_{OH} = 2 mA		1.25	-	-	V
Leakage current							
I_{LI}	input leakage current		[1]	−1	-	+1	µA
Example 2: $V_{CC(IO)}$ = 2.5 V ± 0.2 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	0.7	V
V_{IH}	HIGH-level input voltage			1.7	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA		2.15	-	-	V
		I_{OH} = 2 mA		1.9	-	-	V
Leakage current							
I_{LI}	input leakage current		[1]	−5	-	+5	µA
Example 3: $V_{CC(IO)}$ = 3.3 V ± 0.3 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	0.9	V
V_{IH}	HIGH-level input voltage			2.15	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA		2.85	-	-	V
		I_{OH} = 2 mA		2.6	-	-	V
Leakage current							
I_{LI}	input leakage current		[1]	−5	-	+5	µA

[1] If $V_{CC(IO)} \geq V_{(VREG3V3)}$, then the leakage current will be higher than the specified value.

Table 13. Static characteristics: analog I/O pins DP and DM

$V_{CC(5V0)}$ = 4.0 V to 5.5 V or $V_{(VREG3V3)}$ = 3.0 V to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels							
Differential receiver							
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$		0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range		0.8	-	2.5	V
Single-ended receiver							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Output levels							
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to 3.6 V		-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	[1]	2.8	-	3.6	V
Leakage current							
I_{LZ}	off-state leakage current			−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	20	pF
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	39	44	Ω
Z_{INP}	input impedance			10	-	-	MΩ
$R_{sw(VPU3V3)}$	switch-on resistance on pin VPU3V3			-	-	10	Ω
Termination							
V_{TERM}	termination voltage	for upstream port pull-up (R_{PU})	[3][4]	3.0	-	3.6	V

[1] $V_{OH(min)} = V_{(VREG3V3)} - 0.2$ V.

[2] Includes external resistors of 33 Ω ± 1 % on both pins DP and DM.

[3] This voltage is available at pins VREG3V3 and VPU3V3.

[4] The minimum voltage is 2.7 V in suspend mode.

12. Dynamic characteristics

Table 14. Dynamic characteristics: analog I/O pins DP and DM

$V_{CC(5V0)}$ = 4.0 V to 5.5 V or $V_{(VREG3V3)}$ = 3.0 V to 3.6 V; $V_{CC(IO)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; see Table 8 for valid voltage level combinations; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_{FR}	rise time	C_L = 50 pF to 125 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 4	4	-	20	ns
t_{FF}	fall time	C_L = 50 pF to 125 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 4	4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from Idle state	90	-	111.1	%

Table 14. Dynamic characteristics: analog I/O pins DP and DM *…continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V or $V_{(VREG3V3)}$ = 3.0 V to 3.6 V; $V_{CC(IO)}$ = 1.65 V to 3.6 V; V_{GND} = 0 V; see Table 8 for valid voltage level combinations; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 5	[1]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	VPO, VMO to DP, DM; see Figure 5 and Figure 8		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	VPO, VMO to DP, DM; see Figure 5 and Figure 8		-	-	18	ns
t_{PHZ}	driver disable delay from HIGH level	OE_N to DP, DM; see Figure 6 and Figure 9		-	-	15	ns
t_{PLZ}	driver disable delay from LOW level	OE_N to DP, DM; see Figure 6 and Figure 9		-	-	15	ns
t_{PZH}	driver enable delay to HIGH level	OE_N to DP, DM; see Figure 6 and Figure 9		-	-	15	ns
t_{PZL}	driver enable delay to LOW level	OE_N to DP, DM; see Figure 6 and Figure 9		-	-	15	ns
Receiver timings							
Differential receiver							
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RCV; see Figure 7 and Figure 10		-	-	15	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RCV; see Figure 7 and Figure 10		-	-	15	ns
Single-ended receiver							
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to VP/VPO, VM/VMO; see Figure 7 and Figure 10		-	-	18	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to VP/VPO, VM/VMO; see Figure 7 and Figure 10		-	-	18	ns

[1] Characterized only, not tested. Limits guaranteed by design.

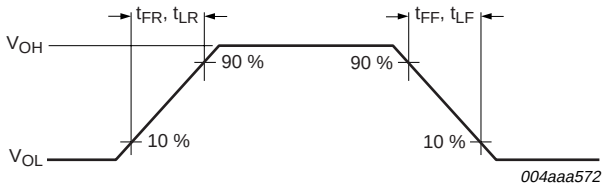


Fig 4. Rise time and fall time

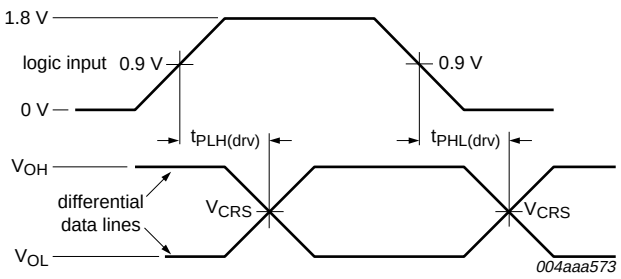


Fig 5. Timing of VPO and VMO to DP and DM

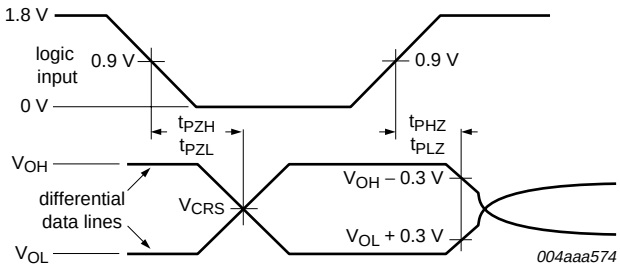


Fig 6. Timing of OE_N to DP and DM

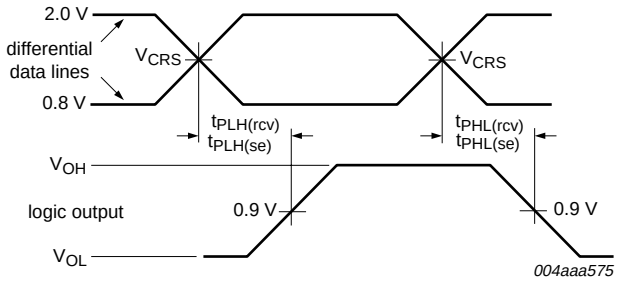
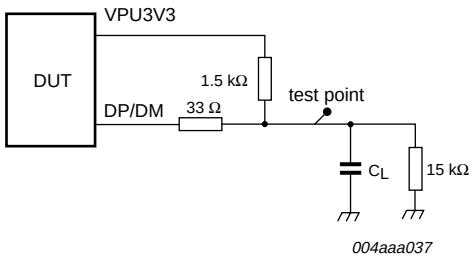


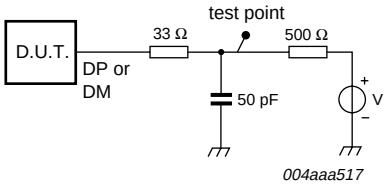
Fig 7. Timing of DP and DM to RCV, VP/VPO and VM/VMO

13. Test information



Load capacitance C_L = 50 pF (minimum or maximum timing)

Fig 8. Load on pins DP and DM



V = 0 V for t_{PZH} and t_{PHZ}

V = $V_{(VREG3V3)}$ for t_{PZL} and t_{PLZ}

Fig 9. Load on pins DP and DM for enable time and disable time

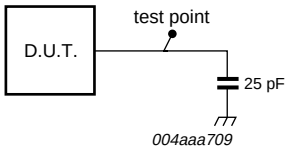
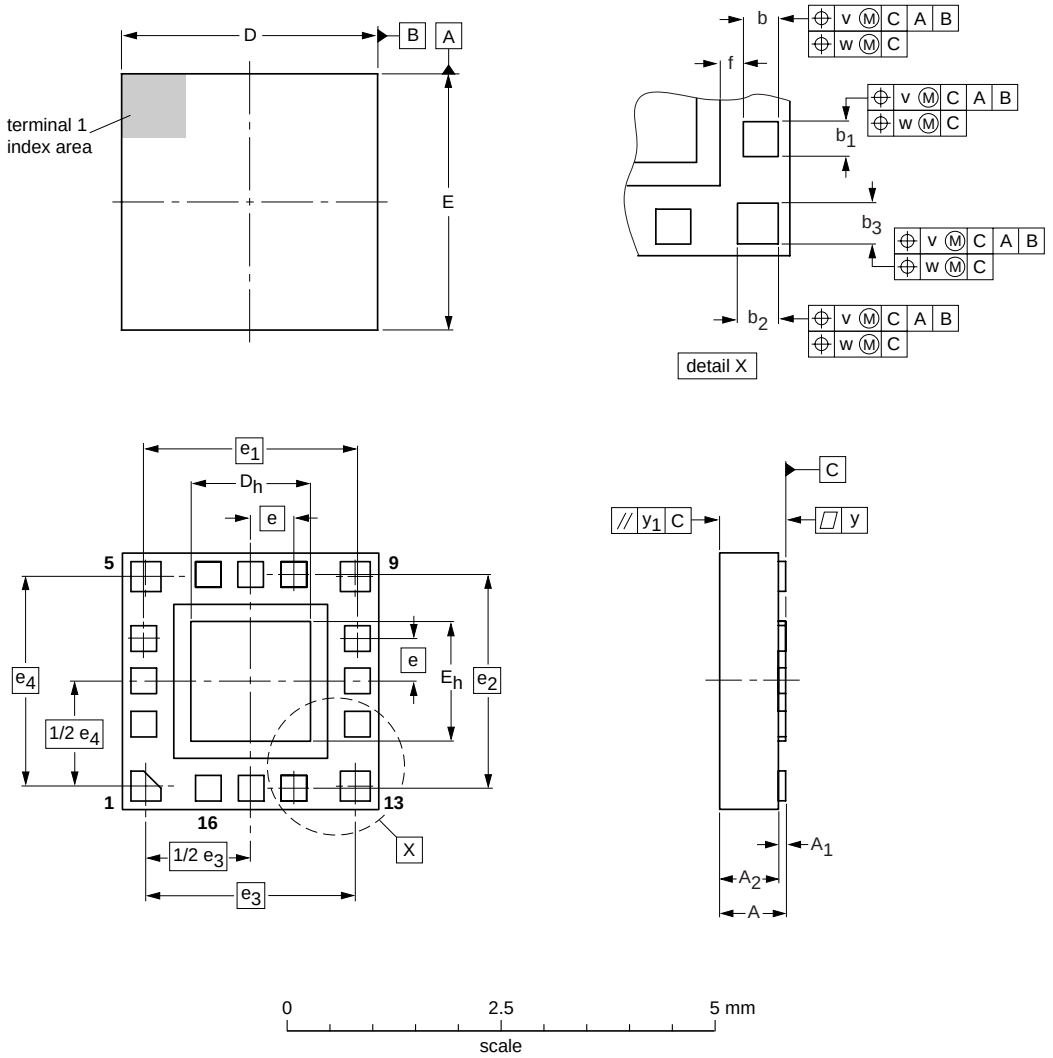


Fig 10. Load on pins VM/VMO, VP/VPO and RCV

14. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm **SOT639-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	f	v	w	y	y_1
mm	0.8	0.10 0.05	0.7 0.6	0.33 0.27	0.33 0.27	0.38 0.32	0.38 0.32	3.1 2.9	1.45 1.35	3.1 2.9	1.45 1.35	0.5	2.5	2.5	2.45	2.45	0.23 0.17	0.08	0.1	0.05	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT639-2		MO-217				01-11-13 03-03-12

Fig 11. Package outline SOT639-2 (HBCC16)

15. Packing information

The ISP1102AW (HBCC16 package) is delivered on a Type A carrier tape, see Figure 12. The tape dimensions are given in Table 15.

The reel diameter is 330 mm. The reel is made of polystyrene (PS) and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is ±0.02 mm. The camber must not exceed 1 mm in 100 mm.

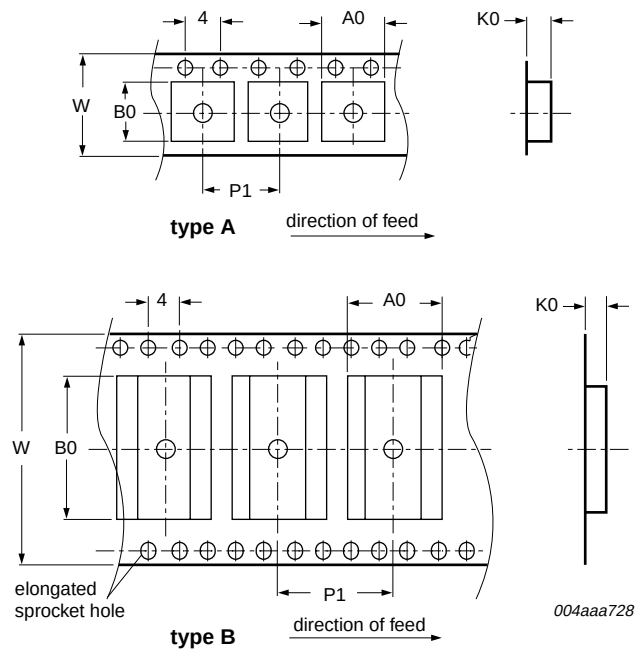


Fig 12. Carrier tape dimensions

Table 15. Type A carrier tape dimensions for the ISP1102AW

Dimension	Value	Unit
A0	3.3	mm
B0	3.3	mm
K0	1.1	mm
P1	8.0	mm
W	12.0 ± 0.3	mm

16. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020C)

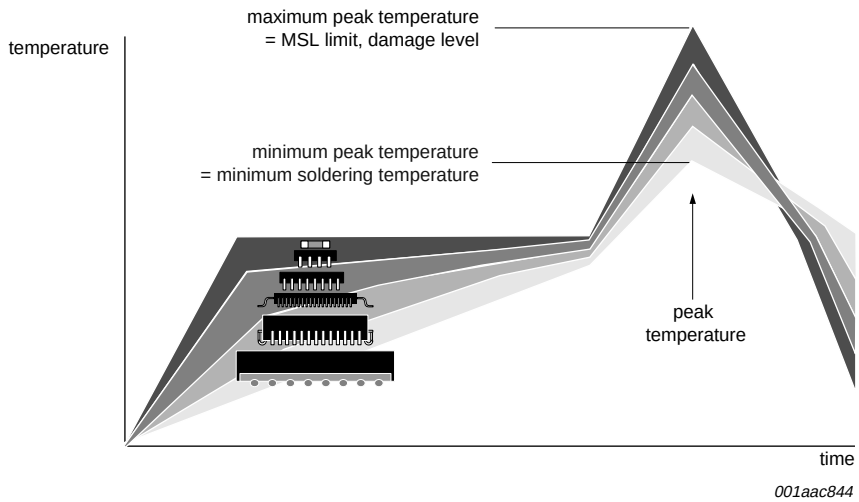
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.



MSL: Moisture Sensitivity Level

Fig 13. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 18. Abbreviations

Acronym	Description
ASIC	Application-Specific Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
SE0	Single-Ended Zero
USB	Universal Serial Bus

18. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) (JESD22-A114D)

19. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ISP1102A_1	20070215	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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