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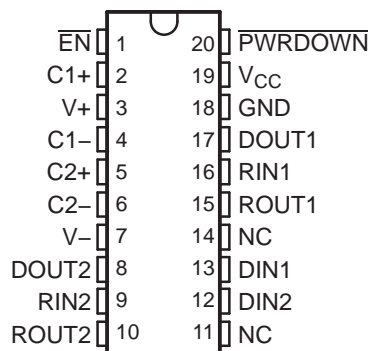
## FEATURES

- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Operates up to 1 Mbit/s
- Low Standby Current . . . 1  $\mu\text{A}$  Typ
- External Capacitors . . .  $4 \times 0.1 \mu\text{F}$
- Accepts 5-V Logic Input With 3.3-V Supply
- RS-232 Bus-Pin ESD Protection Exceeds  $\pm 15 \text{ kV}$  Using Human-Body Model (HBM)

## APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

DB, DW, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## DESCRIPTION/ORDERING INFORMATION

The TRSF3222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15\text{-kV}$  ESD protection pin to pin (serial-port connection pins, including GND). The device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ $\mu\text{s}$  to 150 V/ $\mu\text{s}$ .

The TRSF3222 can be placed in the power-down mode by setting the power-down ( $\overline{\text{PWRDOWN}}$ ) input low, which draws only 1  $\mu\text{A}$  from the power supply. When the device is powered down, the receivers remain active while the drivers are placed in the high-impedance state. Also, during power down, the onboard charge pump is disabled, V+ is lowered to  $V_{CC}$ , and V– is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ( $\overline{\text{EN}}$ ) high.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – DW	Tube of 25	TRSF3222CDW	TRSF3222EC
		Reel of 2000	TRSF3222CDWR	
	SSOP – DB	Tube of 70	TRSF3222CDB	RT22EC
		Reel of 2000	TRSF3222CDBR	
	TSSOP – PW	Tube of 70	TRSF3222CPW	RT22EC
		Reel of 2000	TRSF3222CPWR	
–40°C to 85°C	SOIC – DW	Tube of 25	TRSF3222IDW	TRSF3222EI
		Reel of 2000	TRSF3222IDWR	
	SSOP – DB	Tube of 70	TRSF3222IDB	RT22EI
		Reel of 2000	TRSF3222IDBR	
	TSSOP – PW	Tube of 70	TRSF3222IPW	RT22EI
		Reel of 2000	TRSF3222IPWR	

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



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**FUNCTION TABLES**

**Each Driver<sup>(1)</sup>**

INPUTS		OUTPUT DOUT
DIN	PWRDOWN	
X	L	Z
L	H	H
H	H	L

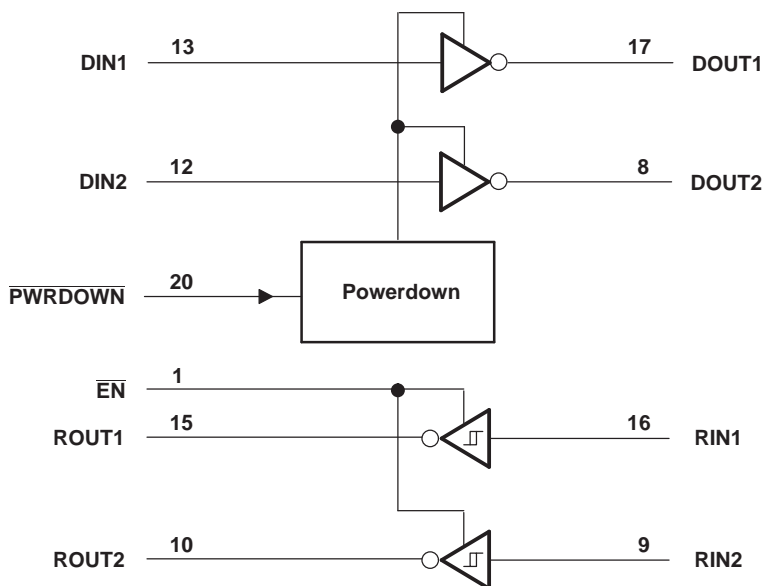
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

**Each Receiver<sup>(1)</sup>**

INPUTS		OUTPUT ROUT
RIN	EN	
L	L	H
H	L	L
X	H	Z
Open	L	H

(1) H = high level, L = low level, X = irrelevant,  
 Z = high impedance (off),  
 Open = input disconnected or connected driver off

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	–0.3	6	V	
V+	Positive-output supply voltage range <sup>(2)</sup>	–0.3	7	V	
V–	Negative-output supply voltage range <sup>(2)</sup>	0.3	–7	V	
V+ – V–	Supply voltage difference <sup>(2)</sup>		13	V	
V <sub>I</sub>	Input voltage range	Drivers ( $\overline{\text{EN}}$ , $\overline{\text{PWRDOWN}}$ )	–0.3	6	V
		Receivers	–25	25	
V <sub>O</sub>	Output voltage range	Drivers	–13.2	13.2	V
		Receivers	–0.3	V <sub>CC</sub> + 0.3	
θ <sub>JA</sub>	Package thermal impedance <sup>(3)(4)</sup>	DB package		70	°C/W
		DW package		58	
		PW package		83	
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	–65	150	°C	

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to network GND.
- Maximum power dissipation is a function of T<sub>J</sub>(max), θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

See [Figure 5](#)

		MIN	NOM	MAX	UNIT	
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{PWRDOWN}}$	V <sub>CC</sub> = 3.3 V	2		V
			V <sub>CC</sub> = 5 V	2.4		
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{PWRDOWN}}$		0.8		V
V <sub>I</sub>	Driver and control input voltage	DIN, $\overline{\text{EN}}$ , $\overline{\text{PWRDOWN}}$		0	5.5	V
V <sub>I</sub>	Receiver input voltage			–25	25	V
T <sub>A</sub>	Operating free-air temperature	TRSF3222C	0	70		°C
		TRSF3222I	–40	85		

- Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>I</sub>	Input leakage current ( $\overline{\text{EN}}$ , $\overline{\text{PWRDOWN}}$ )			±0.01	±1	μA
I <sub>CC</sub>	Supply current	No load, $\overline{\text{PWRDOWN}}$ at V <sub>CC</sub>		0.3	1	mA
	Supply current (powered off)	No load, $\overline{\text{PWRDOWN}}$ at GND		1	10	μA

- Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.
- All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND,	DIN = GND	5	5.4		V
V <sub>OL</sub>	Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND,	DIN = V <sub>CC</sub>	–5	–5.4		V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>			±0.01	±1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND			±0.01	±1	μA
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>O</sub> = 0 V	V <sub>CC</sub> = 3.6 V		±35	±60	mA
			V <sub>CC</sub> = 5.5 V		±35	±90	
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V,	V <sub>O</sub> = ±2 V	300	10M		Ω
I <sub>off</sub>	Output leakage current	$\overline{\text{PWRDOWN}} = \text{GND}$	V <sub>CC</sub> = 3 V to 3.6 V, V <sub>O</sub> = ±12 V			±25	μA
			V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>O</sub> = ±10 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
Maximum data rate (see <a href="#">Figure 1</a> )	R <sub>L</sub> = 3 kΩ, One DOUT switching	C <sub>L</sub> = 1000 pF		250			kbit/s	
		C <sub>L</sub> = 250 pF,	V <sub>CC</sub> = 3 V to 4.5 V	1000				
		C <sub>L</sub> = 1000 pF,	V <sub>CC</sub> = 4.5 V to 5.5 V	1000				
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF,	R <sub>L</sub> = 3 kΩ to 7 kΩ,	See <a href="#">Figure 2</a>		300	ns	
SR(tr)	Slew rate, transition region (see <a href="#">Figure 1</a> )	R <sub>L</sub> = 3 kΩ to 7 kΩ,	C <sub>L</sub> = 150 pF to 1000 pF,	V <sub>CC</sub> = 3.3 V		18	150	V/μs

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.5	2.4	V
		V <sub>CC</sub> = 5 V		1.8	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.2		V
		V <sub>CC</sub> = 5 V	0.8	1.5		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.3		V
I <sub>off</sub>	Output leakage current	$\overline{\text{EN}} = V_{\text{CC}}$		±0.05	±10	µA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

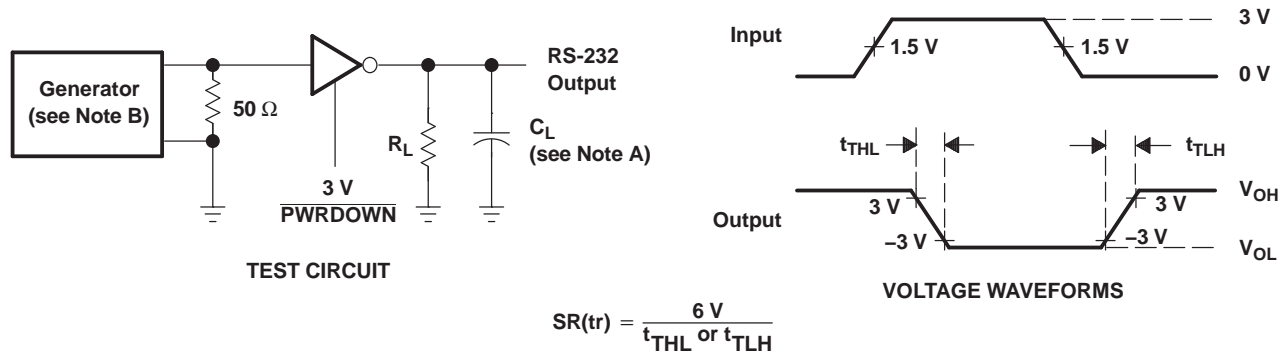
PARAMETER		TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	300	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	300	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	200	ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	See <a href="#">Figure 3</a>	300	ns

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

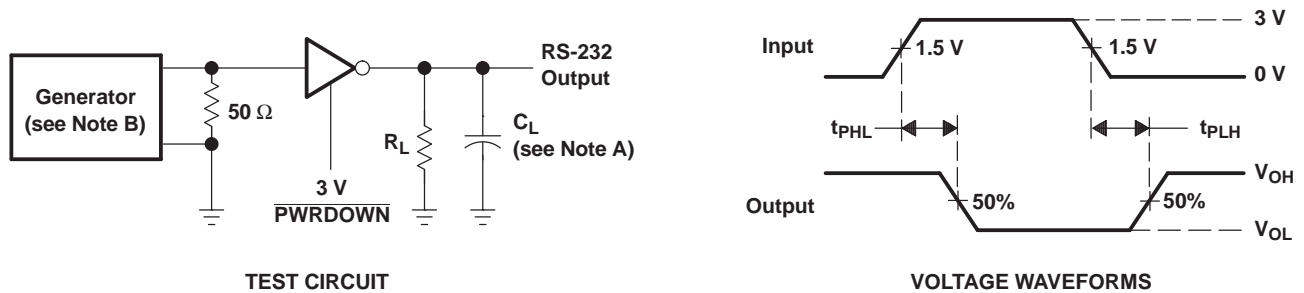
(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



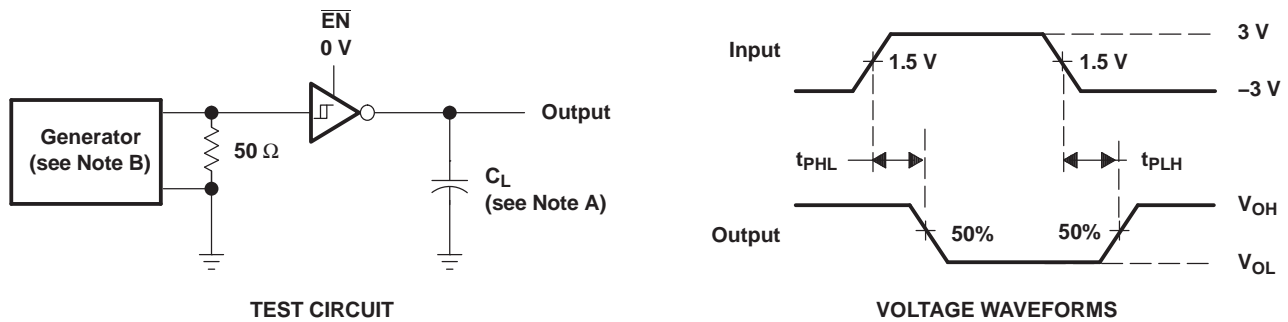
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 1. Driver Slew Rate



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

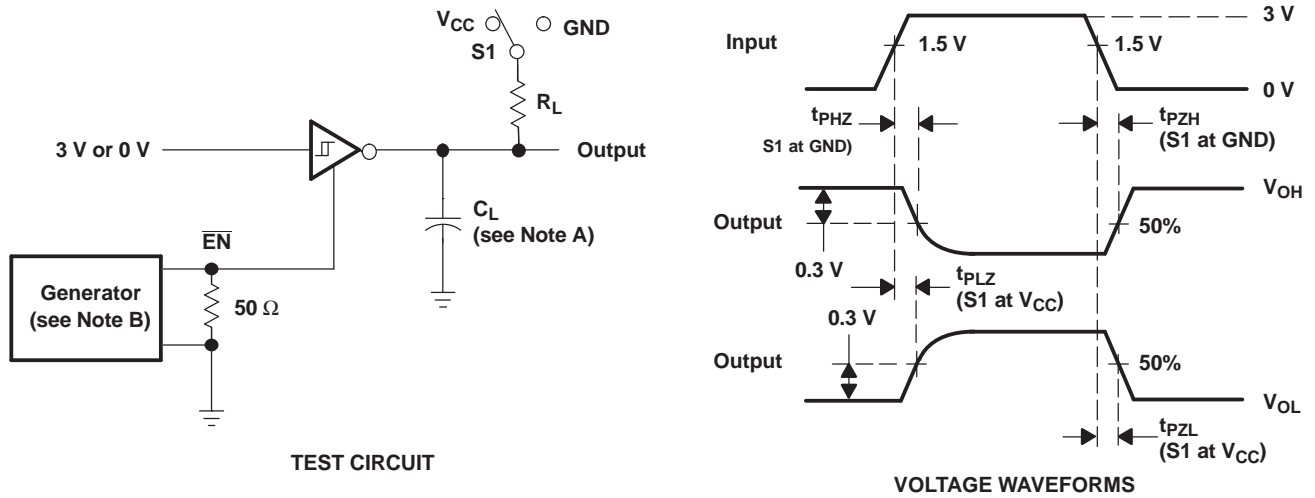
Figure 2. Driver Pulse Skew



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 3. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION (continued)

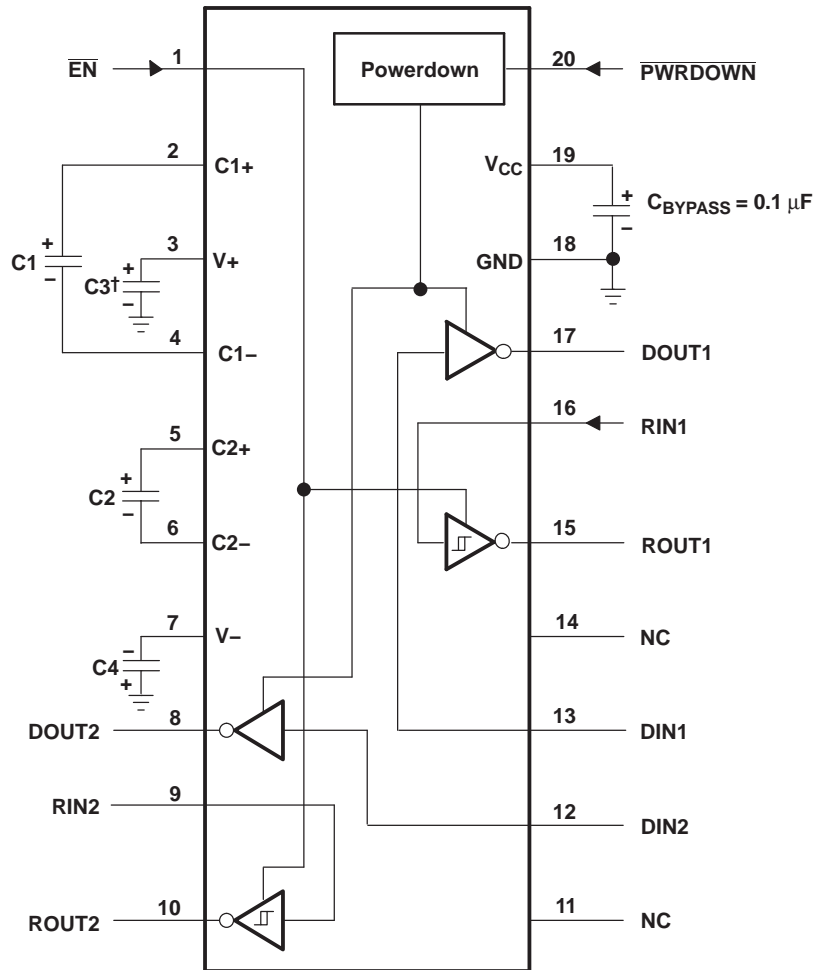


- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 4. Receiver Enable and Disable Times



APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.  
 NOTES: A. Resistor values shown are nominal.  
 B. NC – No internal connection

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 5. Typical Operating Circuit and Capacitor Values

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TRSF3222CDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222CPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDB	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDBG4	ACTIVE	SSOP	DB	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TRSF3222IPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

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**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3222CDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3222CDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
TRSF3222CPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TRSF3222IDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3222IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
TRSF3222IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3222CDBR	SSOP	DB	20	2000	346.0	346.0	33.0
TRSF3222CDWR	SOIC	DW	20	2000	346.0	346.0	41.0
TRSF3222CPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
TRSF3222IDBR	SSOP	DB	20	2000	346.0	346.0	33.0
TRSF3222IDWR	SOIC	DW	20	2000	346.0	346.0	41.0
TRSF3222IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

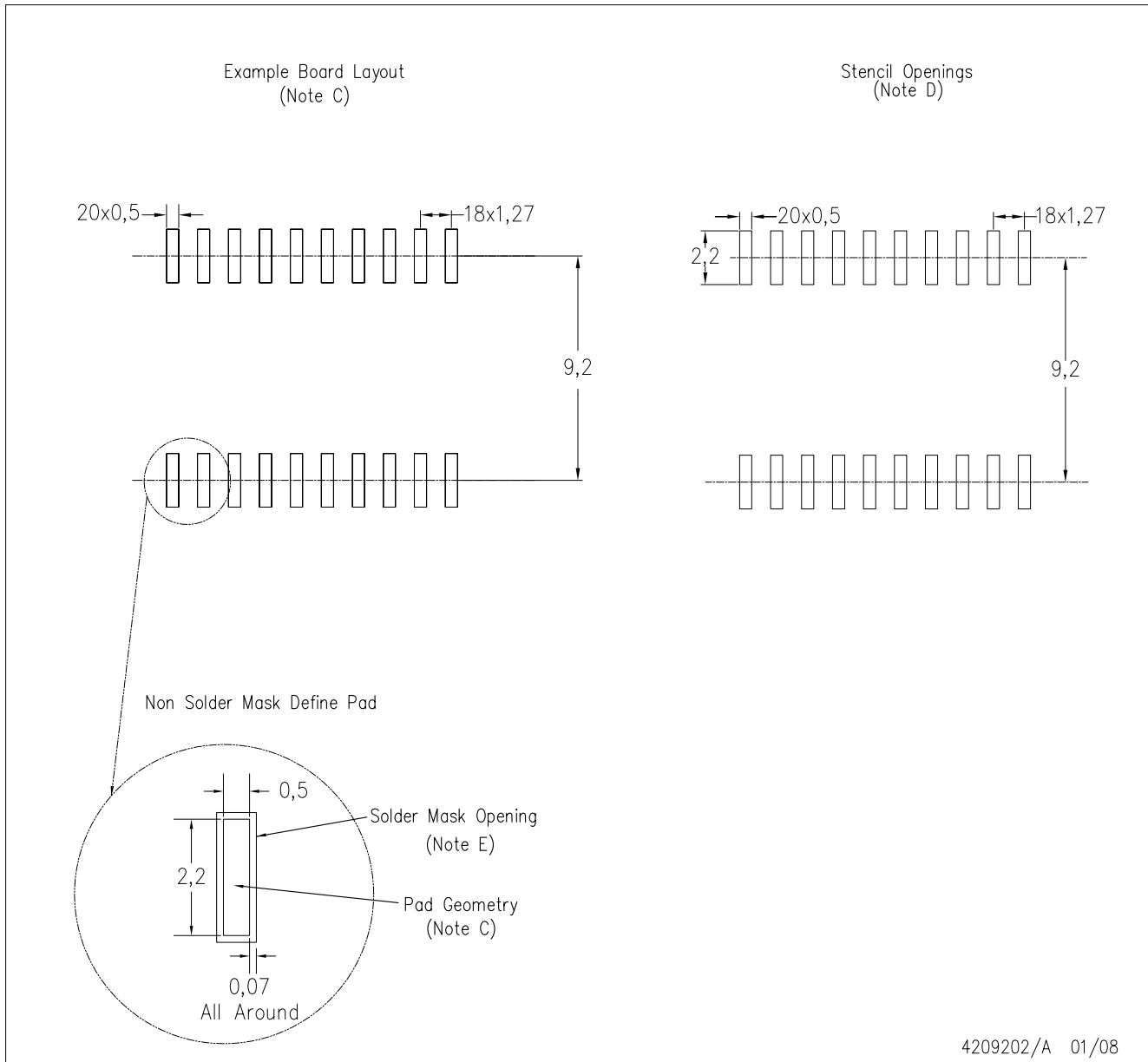


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- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



DW (R-PDSO-G20)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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