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# VSC7216-02

VITESSE

## VSC7216-02 Low Power Quad 1.25Gb/s Backplane Transceiver



### FEATURES:

- ▶ Compatible to Industry Standard VSC7216-01
- ▶ Redundant Transmit and Receive Serial I/O's
- ▶ LVTTTL Parallel Data I/O
- ▶ Rate Matching Between Upstream/Downstream VSC7216-02's
- ▶ Selectable High Speed Input Termination
- ▶ Multi-channel and Multi-chip Aggregation Capability
- ▶ Serial Output Swing Reduction Control
- ▶ Transmitter Pre-Distortion and Receiver Equalization
- ▶ Multiple Clocking Options
- ▶ Internal Serial and Parallel Loopback Modes
- ▶ JTAG and BIST Enabled
- ▶ Optional 8B/10B Encoder/Decoder
- ▶ Fast Lock for use in Asynchronous Switching Applications
- ▶ Adjustable Latency and Deskewing for Varied System Environments
- ▶ Analog Signal Detect for each PECL Input

### SPECIFICATIONS:

- ▶ REFCLK: 24.5 - 136MHz
- ▶ Tx/Rx REFCLK Offset: 200 ppm
- ▶ Serial Input Differential Terminations Adjustable Between 100Ω and 150Ω
- ▶ Fast Lock CRU: <128 DataTransitions
- ▶ Up to 90 Bit Periods of Inter-channel Deskew
- ▶ Tolerates +/- 5 Bit Times of Clock Drift Between Resynchronizations
- ▶ 2.5V Supply, Internal 1.8V Regulator
- ▶ 700 mW Power Dissipation
- ▶ 21 x 21mm, or 27 x 27mm 256-pin Thermally Enhanced Ball Grid Array (TBGA)
- ▶ Maximum Case Temperature: 110°C
- ▶ Offered Extended Temperature Range as VSC7216-06

### APPLICATIONS:

- ▶ Backplane Interconnect for Data Communications
- ▶ Serial Bus Extension
- ▶ Gigabit Ethernet Transceiver
- ▶ Fibre Channel Transceiver
- ▶ Serial Link Redundancy

### SERIAL DATA TRANSFER RATES FOR EACH CHANNEL:

	Full Rate Mode	Half Rate Mode
VSC7216-02	0.98 - 1.36Gb/s	0.49 - 0.68Gb/s

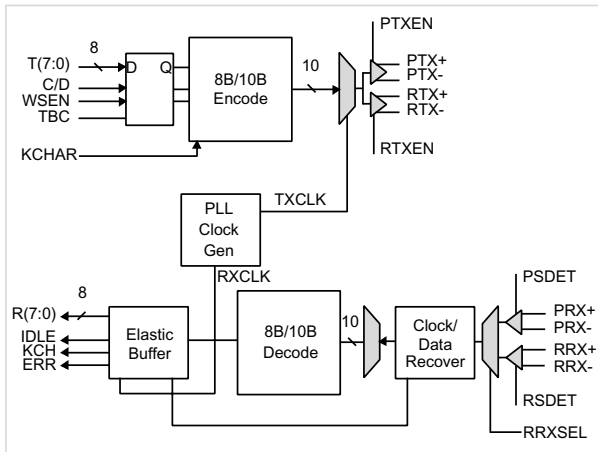
### GENERAL DESCRIPTION:



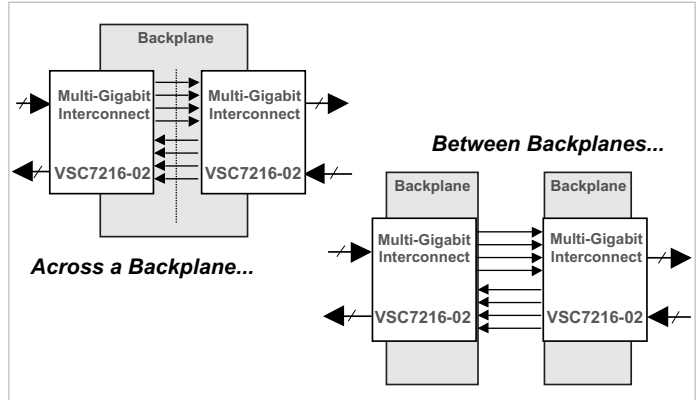
The VSC7216-02 is a quad channel parallel-to-serial and serial-to-parallel transceiver chip designed for use in high bandwidth data transmission between busses, backplanes and other subsystems.

Each channel's transmitter section contains parallel 8-bit or 10-bit input circuitry, an 8B/10B encoder, serializer and a pair of serial PECL output drivers and additional control inputs. Each channel's receiver section contains a pair of PECL inputs, clock and data recovery circuitry, a deserializer, an 8B/10B decoder, elastic buffers, 8-bit or 10-bit output drivers and additional control outputs. Each transmitter may be supplied 8-bit data which will be encoded into 10-bit characters for transmission, or may be supplied pre-encoded 10-bit data in which case the internal encoder is bypassed. The four channels may operate independently or in a synchronized mode transferring data that is word-aligned across 16 or 32 data inputs.

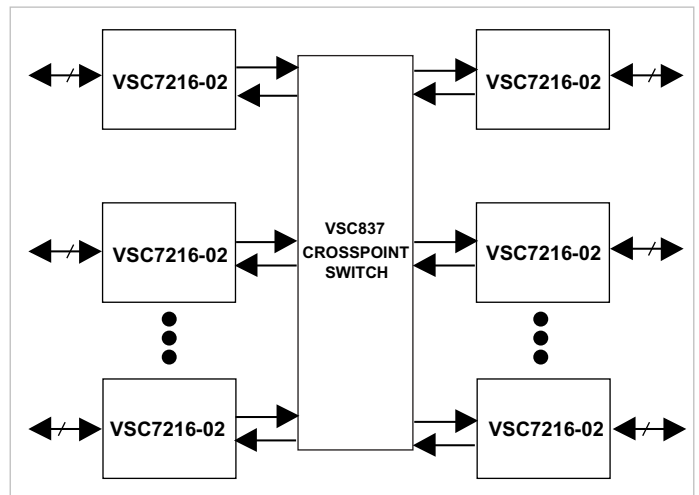
### VSC7216-02 BLOCK DIAGRAM: (Single Channel Shown)



### VSC7216-02 TWO APPLICATIONS:



### VSC7216-02 CONNECTION TO VITESSE'S CROSSPOINT PRODUCTS:



### Your Partner for Success.

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