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DATACOM PRODUCTS

# VSC7145

VITESSE

## VSC7145 - Dual Speed 10-bit Serializer/Deserializer


### FEATURES:

- Dual Speed Operation:
  - Fibre Channel: 1.06/2.12Gb/s
  - Gigabit Ethernet: 1.25Gb/s
  - InfiniBand™: 2.5Gb/s
- 10-bit, SSTL_2 or SSTL_3 Interface
- HSPI Interface Compliant
- ASIC-Friendly™ Timing to the Transmitter
- Separate Transmitter/Receiver Rate Controls support Auto Speed Negotiation
- No Passives needed on High Speed Signals
- On-chip, 100 Ohm Termination
- Write Pre-Emphasis in Transmitter
- Cable Equalization in Receiver
- Analog/Digital Signal Detection
- Flexible Reference Clock
- Single 3.3V Supply, 800mW
- 64-pin, 14 mm PQFP Package
- Pin Compatible to Agilent HDMP-263x

### SPECIFICATIONS:

- Data Rate: 1.0 - 2.5 Gb/s
- REFCLK: 52.5 to 126 MHz
- Frequency Offset: +/-200 ppm
- Fast Locking: <300 data edges
- Transmitter Output: 1.0V p-p Minimum
- Receiver Input: 200mV p-p Minimum
- 3.3V +/- 5% Supply
- 0° - 70°C Ambient Operation

### APPLICATIONS:

- Fibre Channel
  - -Host Adapters
  - -Hubs/Switches
  - -RAID systems
- Gigabit Ethernet
  - -NICs
  - -Switches
  - -Proprietary Uplinks
- InfiniBand
  - -Host Channel Adapters
  - -Target Channel Adapters
  - -Switches
- Proprietary Serial Links

### PRODUCT OPTIONS:

| Part Number | Low Speed I/O | Speed (Gb/s) | HS Termination | Compatibility |
|---|---|---|---|---|
| VSC7145RU-30 | SSTL_2 | 1.05 - 1.26 (Half Speed) or 2.10 - 2.52 (Full Speed) | 100 Ohms | Agilent HDMP-2630 |
| VSC7145RU-31 | SSTL_3 | | | Agilent HDMP-2631 |
| VSC7145RU-34 | SSTL_2 | | | Agilent HDMP-2634 |

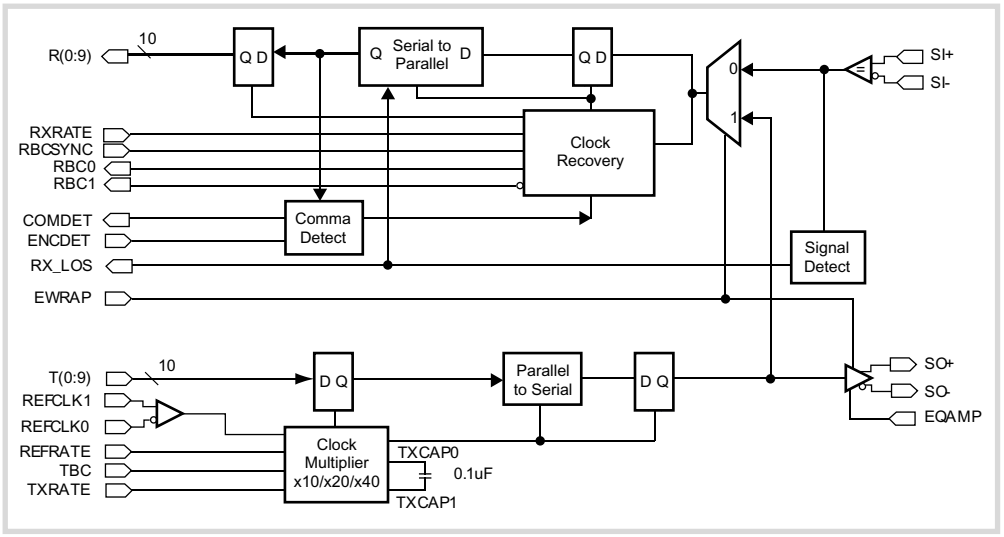
# VSC7145

## VSC7145 - Dual Speed 10-bit Serializer/Deserializer

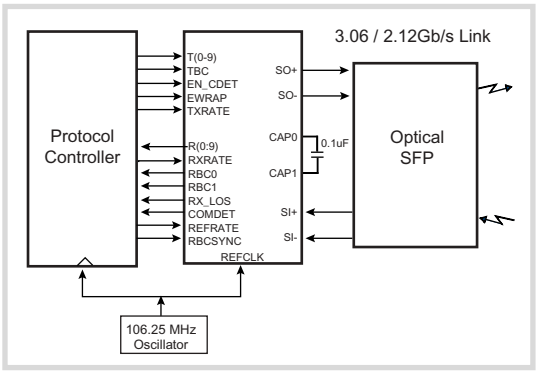
### GENERAL DESCRIPTION:


The VSC7145 is a dual-speed Fibre Channel, Gigabit Ethernet and InfiniBand Serializer/Deserializer (SerDes) optimized for performance and power in an industry-standard pinout. It accepts 10-bits of SSTL, 8B/10B encoded transmit data, latches it synchronously to the Transmit Byte Clock (TBC) and serializes it onto the SO differential output at a baud rate which is 10, 20 or 40 times the REFCLK frequency. The VSC7145 samples serial receive data on the SI input, recovers the clock and data, deserializes it onto a 10-bit SSTL bus and outputs two recovered clocks at 1/10th or 1/20th of the baud rate. Both disparities of the K28.5 characters are detected and used for aligning the serial data to the parallel output bus. Independent speed selectors control the transmitter and receiver separately to support industry-standard automatic speed negotiation protocols. A combined analog/digital signal detect circuit indicates the presence of valid signal levels on the SI input. The VSC7145 contains on-chip PLL circuitry for synthesis of the bit rate transmit clock, and extraction of the clock from the received serial stream. The parallel bus of the VSC7145 is compliant with the High Speed Parallel Interface (HSPI) standard developed by the T11.2 Fibre Channel Committee.

### VSC7145 BLOCK DIAGRAM:




### DUAL SPEED AUTO NEGOTIATION FIBRE CHANNEL APPLICATION:

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VITESSE

**741 Calle Plano**
**Camarillo, CA 93012**
**Tel: 805.388.3700**
**Fax: 805.388.7565**
**www.vitesse.com**