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HCPL-0872
Digital Interface IC

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

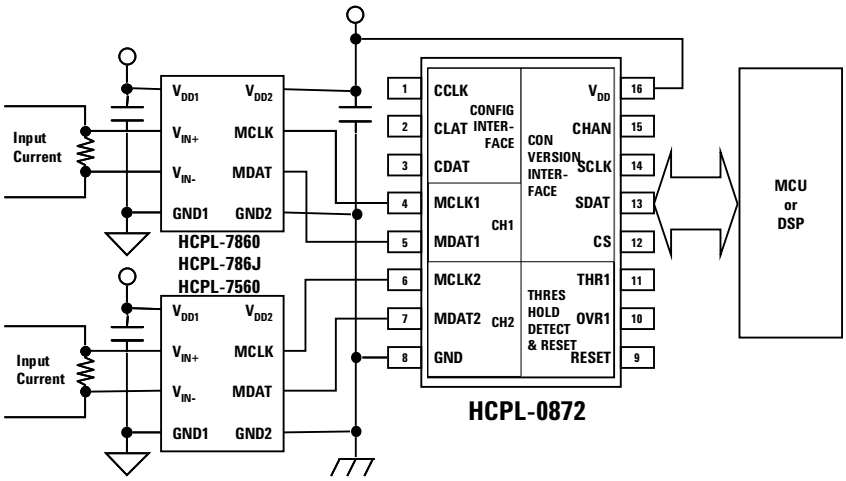
The Digital Interface IC, HCPL-0872 converts the single-bit data stream from the Isolated Modulator (such as HCPL-7860/786J/7560) into fifteen-bit output words and provides a serial output interface that is compatible with SPI®, QSPI®, and Microwire® protocols, allowing direct connection to a microcontroller. The Digital Interface IC, HCPL-0872 is available in a 300-mil wide SO-16 surface-mount package. Features of the Digital Interface IC include five different conversion modes, three different pre-trigger modes, offset calibration, fast over-range detection, and adjustable threshold detection. Programmable features are configured via the Serial Configuration port. A second multiplexed input is available to allow measurements with a second isolated modulator without additional hardware.

Features

- Interface between HCPL-7860/786J/7560 and MCU/DSP
- 5 Conversion Modes for Resolution/Speed Trade-Off
- 3 Pre-Trigger Modes
- Offset Calibration
- Fast 3 µs Over-Range Detection
- Adjustable Threshold Detection
- Serial I/O (SPI®, QSPI® and Microwire Compatible)
- Offset Calibration
- -40°C to +85°C Operating Temperature Range

Applications

- Motor Phase and Rail Current Sensing
- Data Acquisition Systems
- Industrial Process Control
- Inverter Current Sensing
- General Purpose Current Sensing and Monitoring



A 0.1 µF bypass capacitor must be connected between pins V_{DD} and Ground

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.

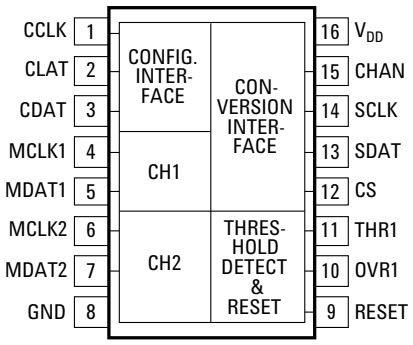
SPI and QSPI are trademarks of Motorola Corp.

Microwire is a trademark of National Semiconductor Inc.

HCPL-0872 Digital Interface IC

Because the two inputs are multiplexed, only one conversion at a time can be made and not all features are available for the second channel. The available features for both channels are shown in the table below

Feature	Channel 1	Channel 2
Conversion Mode	•	•
Offset Calibration	•	•
Pre-Trigger Mode	•	
Over-Range Detection	•	
Adjustable Threshold Detection	•	



Pin Description, Digital Interface IC

Symbol	Description
CCLK	Clock input for the Serial Configuration Interface (SCI). Serial Configuration data is clocked in on the rising edge of CCLK.
CLAT	Latch input for the Serial Configuration Interface (SCI). The last 8 data bits clocked in on CDAT by CCLK are latched into the appropriate configuration register on the rising edge of CLAT.
CDAT	Data input for the Serial Configuration Interface (SCI). Serial configuration data is clocked in MSB first.
MCLK1	Channel 1 Isolated Modulator clock input. Input Data on MDAT1 is clocked in on the rising edge of MCLK1.
MDAT1	Channel 1 Isolated Modulator data input.
MCLK2	Channel 2 Isolated Modulator clock input. Input Data on MDAT2 is clocked in on the rising edge of MCLK2.
MDAT2	Channel 2 Isolated Modulator data input.
GND	Digital ground.
VDD	Supply voltage (4.5 V to 5.5 V).
CHAN	Channel select input. The input level on CHAN determines which channel of data is used during the next conversion cycle. An input low selects channel 1, a high selects channel 2.
SCLK	Serial clock input. Serial data is clocked out of SDAT on the falling edge of SCLK.
SDAT	Serial data output. SDAT changes from high impedance to a logic low output at the start of a conversion cycle. SDAT then goes high to indicate that data is ready to be clocked out. SDAT returns to a high-impedance state after all data has been clocked out and CS has been brought high. SDAT goes high immediately after RESET is released.
CS	Conversion start input. Conversion begins on the falling edge of CS. CS should remain low during the entire conversion cycle and then be brought high to conclude the cycle.
THR1	Continuous, programmable-threshold detection for channel 1 input data. A high level output on THR1 indicates that the magnitude of the channel 1 input signal is beyond a user programmable threshold level between 160 mV and 310 mV. This signal continuously monitors channel 1 independent of the channel select (CHAN) signal.
OVR1	High speed continuous over-range detection for channel 1 input data. A high level output on OVR1 indicates that the magnitude of the channel 1 input is beyond full-scale. This signal continuously monitors channel 1 independent of the CHAN signal.
RESET	Master reset input. A logic high input for at least 100 ns asynchronously resets all configuration registers to their default values and zeroes the Offset Calibration registers.

Ordering Information

Part number	Option: RoHS Compliant	Option: Non-RoHS Compliant	Package	Surface Mount	Tape & Reel	Quantity
HCPL-0872	-000E	No option	SO-16	X		47 per tube
	-500E	-500		X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-0872-500E to order product of 16-Pin SO package in Tape and Reel packaging in RoHS compliant.

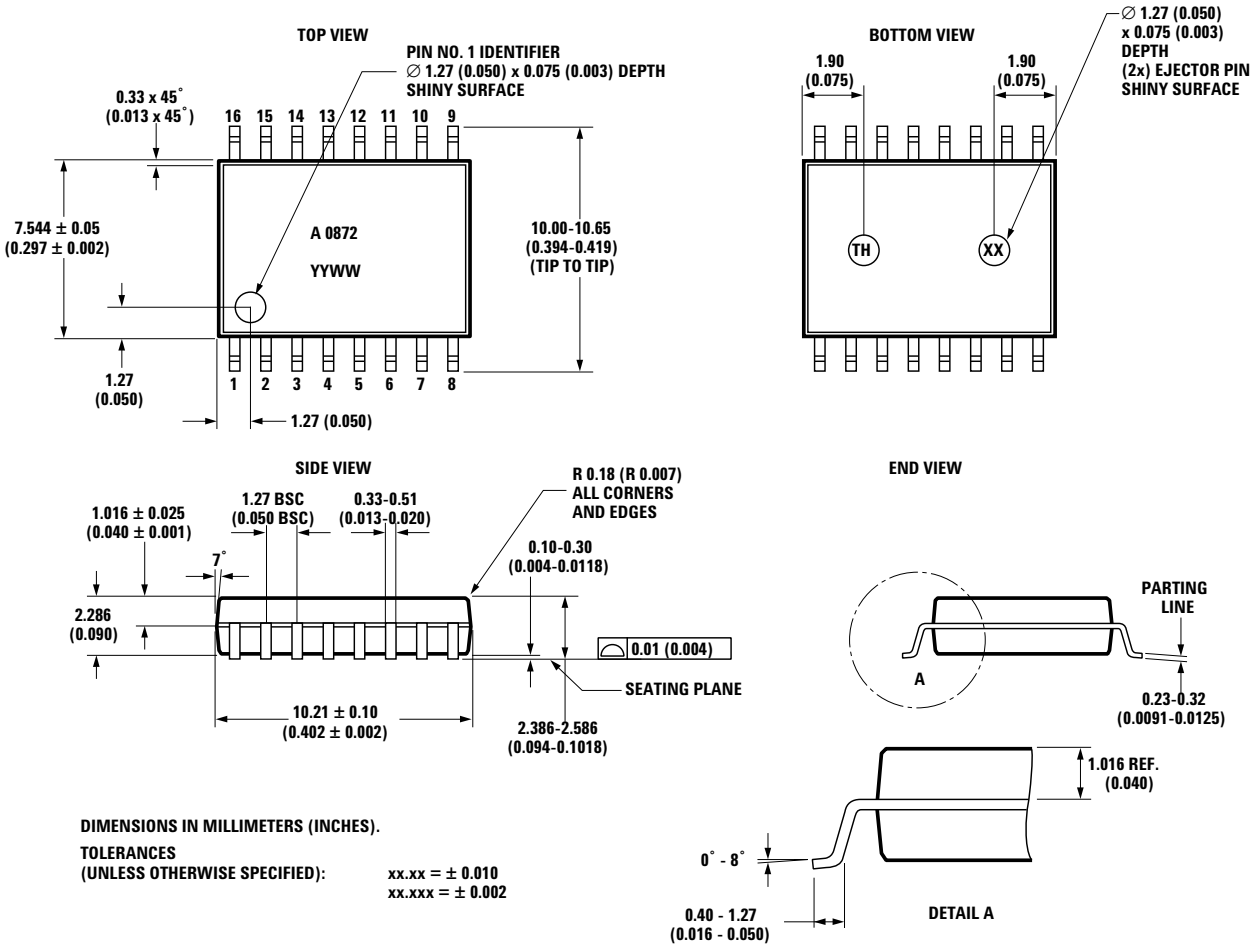
Example 2:

HCPL-0872 to order product of 16-Pin SO package in tube packaging and non-RoHS compliant.

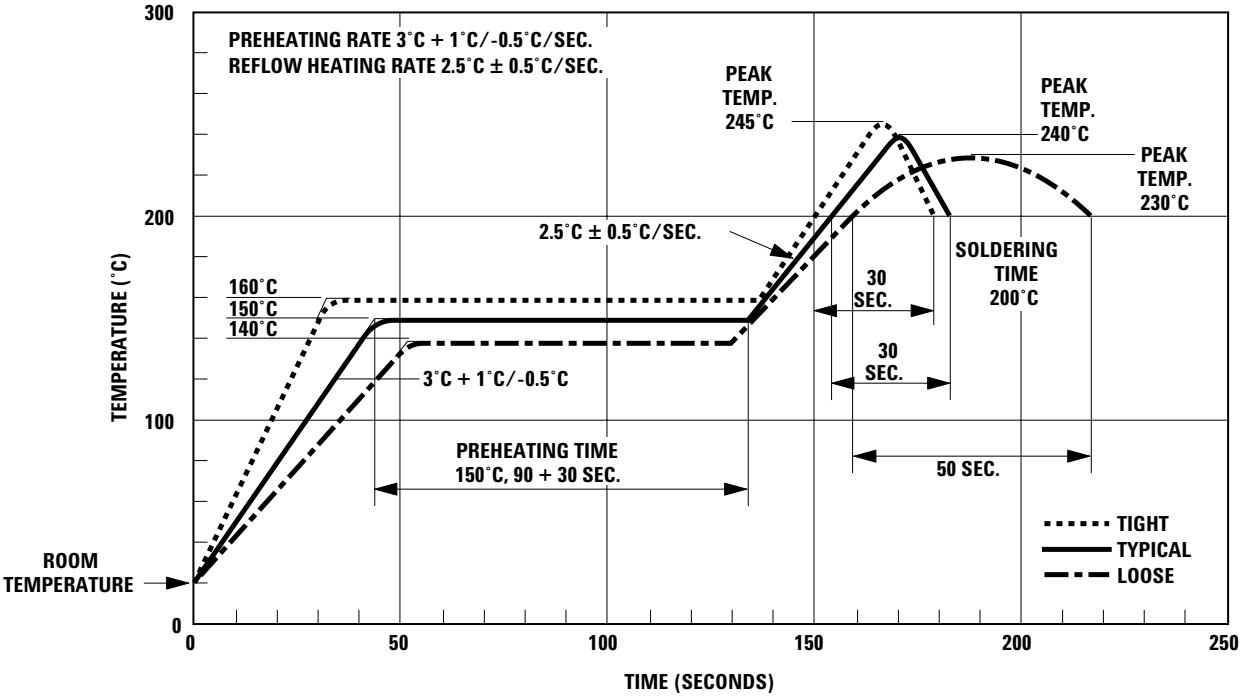
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

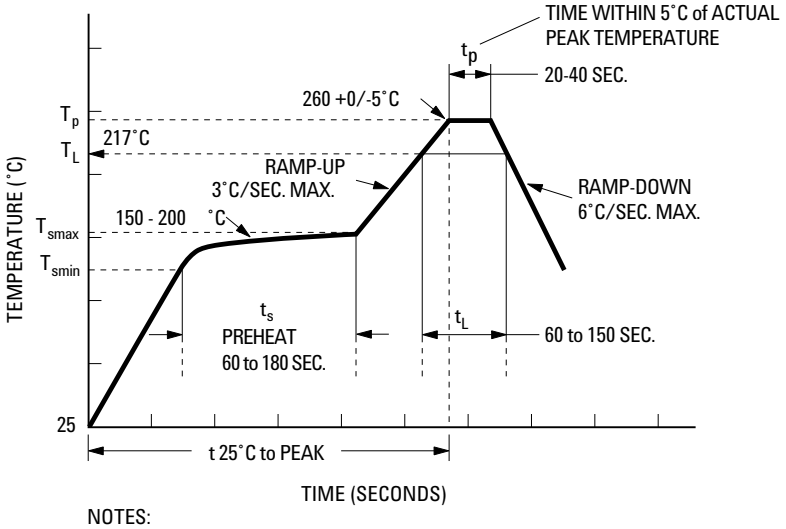
Package Outline Drawings
Standard 16-pin SO Package



Solder Reflow Temperature Profile



Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200˚C, T_{smin} = 150˚C

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	85	°C	
Supply Voltage	V_{DD}	0	5.5	V	
Input Voltage	All Inputs	-0.5	V_{DD} + 0.5	V	
Output Voltage	All Outputs	-0.5	V_{DD} + 0.5	V	
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				1
Solder Reflow Temperature Profile	See Reflow Thermal Profile				

Notes 1. Avago Technologies recommends the use of non-chlorinated solder fluxes.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	85	°C
Supply Voltage	V_{DD}	4.5	5.5	V
Input Voltage	All Inputs	0	V_{DD}	V

Electrical Specifications (DC)

Unless otherwise noted, all Typical specifications are at T_A = 25°C and V_{DD} = 5 V, and all Minimum and Maximum specifications apply over the following ranges: T_A = -40°C to +85°C and V_{DD} = 4.5 to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.
Supply Current	I_{DD}		3	5	mA	f_{CLK} = 10 MHz	
DC Input Current	I_{IN}		0.001	10	µA		
Input Logic Low Voltage	V_{IL}			0.8	V		
Input Logic High Voltage	V_{IH}	3.6			V		
Output Logic Low Voltage	V_{OL}		0.15	0.4	V	I_{OUT} = 4 mA	
Output Logic High Voltage	V_{OH}	4.3	5.0		V	I_{OUT} = -400 µA	
Clock Frequency (CCLK, MCLK and SCLK)	f_{CLK}			20	MHz		
Clock Period (CCLK, MCLK and SCLK)	t_{PER}	50			ns		2, 3
Clock High Level Pulse Width (CCLK, MCLK and SCLK)	t_{PWH}	20			ns		2, 3
Clock Low Level Pulse Width (CCLK, MCLK and SCLK)	t_{PWL}	20			ns		2, 3
Setup Time from DAT to Rising Edge of CLK (CDAT, CCLK, MDAT and MCLK)	t_{SUCLK}	10			ns		2
DAT Hold Time after Rising Edge of CLK (CDAT, CCLK, MDAT and MCLK)	t_{HDCLK}	10			ns		2
Setup Time from Falling Edge of CLAT to First Rising Edge of CCLK	t_{SUCL1}	20			ns		2
Setup Time from Last Rising Edge of CCLK to Rising Edge of CLAT	t_{SUCL2}	20			ns		2
Delay Time from Falling Edge of SCLK to SDAT	t_{DSDAT}			15	ns		3
Setup Time from Data Ready to First Falling Edge of SCLK	t_{SUS}	200			ns		3
Setup Time from CHAN to falling edge of CS	t_{SUCHS}	20			ns		
Reset High Level Pulse Width	t_{PWR}	100			ns		

Notes:
1. Avago Technologies recommends the use of non-chlorinated solder fluxes.

Applications Information

Digital Current Sensing

As shown in Figure 1, using the Isolated 2-chip A/D converter to sense current can be as simple as connecting a current-sensing resistor, or shunt, to the input and reading output data through the 3-wire serial output interface. By choosing the appropriate shunt resistance, any range of current can be monitored, from less than 1 A to more than 100 A.

Even better performance can be achieved by fully utilizing the more advanced features of the Isolated A/D converter, such as the pre-trigger circuit, which can reduce conversion time to less than 1µs, the fast over-range detector for quickly detecting short circuits, different conversion modes giving various resolution/ speed trade-offs, offset calibration mode to eliminate initial offset from measurements, and an adjustable threshold detector for detecting non-short circuit overload conditions.

Product Description

The Digital Interface IC, HCPL-0872 converts the single-bit data stream from the Isolated Modulator (such as HCPL-7860/786J/7560) into fifteen-bit output words and provides a serial output interface that is compatible with SPI®, QSPI®, and Microwire® protocols, allowing direct connection to a microcontroller. A second multiplexed input is available to allow measurements with a second isolated modulator without additional hardware.

The Digital Interface IC, HCPL-0872 can used together with Isolated Modulator, HCPL-7860/786J/7560 to form an isolated programmable two-chip analog-to-digital converter. The primary functions of the HCPL-0872 Digital Interface IC are to derive a multi-bit output signal by averaging the single-bit modulator data, as well as to provide a direct microcontroller interface. The effective resolution of the multi-bit output signal is a function of the length of time (measured in modulator clock cycles) over which the average is taken; averaging over longer periods of time results in higher resolution. The Digital Interface IC can be configured for five conversion modes, which have different combinations of speed and resolution to achieve the desired level of performance. Other functions of the HCPL-0872 Digital Interface IC include a Phase Locked Loop based pre-trigger circuit that can either give more precise control of the effective sampling time or reduce conversion time to less than 1µs, a fast over-range detection circuit that rapidly indicates when the magnitude of the input signal is beyond full-scale, an adjustable threshold detection circuit that indicates when the magnitude of the input signal is above a user adjustable threshold level, an offset calibration circuit, and a second multiplexed input that allows a second Isolated Modulator to be used with a single Digital Interface IC.

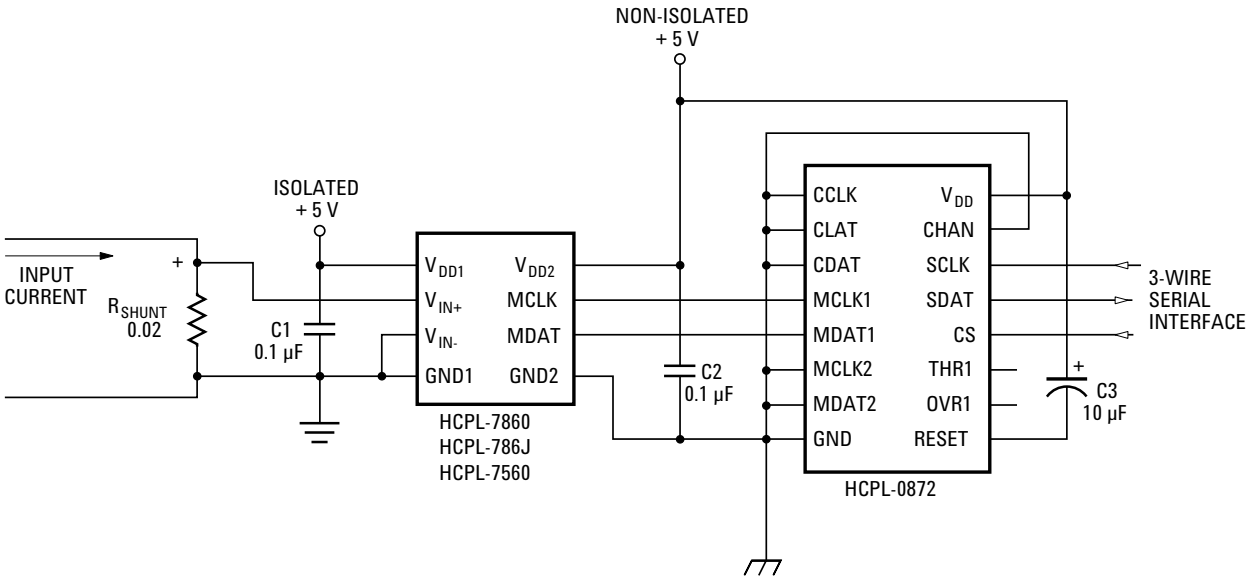


Figure 1. Typical Application Circuit.

Digital Interface Timing

Power Up/Reset

At power up, the digital interface IC should be reset either manually, by bringing the RESET pin (pin 9) high for at least 100 ns, or automatically by connecting a 10µF capacitor between the RESET pin and V_{DD} (pin 16). The RESET pin operates asynchronously and places the IC in its default configuration, as specified in the Digital Interface Configuration section.

Conversion Timing

Figure 2 illustrates the timing for one complete conversion cycle. A conversion cycle is initiated on the falling edge of the convert start signal (CS); CS should be held low during the entire conversion cycle. When CS is brought low, the serial output data line (SDAT) changes from a high-impedance to the low state, indicating that the converter is busy. A rising edge on SDAT indicates that data is ready to be clocked out. The output data is clocked out on the negative edges of the serial clock pulses (SCLK), MSB first. A total of 16 pulses is needed to clock out all of the data. After the last clock pulse, CS should be brought high again, causing SDAT to return to a high-impedance state, completing the conversion cycle. If the external circuit uses the positive edges of SCLK to clock in the data, then a total of sixteen bits is clocked in, the first bit is always high (indicating that data is ready) followed by 15 data bits. If fewer than 16 cycles of SCLK are input before CS is brought high, the conversion cycle will terminate and SDAT will go to the high-impedance state after a few cycles of the Isolated Modulator's clock.

The amount of time between the falling edge of CS and the rising edge of SDAT depends on which conversion and pre-trigger modes are selected; it can be as low as 0.7µs when using pre-trigger mode 2, as explained in the Digital Interface Configuration section.

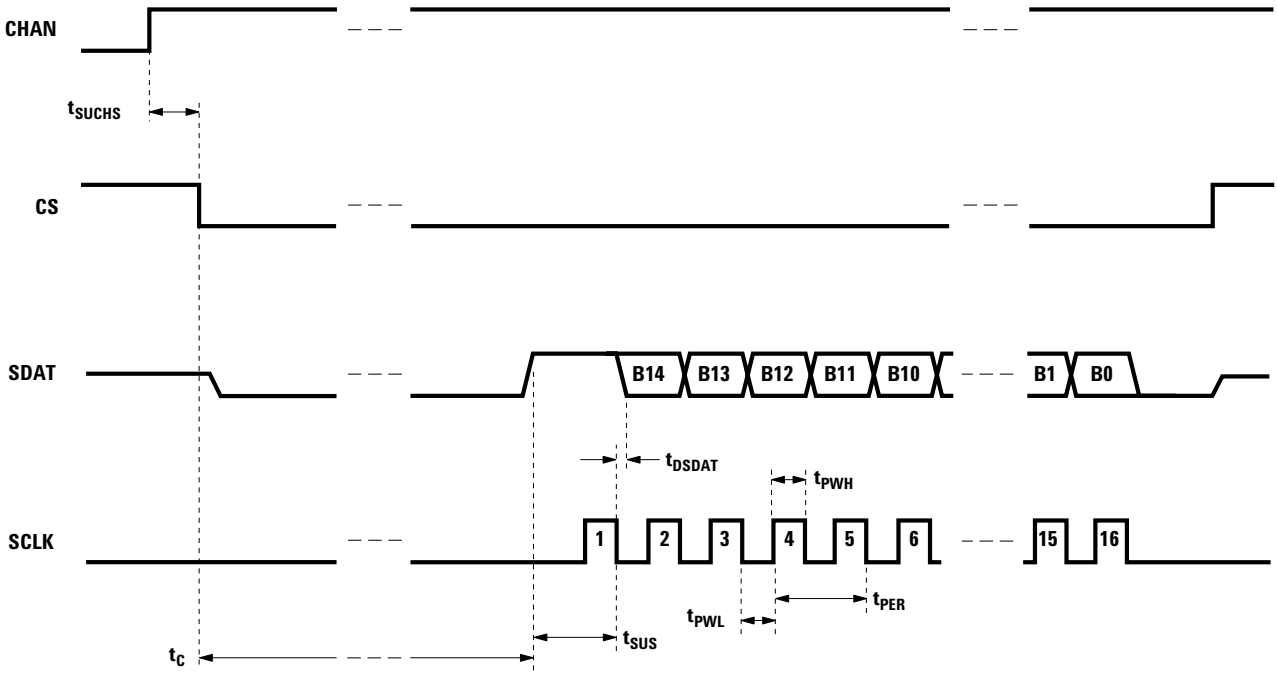


Figure 2. Conversion Timing.

Serial Configuration Timing

The HCPL-0872 Digital Interface IC is programmed using the Serial Configuration Interface (SCI), which consists of the clock (CCLK), data (CDAT), and enable/latch (CLAT) signals. Figure 3 illustrates the timing for the serial configuration interface. To send a byte of configuration data to the HCPL-0872, first bring CLAT low. Then clock in the eight bits of the configuration byte (MSB first) using CDAT and the rising edge of CCLK. After the last bit has been clocked in, bringing CLAT high again will latch the data into the appropriate configuration register inside the interface IC. If more than eight bits are clocked in before CLAT is brought high, only the last eight bits will be used. Refer to the Digital Interface Configuration section to determine appropriate configuration data. If the default configuration of the digital interface IC is acceptable, then CCLK, CDIN and CLAT may be connected to either V_{DD} or GND.

Channel Select Timing

The channel select signal (CHAN) determines which input channel will be used for the next conversion cycle. A logic low level selects channel one, a high level selects channel 2. CHAN should not be changed during a conversion cycle. The state of the CHAN signal has no effect on the behavior of either the over-range detection circuit (OVR1) or the adjustable threshold detection circuit (THR1). Both OVR1 and THR1 continuously monitor channel 1 independent of the CHAN signal. CHAN also does not affect the behavior of the pre-trigger circuit, which is tied to the conversion timing of channel 1, as explained in the Digital Interface Configuration section.

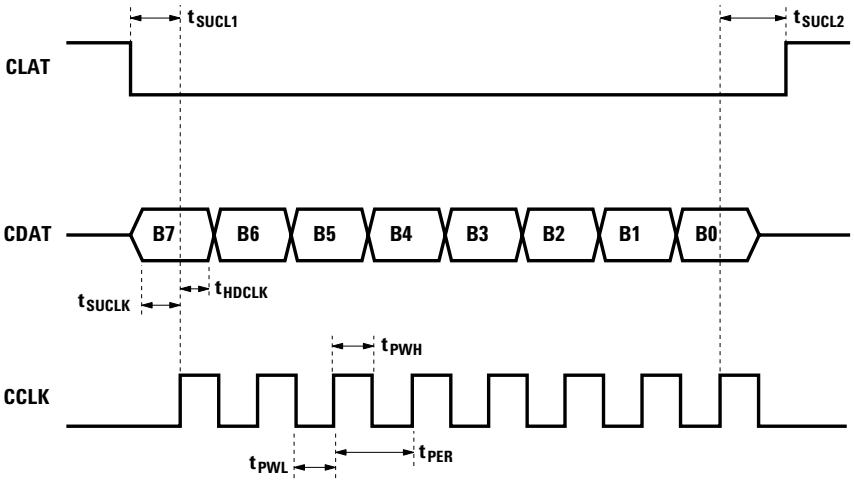


Figure 3. Serial Configuration Interface Timing.

Digital Interface Configuration

Configuration Registers

The Digital Interface IC contains four 6-bit configuration registers that control its behavior. The two LSBs of any byte clocked into the serial configuration port (CDAT, CCLK, CLAT) are used as address bits to determine which register the data will be loaded into. Registers 0 and 1 (with address bits 00 and 01) specify the conversion and offset calibration modes of channels 1 and 2, register 2 (address bits 10) specifies the behavior of the adjustable threshold circuit, and register 3 (address bits 11) specifies which pre-trigger mode to use for channel 1. These registers are illustrated in Table 1 below, with default values indicated in bold italic type. Note that there are several reserved bits, which should always be set low and that the configuration registers should not be changed during a conversion cycle.

Conversion Mode

The conversion mode determines the speed/resolution trade-off for the Isolated A/D converter. The four MSBs of registers 0 and 1 determine the conversion mode for the appropriate channel. The bit settings for choosing a particular conversion mode are shown in Table 2 below. Combinations of data bits not specified in Table 2 below are not recommended.

Table 1. Register Configuration.

	Configuration Data Bits						Address Bit	
Register	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Channel 1 Conversion Mode				Channel 1 Offset Cal	Reserved		
	High	High	Low	Low	Low	Low	Low	Low
1	Channel 2 Conversion Mode				Channel 2 Offset Cal	Reserved		
	High	High	Low	Low	Low	Low	Low	High
2	Threshold Detection Time		Threshold Level					
	High	Low	Low	Low	Low	Low	High	Low
3	Pre-Trigger Mode		Reserved					
	Low	Low	Low	Low	Low	Low	High	High

Notes: Bold italic type indicates Default values. Reserved bits should be set low.

Table 2. Conversion Mode Configuration.

Conversion Mode	Configuration Data Bits			
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**
1	Low	High	Low	High
2	Low	Low	High	High
3	High	High	High	Low
4	High	High	Low	Low
5	High	Low	High	Low

Notes: Bold italic type indicates Default values.

Pre-Trigger Mode

The pre-trigger mode refers to the operation of a PLL-based circuit that affects the sampling behavior and conversion time of the A/D converter when channel 1 is selected. The PLL pre-trigger circuit has two modes of operation; the first mode allows more precise control of the time at which the analog input voltage is effectively sampled, while the second mode essentially eliminates the time between when the external convert start command is given and when output data is available (reducing it to less than 1µs). A brief description of how the A/D converter works with the pre-trigger circuit disabled will help explain how the pre-trigger circuit affects operation when it is enabled.

With the pre-trigger circuit is disabled (pre-trigger mode 0), Figure 4 illustrates the relationship between the convert start command, the weighting function used to average the modulator data, and the data ready signal. The weighted averaging of the modulator data begins immediately following the convert start command. The weighting function increases for half of the conversion cycle and then decreases back to zero, at which time the data ready signal is given, completing the conversion cycle. The analog signal is effectively sampled at the peak of the weighting function, half-way through the conversion cycle. This is the default mode.

If the convert start signal is periodic (i.e., at a fixed frequency) and the PLL pre-trigger circuit is enabled (pre-trigger modes 1 or 2), either the peak of the weighting function or the end of the conversion cycle can be aligned to the external convert start command, as shown in Figure 4. The Digital Interface IC can therefore synchronize the conversion cycle so that either the beginning, the middle, or the end of the conversion is aligned with the external convert start command, depending on whether pre-trigger mode 0, 1, or 2 is selected, respectively. The only requirement is that the convert start signal for channel 1 be periodic. If the signal is not periodic and pre-trigger mode 1 or 2 is selected, then the pre-trigger circuit will not function properly.

An important distinction should be made concerning the difference between conversion time and signal delay. As can be seen in Figure 4, the amount of time from the peak of the weighting function (when the input signal is being sampled) to when output data is ready is the same for all three modes. This is the actual delay of the analog signal through the A/D converter and is independent of the "conversion time," which is simply the time between the convert start signal and the data ready signal. Because signal delay is the true measure of how much phase shift the A/D converter adds to the signal, it should be used when making calculations of phase margin and loop stability in feedback systems.

There are different reasons for using each of the pre-trigger modes. If the signal is not periodic, then the pre-trigger circuit should be disabled by selecting pre-trigger mode 0. If the most time-accurate sampling of the input signal is desired, then mode 1 should be selected. If the shortest possible conversion time is desired, then mode 2 should be selected. The pre-trigger circuit functions only with channel 1; the circuit ignores any convert start signals while channel 2 is selected with the CHAN input. This allows conversions on channel 2 to be performed between conversions on channel 1 without affecting the operation of the pre-trigger circuit. As long as the convert start signals are periodic while channel 1 is selected, then the pre-trigger circuit will function properly. The three different pre-trigger modes are selected using bits 6 and 7 of register 3, as shown in Table 3 below.

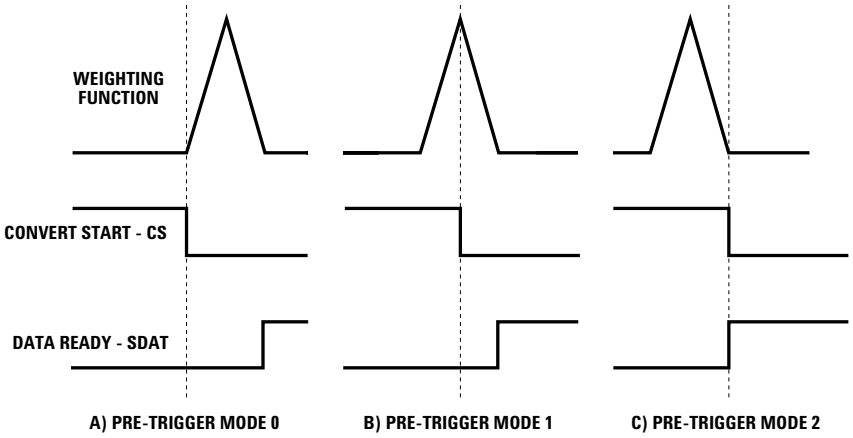


Figure 4. Pre-Trigger Modes 0, 1, and 2.

Table 3. Pre-Trigger Mode Configuration.

Pre-Trigger Mode	Configuration Data Bits	
	Bit 7	**Bit 6**
0	Low	Low
1	Low	High
2	High	Don't Care

Notes: Bold italic type indicates Default values.

Table 4. Offset Calibration Configuration.

Offset Calibration Mode	Configuration Data Bits
	Bit 3
Off	Low
On	High

Notes: Bold italic type indicates Default values.

Offset Calibration

The offset calibration circuit can be used to separately calibrate the offsets of both channels 1 and 2. The offset calibration circuit contains a separate offset register for each channel. After an offset calibration sequence, the offset registers will contain a value equal to the measured offset, which will then be subtracted from all subsequent conversions. A hardware reset (bringing the RESET pin high for at least 100 ns) is required to reset the offset calibration registers to zero.

The following sequence is recommended for performing an offset calibration:

1. Select the appropriate channel using the CHAN pin (low = channel 1, high = channel 2).
2. Force zero volts at the input of the selected isolated modulator.
3. Send a configuration data byte to the appropriate register for the selected channel (register 0 for channel 1, register 1 for channel 2). Bit 3 of the configuration byte should be set high to enable offset calibration mode and bits 4 through 7 should be set to select conversion mode 1 to achieve the highest resolution measurement of the offset.
4. Perform one complete conversion cycle by bringing CS low until SDAT goes high, indicating completion of the conversion cycle. Because bit 3 of the configuration has been set high, the uncalibrated output data from the conversion will be stored in the appropriate offset calibration register and will be subtracted from all subsequent conversions on that channel. If multiple conversion cycles are performed while the offset calibration mode is enabled, the uncalibrated data from the last conversion cycle will be stored in the offset calibration register.
5. Send another configuration byte to the appropriate register for the selected channel, setting bit 3 low to disable calibration mode and setting bits 4 through 7 to select the desired conversion mode for subsequent conversions on that channel.

To calibrate both channels, perform the above sequence for each channel. The offset calibration sequence can be performed as often as needed. Table 4 below summarizes how to turn the offset calibration mode on or off using bit 3 of configuration registers 0 and 1.

Over-Range Detection

The over-range detection circuit allows fast detection of when the magnitude of the input signal on channel 1 is near or beyond full-scale, causing the OVR1 output to go high. This circuit can be very useful in current-sensing applications for quickly detecting when a short-circuit occurs. The over-range detection circuit works by detecting when the modulator output data has not changed state for at least 25 clock cycles in a row, indicating that the input signal is near or beyond full-scale, positive or negative. Typical response time to over-range signals is less than 3µs.

The over-range circuit actually begins to indicate an over-range condition when the magnitude of the input signal exceeds approximately 250 mV; it starts to generate periodic short pulses on OVR1, which get longer and more frequent as the input signal approaches full scale. The OVR1 output stays high continuously when the input is beyond full-scale.

The over-range detection circuit continuously monitors channel 1 independent of which channel is selected with the CHAN signal. This allows continuous monitoring of channel 1 for faults while converting an input signal on channel 2.

Adjustable Threshold Detection

The adjustable threshold detector causes the THR1 output to go high when the magnitude of the input signal on channel 1 exceeds a user-defined threshold level. The threshold level can be set to one of 16 different values between approximately 160 mV and 310 mV. The adjustable threshold detector uses a smaller version of the main conversion circuit in combination with a digital comparator to detect when the magnitude of the input signal on channel 1 is beyond the defined threshold level. As with the main conversion circuit, there is a trade-off between speed and resolution with the threshold detector; selecting faster detection times exhibit more noise as the signal passes through the threshold, while slower detection times offer lower noise. Both the detection time and threshold level are programmable using bits 2 through 7 of configuration register 2, as shown in Tables 5 and 6 below.

As with the over-range detector, the adjustable threshold detector continuously monitors channel 1 independent of which channel is selected with the CHAN signal. This allows continuous monitoring of channel 1 for faults while converting Channel 2.

Table 5. Threshold Detection Configuration.

Threshold Detection Time	Configuration Data Bits	
	Bit 7	**Bit 6**
2 - 6 µs	Low	Low
3 - 10 µs	Low	High
5 - 20 µs	High	Low
10 - 35 µs	High	High

Notes: Bold italic type indicates Default values.

Table 6. Threshold Level Configuration.

Threshold Level	Configuration Data Bits			
	Bit 5	**Bit 4**	**Bit 3**	**Bit 2**
±160 mV	Low	Low	Low	Low
± 170 mV	Low	Low	Low	High
± 180 mV			High	Low
± 190 mV				High
± 200 mV		High	Low	Low
± 210 mV				High
± 220 mV			High	Low
± 230 mV				High
± 240 mV	High	Low	Low	Low
± 250 mV				High
± 260 mV			High	Low
± 270 mV				High
± 280 mV		High	Low	Low
± 290 mV				High
± 300 mV			High	Low
± 310 mV				High

Notes: Bold italic type indicates Default values.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0411EN - May 14, 2007