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DATA SHEET

SEE THE LAST 2 PAGES OF THIS DATASHEET FOR A LIST OF ERRATA RELATED TO THIS PART.

PDI1394L40

1394 enhanced AV link layer controller

Preliminary specification
Supersedes data of 2000 May 15

2000 Dec 15

Philips
Semiconductors

PHILIPS

1394 enhanced AV link layer controller PDI1394L40

1.0 FEATURES

- IEEE1394a and IEEE1394–1995 Standard Link Layer Controller
- Hardware Support for the IEC61883 International Standard of Digital Interface for Consumer Electronics
- Interface to any IEEE 1394–1995 or 1394a Physical Layer Interface
- 5 V Tolerant I/Os
- Single 3.3 V supply voltage
- Full-duplex isochronous operation
- Operates with 400/200/100 Mbps physical layer devices
- 12K byte fully programmable FIFO pool for isochronous and asynchronous data
- Supports single capacitor isolation mode and IEEE 1394–1995, Annex J. isolation
- 6-field deep SYT buffer added to enhance real-time isochronous synchronization using the AVFSYNC pin
- Generates its own AV port clocks under software control. Select one of three frequencies: 24.576, 12.288, or 6.144 MHz
- On chip timer resources
- Flexible 8/16 bit multiplexed/non-multiplexed host interface
- Parallel AV interface

2.0 DESCRIPTION

The PDI11394L40, Philips Semiconductors Full Duplex 1394 Audio/Video (AV) Link Layer Controller, is an IEEE 1394a–2000 compliant link layer controller featuring 2 embedded AV layer interfaces.

The application data is packetized according to the IEC 61883 International Standard of Interface for Consumer Electronic Audio/Video Equipment. Both AV layer interfaces are byte-wide ports capable of accommodating various MPEG–2 and DVC codecs. A flexible host interface is provided for internal register configuration as well as performing asynchronous data transfers. Both 8 bit and 16 bit wide data paths, as well as multiplexed/non-multiplexed access modes are supported.

The PDI1394L40 is powered by a single 3.3 V power supply and the inputs and outputs are 5 V tolerant. It is available in the LQFP144 package.

3.0 QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C

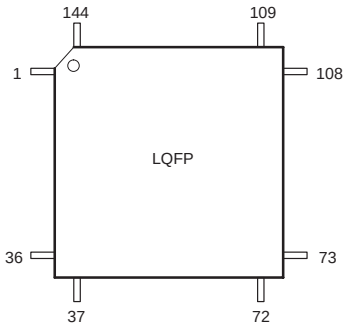
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Functional supply voltage range		3.0	3.3	3.6	V
I_{DD}	Supply current @ V_{DD} = 3.3 V	Operating		110	200	mA
SCLK	Device clock		49.147	49.152	49.157	MHz

4.0 ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
144-pin LQFP144	0 to +70 °C	PDI1394L40BE	PDI1394L40BE	SOT486–1

NOTE:
This datasheet is subject to change.
Please visit our internet website *www.semiconductors.philips.com/1394* for latest changes.

5.0 PIN CONFIGURATION

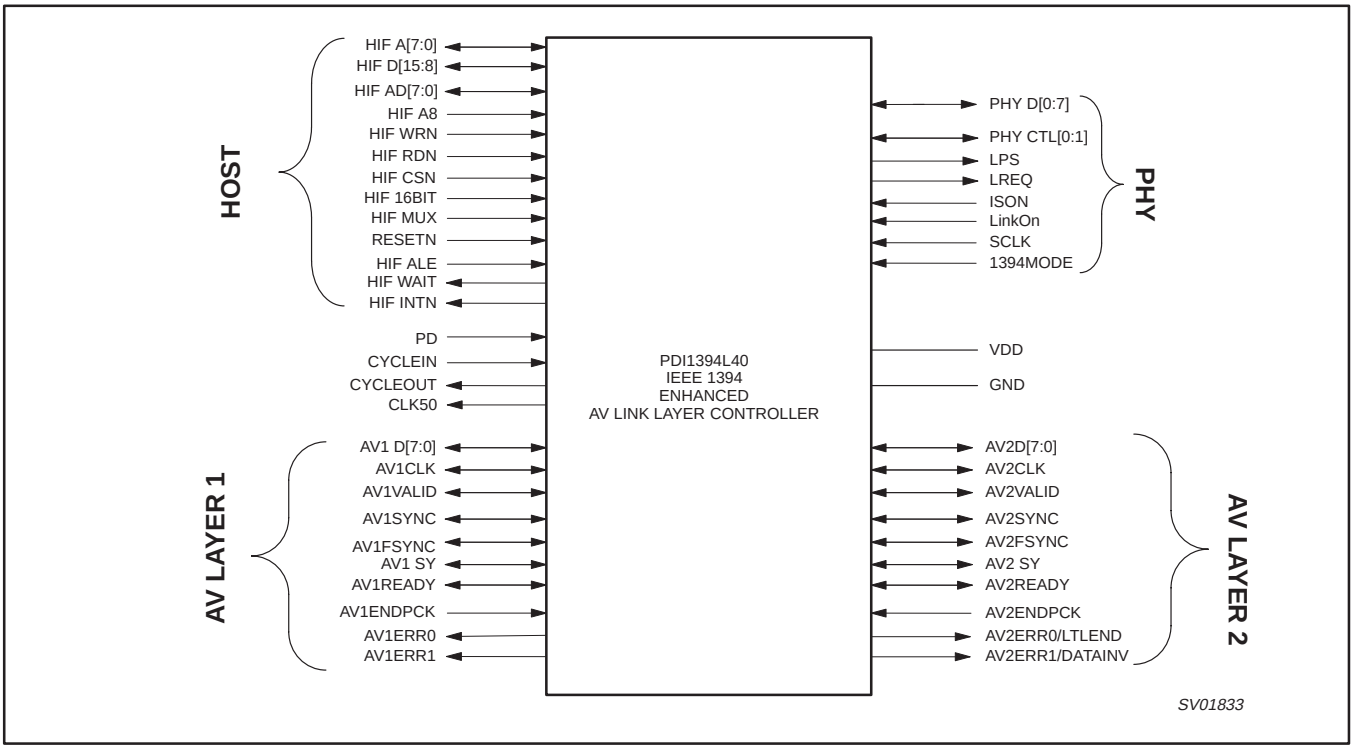


Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HIF D15	37	HIF WRN	73	PHY D7*	109	AV1D1
2	HIF D14	38	HIF INTN	74	PHY D6*	110	AV1D2
3	HIF D13	39	HIF ALE	75	PHY D5*	111	AV1D3
4	HIF D12	40	HIF RDN	76	PHY D4*	112	GND
5	GND	41	HIF WAIT	77	GND	113	V_{DD}
6	V_{DD}	42	RESETN	78	V_{DD}	114	AV1D4
7	HIF D11	43	GND	79	PHY D3*	115	AV1D5
8	HIF D10	44	V_{DD}	80	PHY D2*	116	AV1D6
9	HIF D9	45	HIF 16BIT	81	PHY D1*	117	AV1D7
10	HIF D8	46	HIF MUX	82	PHY D0*	118	AV1READY
11	GND	47	1394 MODE	83	GND	119	GND
12	V_{DD}	48	PD	84	V_{DD}	120	V_{DD}
13	HIF AD7	49	RESERVED	85	PHY CTL1*	121	AV2ERR0/LTLEND
14	HIF AD6	50	RESERVED	86	PHY CTL0*	122	AV2ERR1/DATINV
15	HIF AD5	51	RESERVED	87	LREQ	123	AV2ENDPCK
16	HIF AD4	52	RESERVED	88	SCLK*	124	AV2CLK
17	GND	53	GND	89	GND	125	AV2FSYNC
18	V_{DD}	54	V_{DD}	90	V_{DD}	126	AV2 SY
19	HIF AD3	55	CLK50	91	LPS*	127	AV2VALID
20	HIF AD2	56	CYCLEIN	92	LINKON	128	AV2SYNC
21	HIF AD1	57	CYCLEOUT	93	ISON	129	RESERVED
22	HIF AD0	58	RESERVED	94	GND	130	RESERVED
23	GND	59	RESERVED	95	V_{DD}	131	GND
24	V_{DD}	60	GND	96	AV1ERR0	132	V_{DD}
25	HIF A8	61	V_{DD}	97	AV1ERR1	133	AV2D0
26	HIF A7	62	TESTPIN	98	AV1ENDPCK	134	AV2D1
27	HIF A6	63	TESTPIN	99	AV1CLK	135	AV2D2
28	HIF A5	64	TESTPIN	100	AV1FSYNC	136	AV2D3
29	HIF A4	65	RESERVED	101	AV1 SY	137	GND
30	HIF A3	66	RESERVED	102	AV1VALID	138	V_{DD}
31	HIF A2	67	RESERVED	103	AV1SYNC	139	AV2D4
32	HIF A1	68	RESERVED	104	RESERVED	140	AV2D5
33	HIF A0	69	GND	105	RESERVED	141	AV2D6
34	GND	70	V_{DD}	106	GND	142	AV2D7
35	V_{DD}	71	RESERVED	107	V_{DD}	143	AV2READY
36	HIF CSN	72	RESERVED	108	AV1D0	144	RESERVED

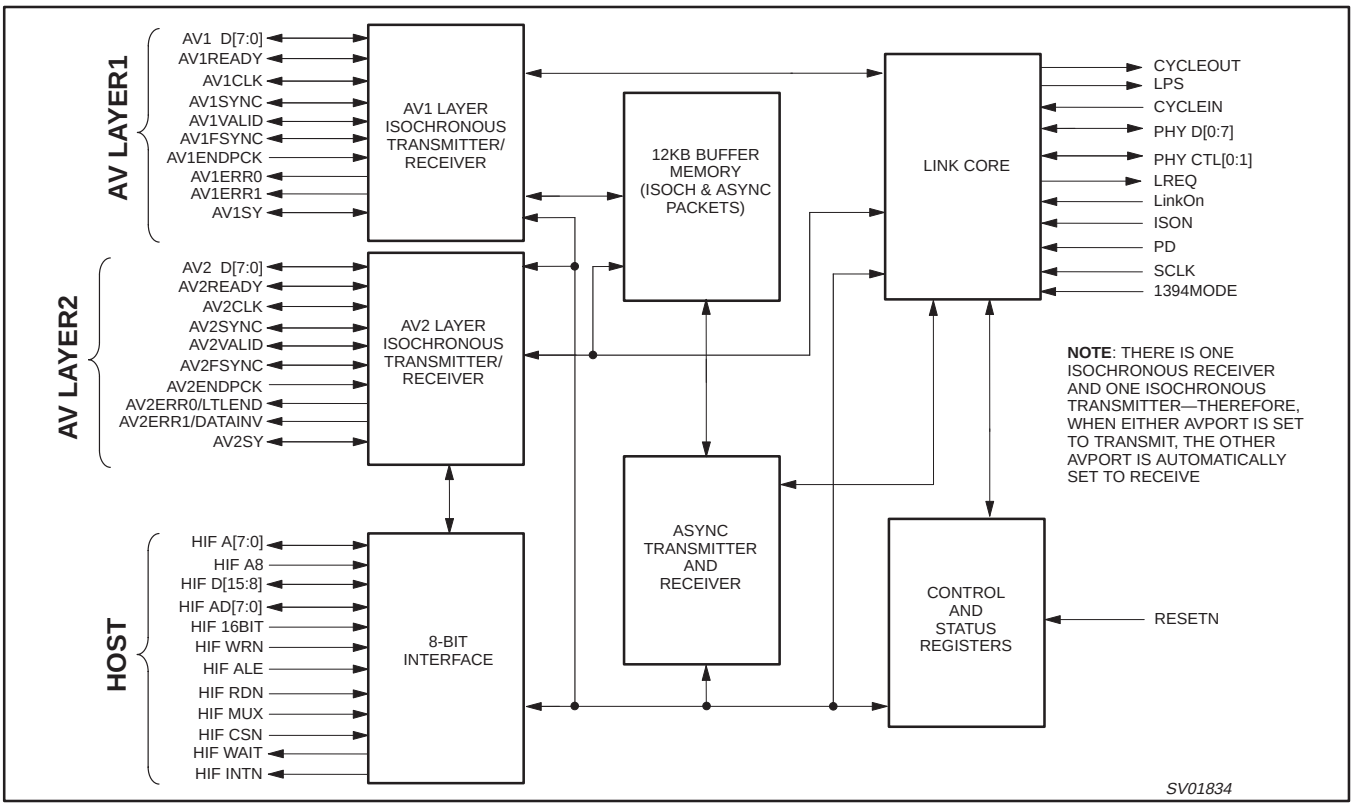
* Indicates pin equipped with internal bus hold circuit activated by the state of the ISON pin.

SV01832

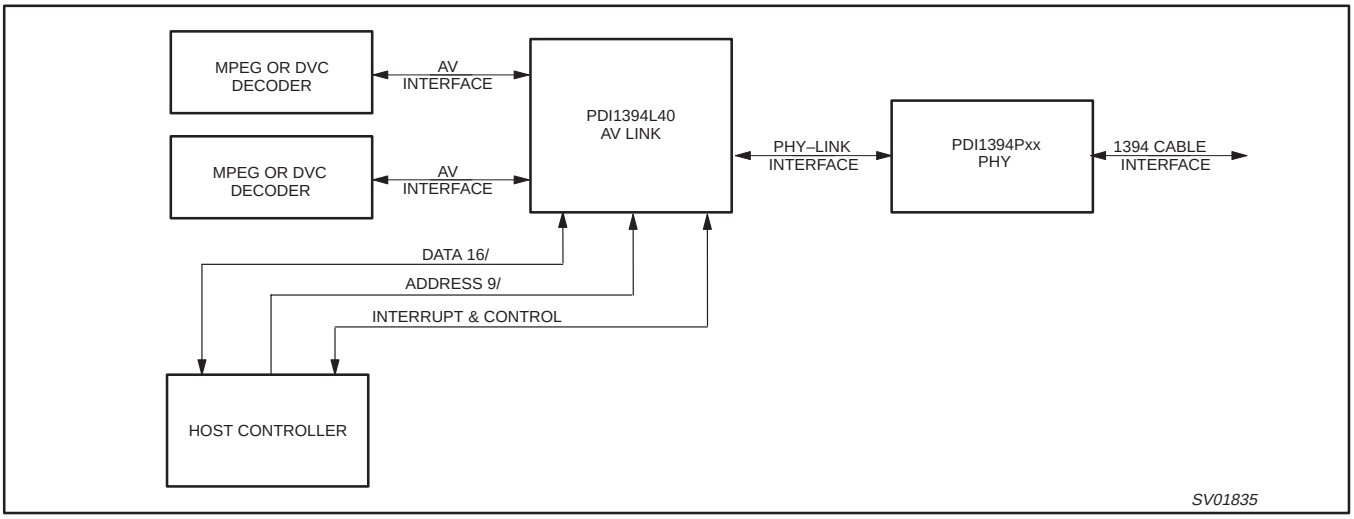
6.0 FUNCTIONAL DIAGRAM



7.0 INTERNAL BLOCK DIAGRAM



8.0 APPLICATION DIAGRAM



9.0 PIN DESCRIPTION

9.1 Host Interface

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
13, 14, 15, 16, 19, 20, 21, 22	HIF AD[7:0]	I/O	Host Interface Data 7 (MSB) through 0. Byte wide data path to internal registers.
1, 2, 3, 4, 7, 8, 9, 10	HIF D[15:8]	I/O	Host Interface Data 15 (MSB) through 8. Only used in 16 bit access mode (HIF 16BIT = HIGH).
26, 27, 28, 29, 30, 31, 32, 33	HIF A[7:0]	I/O	Host Interface Address 0 through 8. Provides the host with a byte wide interface to internal registers. See description of Host Interface for addressing rules (Section 12.5).
25	HIF A8	I	Control bit used to indicate the first byte/word of a read function or the last byte/word of a write function so that the data quadlet is fetched or stored. See Section 12.5 for more information regarding the host interface.
36	HIF CSN	I	Chip Select (active LOW). Host bus control signal to enable access to the FIFO and control and status registers.
37	HIF WRN	I	Write enable. When asserted (LOW) in conjunction with HIF CSN, a write to the PDI1394L40 internal registers is requested. (NOTE: HIF WRN and HIF RDN : if these are both LOW in conjunction with HIF CSN, then a write cycle takes place. This can be used to connect CPUs that use R/W_N line rather than separate RD_N and WR_N lines. In that case, connect the R/W_N line to the HIF WRN and tie HIF RDN LOW.)
38	HIF INTN	O	Interrupt (active LOW). Indicates a interrupt internal to the PDI1394L40. Read the General Interrupt Register for more information. This pin is open drain and requires a 1KΩ pull-up resistor.
39	HIF ALE	I	Address latch enable. Used in multiplex mode only.
40	HIF RDN	I	Read enable. When asserted (LOW) in conjunction with HIF CSN, a read of the PDI1394L40 internal registers is requested.
41	HIF WAIT	O	Wait signal. Signals Host interface in WAIT condition when HI. See Section 12.5.
42	RESETN	I	Reset (active LOW). The asynchronous master reset to the PDI1394L40.
45	HIF 16BIT	I	Host interface mode pin. When LOW HIF operates in 8 bit mode. When HIGH HIF operates in 16 bit mode.
46	HIF MUX	I	Host interface mode pin. When LOW HIF operates in non-multiplex mode, when HIGH HIF operates in multiplex mode. When HIGH, the low-order eight address bits are multiplexed with data on HIF AD[7:0], otherwise they are non-multiplexed and supplied on A[7:0].

9.2 AV Interface 1

NOTE: This AV interface may be configured to transmit or receive according to the condition of “DIRAV1” bit in GLOBCSR register (0x018)—default is transmit.

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
96	AV1ERR0	O	CRC error. Indicates bus packet delivered on AV1 D[7:0] had a CRC error; the current AV packet is unreliable.
97	AV1ERR1	O	Sequence Error. Indicates at least one source packet was lost before the current AV1 D [7:0] data.
98	AV1ENDPCK	I	End of application packet indication from data source. Required only if input packet is not multiple of 4 bytes. It can be tied LOW for data packets that are 4*N in size.
99	AV1CLK	I/O	External application clock. Rising edge active. This pin can be programmed to be an output and the application clock. Depending on the configuration of AV Port 1 as transmitter or receiver, the output enable is located in the ITXPKCTL register (address 0x020) or IRXPKCTL register (address 0x040).
100	AV1FSYNC	I/O	Programmable frame sync, is set to input when AV interface 1 is a transmitter and to output when the interface is configured as a receiver. When the pin is an input, it is used to designate a frame of data for Digital Video (DV). The signal is time stamped and transmitted in the SYT field of ITXHQ2. When set to an output, the signal is derived from SYT field of IRXHQ2.
101	AV1 SY	I/O	SY Value. When port AV1 is configured as a transmitter, this pin is an input. When the AV port is configured to as a receiver, the pin is an output. See the description for bit 0 of the ITXCTL (0x034) and IRXCTL (0x054) registers.
102	AV1VALID	I/O	Indicates data on AV1 D [7:0] is valid.
103	AV1SYNC	I/O	Indicates that the data currently being clocked by the source under the condition of AV1VALID is the start of an application packet. If the AV interface is configured as a receiver, then it will assert AV1SYNC when an application packet becomes available and persist until the first data of the packet is clocked out. Thus, AV1VALID may last for more than one cycle, but for exactly one cycle in which AV1VALID is asserted.
117, 116, 115, 114, 111, 110, 109, 108	AV1 D[7:0]	I/O	Audio/Video Data 7 (MSB) through 1. Part of byte-wide interface to the AV layer 1.
118	AV1READY	I	When the AV port is configured as a receiver, this pin is an input. This is a flow control signal that allows the application to indicate whether it is able to accept data flowing across AV Interface 1. The AV interface responds to an inactive AV1READY by not asserting AV1VALID, and thereby withholding data from the application. The AV1READY signal is processed through one level of pipelining, which means that the AV Link will accept data on the cycle in which AV1READY is de-asserted and will not accept data on the cycle in which AV1READY is asserted.
		O	When the AV port is configured to transmit, this pin is an output. This is a flow control signal that allows the link chip to indicate whether it is able to accept data flowing across AV Interface 1. The source of data, an external entity, responds to an inactive AV1READY by not asserting AV1VALID, and thereby withholding data. The AV1READY signal should be processed by the sink through one level of pipelining, which means that the receiver must be able to accept data on the cycle in which AV1READY is de-asserted. The receiving interface does not have to accept data on the cycle in which AV1READY is asserted.

9.3 AV Interface 2

NOTE: This AV interface may be configured to transmit or receive according to the condition of “DIRAV1” bit in GLOBCSR register—default is receive.

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
121	AV2ERR0/ LTLEND	I/O	CRC error, indicates bus packet containing AV2 D [7:0] had a CRC error, the current AV packet is unreliable. This pin is also used to input the mode of LTLEND (Little Endian) bit after a chip reset. An appropriate pull-up or pull-down resistor (22 kΩ recommended) should be connected to place the pin in the desired state during reset. Please see details related to use of the LTLEND bit in the “Host Interface” section (of the datasheet (Section 12.5).
122	AV2ERR1/ DATINV	I/O	Sequence Error. Indicates at least one source packet was lost before the current AV2 D [7:0] data. This pin is also used to input the mode of DATINV (Data Invariant) bit after a chip reset. An appropriate pull-up or pull-down resistor (22 kΩ recommended) should be connected to place the pin in the desired state during reset. Please see details related to use of the DATINV bit in the “Host Interface” section (of the datasheet (Section 12.5).
123	AV2ENDPCK	I	End of application packet indication from data source. Required only if input packet is not multiple of 4 bytes. It can be tied LOW for data packets that are 4*N in size.
124	AV2CLK	I/O	External application clock. Rising edge active. This pin can be programmed to be an output and the application clock. Depending on the configuration of AV Port 2 as transmitter or receiver, the output enable is located in the ITXPKCTL register (address 0x020) or IRXPKCTL register (address 0x040).
125	AV2FSYNC	I/O	Programmable frame sync, is set to input when AV interface 2 is a transmitter, and to output when the interface is configures as a receiver. When the pin is an input, it is used to designate a frame of data for Digital Video (DV). The signal is time stamped and transmitted in the SYT field of ITXHQ2. When set to an output, the signal is derived from SYT field of IRXHQ2.
126	AV2 SY	I/O	SY Value: When port AV2 is configured as a transmitter, this pin is an input. When the AV port is configured to as a receiver, the pin is an output. See the description for bit 0 of the ITXCTL (0x034) and IRXCTL (0x054) registers.
127	AV2VALID	I/O	Indicates data on AV2 D [7:0] is valid.
128	AV2SYNC	I/O	Indicates that the data currently being clocked by the source under the condition of AV2VALID is the start of an application packet. If the AV interface is configured as a receiver, then it will assert AV2SYNC when an application packet becomes available and persist until the first data of the packet is clocked out. Thus, AV2VALID may last for more than one cycle, but for exactly one cycle in which AV2VALID is asserted.
142, 141, 140, 139, 136, 135, 134, 133	AV2 D[7:0]	I/O	Audio/Video Data 7 (MSB) through 0. Part of byte-wide interface to the AV layer 2.
143	AV2READY	I	When the AV port is configured as a receiver, this pin is an input. This is a flow control signal that allows the application to indicate whether it is able to accept data flowing across AV Interface 2. The AV interface responds to an inactive AV2READY by not asserting AV2VALID, and thereby withholding data from the application. The AV2READY signal is processed through one level of pipelining, which means that the AV Link will accept data on the cycle in which AV2READY is de-asserted and will not accept data on the cycle in which AV2READY is asserted.
		O	When the AV port is configured to transmit, this pin is an output. This is a flow control signal that allows the link chip to indicate whether it is able to accept data flowing across AV Interface 2. The source of data, and external entity, responds to an inactive AV2READY by not asserting AV2VALID, and thereby withholding data. The AV2READY signal should be processed by the sink through one level of pipelining, which means that the receiver must be able to accept data on the cycle in which AV2READY is de-asserted. The receiving interface does not have to accept data on the cycle in which AV2READY is asserted.

9.4 Phy Interface

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
82, 81, 80, 79, 76, 75, 74, 73	PHY D[0:7]	I/O	Data 0 (MSB) through 7 (NOTE: To preserve compatibility to the specified Link-Phy interface of the IEEE 1394–1995 standard, Annex J, bit 0 is the most significant bit). Data is expected on AV D[0:1] for 100Mb/s, AV D[0:3] for 200Mb/s, and AV D[0:7] for 400Mb/s. See IEEE 1394–1995 standard, Annex J for more information.
86, 85	PHY CTL[0:1]	I/O	Control Lines between Link and Phy. See 1394 Specification for more information.
47	1394 MODE	I	1394–1995 Annex J PHY (HIGH), or 1394a PHY (LOW)
87	LREQ	O	Link Request. Bus request to access the PHY. See IEEE 1394–1995 standard, Annex J for more information. (Used to request arbitration or read/write PHY registers).
88	SCLK	I	System clock. 49.152MHz input from the PHY (the PHY-LINK interface operates at this frequency).
91	LPS	O	Link power status. Outputs a frequency (typically 1.4 MHz) with 25% duty cycle which tells the PHY chip that the L40 is active.
92	LINKON	I	L40 generates a host interrupt when this pin receives a link on signal from the PHY. Interrupt is a request from another node for the L40 to be powered up (see PD pin).
93	ISON	I	Isolation mode. This pin is asserted (LOW) when an Annex J type isolation barrier is used. See IEEE 1394–1995 Annex J. for more information. When tied HIGH, this pin enables internal bushold circuitry on the affected PHY interface pins (see below). Active bushold circuits allow either the direct connection to PHY pins or the use of the single capacitor isolation mode.

9.5 Other Pins

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
5, 11, 17, 23, 34, 43, 53, 60, 69, 77, 83, 89, 94, 106, 112, 119, 131, 137	GND		Ground reference
6, 12, 18, 24, 35, 44, 54, 61, 70, 78, 84, 90, 95, 107, 113, 120, 132, 138	V_{DD}		3.3 V $\pm$ 0.3 V power supply
48	$PD^{1,2,3,4}$	I	Power Down. When asserted (high), the AV Link goes into a low power mode and de-asserts the LPS pin. When in this state, reads and writes to the registers are not allowed. The AV Link will resume operation when PD is de-asserted (low), all register settings and configurations are restored to their pre power down values.
49, 50, 51, 52, 58, 59, 65, 66, 67, 68, 71, 72 104, 105, 129, 130, 144	RESERVED	NA	These pins are reserved for factory testing. For normal operation they should be connected to ground.
55	CLK50	O	Auxiliary clock, value is SCLK (usually 49.152 MHz)
56	CYCLEIN	I	Provides the capability to supply an external cycle timer signal for the beginning of 1394 bus cycles.
57	CYCLEOUT	O	Reproduces the 8kHz cycle clock of the cycle master.
62, 63, 64	TESTPIN		Test pins. These signals must be connected to ground.

NOTES:
Before asserting the RPL bit, SWPD or setting the PD pin high, the user should assure that the link chip is in the following state of operation:
1. The isochronous transmit FIFO is not receiving data for transmission
2. The isochronous transmitter is disabled
3. No asynchronous packets are being generated for transmission
4. Both the ASYNC request and response queues are empty

10.0 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	Input voltage		0	5	V
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current			–4	mA
dT/dV	Input transition rise or fall time		0	20	ns/V
T_{amb}	Operating ambient temperature range		0	+70	°C
SCLK	System clock		49.147	49.157	MHz
AVCLK	AV interface clock		0	24	MHz
t_r	Input rise time			10	ns
t_f	input fall time			10	ns

11.0 ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current		–	–50	mA
V_I	DC input voltage		–0.5	+5.5	V
I_{OK}	DC output diode current		–	±50	mA
V_O	DC output voltage		–0.5	V_{DD} +0.5	V
I_O	DC output source or sink current		–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		–	±150	mA
T_{stg}	Storage temperature range		–60	150	°C
T_{amb}	Operating ambient temperature		0	70	°C
P_{tot}	Power dissipation per package			0.6	W

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

12.0 FUNCTIONAL DESCRIPTION

12.1 Overview

The PDI1394L40 is an IEEE1394–1995 and IEEE1394.a compliant link layer controller. It provides a direct interface between a 1394 bus and various MPEG–2 and DVC codecs. The AV Link maps and unmaps AV data streams and similar data onto 1394 isochronous packets. Data can be ciphered or deciphered according to the '5C' standard method of content protection. The AV Link also provides an 8 bit or 16 bit wide host interface for an attached microcontroller. Through the host interface port, the host controller can configure the AV layer for transmission or reception of AV datastreams. The host interface port also allows the host controller to transmit and receive 1394 asynchronous data packets.

12.2 AV interface and AV layer

The AV interface and AV layer format "application packets" according to the IEC 61883 specification for isochronous transport over the 1394 network. The AV transmitter and receiver within the AV layer perform all the functions required to pack and unpack AV packet data for transfer over a 1394 network. Once the AV layer is properly configured for operation, no further host controller service should be required. The operation of the AV layer is full-duplex, i.e., the AV layer can receive and transmit AV packets on the same bus cycle.

12.2.1 IEC 61883 International Standard

The PDI1394L40 is specifically designed to support the IEC61883 International Standard of Digital Interface for Consumer Electronic Audio/Video Equipment. The IEC specification defines a scheme for mapping various types of AV datastreams onto 1394 isochronous data packets. The standard also defines a software protocol for managing isochronous connections in a 1394 bus called Connection Management Protocol (CMP). It also provides a framework for transfer of functional commands, called Function Control Protocol (FCP).

12.2.2 CIP Headers

A feature of the IEC61883 International Standard is the definition of Common Isochronous Packet (CIP) headers. These CIP headers contain information about the source and type of datastream mapped onto the isochronous packets.

The AV Layer supports the use of CIP headers. CIP headers are added to transmitted isochronous data packets at the AV data source. When receiving isochronous data packets, the AV layer automatically analyzes their CIP headers. The analysis of the CIP headers determines the method the AV layer uses to unpack the AV data from the isochronous data packets.

The information contained in the CIP headers is accessible via registers in the host interface.

(See *IEC61883 International Standard of Digital Interface for Consumer Electronic Audio/Video Equipment* for more details on CIP headers).

12.2.3 The AV Interface

The AV link's 8-bit parallel interface is synchronous with AVxCLK, and was designed to interface with various MPEG-2 and DVC codecs. The AV interface port buffer, if so programmed, can time stamp incoming AV packets. The AV packet data is stored in the embedded memory buffer, along with its time stamp information. After the AV packet has been written into the AV layer, the AV layer creates an isochronous bus packet with the appropriate CIP header. The bus packet along with the CIP header is transferred over the appropriate isochronous channel/packet. The size and configuration of isochronous data packet payload transmitted is determined by the AV layer's configuration registers accessible through the host interface.

The AV interface port waits for the assertion for AVxVALID and AVxSYNC. AVxSYNC is aligned with the rising edge of AVxCLK and the first byte of data on AVxDATA[7:0]. The duration of AVxSYNC is one AVxCLK cycle. AVxSYNC signals the AV layer that the transfer of an AV packet has begun. At the time the AVxSYNC is asserted, the AV layer creates a new time stamp in the buffer memory. (This only happens if so configured. The DVC format does not require these time stamps). The time stamp is then transmitted as part of the source packet header. This allows the AV receiver to provide the AV packet for output at the appropriate time. Only one AVSYNC pulse is allowed per application packet; if additional sync pulses are presented before the full packet is inputted, a new packet will be started and the previously inputted packet data will be discarded (and not transmitted) in conjunction with the input error interrupt bit (INPERR, bit 3 of register 0x02C) being set to flag the error.

An additional synchronization mechanism is defined by the IEC 61883 specification, called frame sync. The frame synchronization signal AVxFSYNC is time stamped and placed in the SYT field of the CIP header. The default delay value for the frame sync is 3 bus cycle times (duration of 125 µs each) in the future, and is transmitted on the very next isochronous cycle regardless of available data. The PDI1394L40 allows this value to be programmable from 2 to 4 cycle times (see Section 13.2.1). Additionally, for some audio applications, the SYT value can be programmed to be appended only to isochronous cycles that have application data attached to them. This mode is enabled via the AUDIO bit (again, see Section 13.2.1). When the AUDIO mode is enabled, two additional cycle delays are automatically added to the SYT_DELAY value (bits 6 and 5 of the ITXPKCLT register). On the receiver side, when the SYT stamp matches the cycle timer register, a pulse is generated on the AVxFSYNC output. The timing for AVxFSYNC is independent of AVxCLK. The maximum repetition rate of application-presented AVFSYNC pulses is limited to 8,000 pulses per second (the bus cycle rate). In the rare instance of SYT queue overflow with possible loss of up to 7 AVFSYNC pulses, the "SYTOVF" interrupt (bit 14 in register 0x04C) will occur. If an SYTOVF interrupt occurs, the contents of the SYT queue is automatically flushed and normal operation automatically resumes.

Some applications would like to create their own transmit timestamps independent of the AV Layer. On receive, these applications would like to process the embedded time stamps instead of allowing the AV Layer to process these time stamps. This can be accommodated via the ENXTMSTMP bit in the ITXPKCTL register for transmit and DIS_TSC bit in the IRXPKCTL register for receive. In conjunction with this mode, additional means of flow control are enabled via the AVxREADY signal.

Port Dir	AVxREADY	Description
Transmit	Out	The L40 is prepared to receive a byte. The attached device will not assert AVVALID for any cycle in which AVxRDY is false.
Receive	In	The attached device is prepared to receive a byte. The L40 will not assert AVxVALID for any cycle in which AVxREADY is false.

When the AV port is configured as a receiver, the AVxSYNC signal will be asserted as soon as the PDI1394L40 AVx port has an application packet available for delivery (independent of AVxREADY) and will remain asserted until the first byte of the application packet is clocked from the AV port.

12.2.4 Audio Support

The AV transmitter has some additional features to support some types of audio transport. These are enabled by setting bit 30 of ITXPKCTL (0x020) to logic 1. At the rising edge of AVxFSYNC, a SYT time stamp will be generated and written into the SYT queue of the isochronous transmitter. This stamp will point to a time in the future dictated by the following formula:

SYT[15:12] = CYCTM[15:12] + programmed SYT_DELAY value + 2
SYT[11:0] = CYCTM[11:0]

The additional delay of two cycles is specific to this AUDIO mode. The oldest SYT time stamp in the SYT queue will be sent first, but only when accompanied by a data payload. Any pending SYT time stamp will be held until the next non-empty bus packet is sent. At the moment of transmission, the SYT time stamp should at least point one cycle in the future. If it points to a time that is less than one cycle in the future, it will be discarded.

The SYT queue in the isochronous transmitter can store 4 entries, the SYT queue in the isochronous receiver can store six entries. This supports the case where an 8 kHz signal is applied to AVxFSYNC, and AUDIO = 1, and SYT_Delay = 2. Assuming there is data on every cycle, the receiver will receive an SYT time stamp each cycle with the first SYT time stamp pointing just less than six cycles in the future. When the SYT queue in the isochronous receiver is full, then the most recently received SYT time stamp is overwritten with the next arriving SYT time stamp. If the queue should become full or contain a corrupted time stamp, the queue will automatically clear and indicate so by setting the “SYTOVF” interrupt.

12.2.5 SY – Sync Support

This feature supports the 1394 digital camera specification. The state of this pin will be reflected in the SY bit (ITXCTL register 0x034) and will be transmitted along with the isochronous data block that was entered with it. The intended use of this pin is to signal the start of a new frame of video in the isochronous header section of the data payload. Similarly, the isochronous receiver will assert the AVxSY pin simultaneously with the first byte of the isochronous bus packet in which the SY value was received.

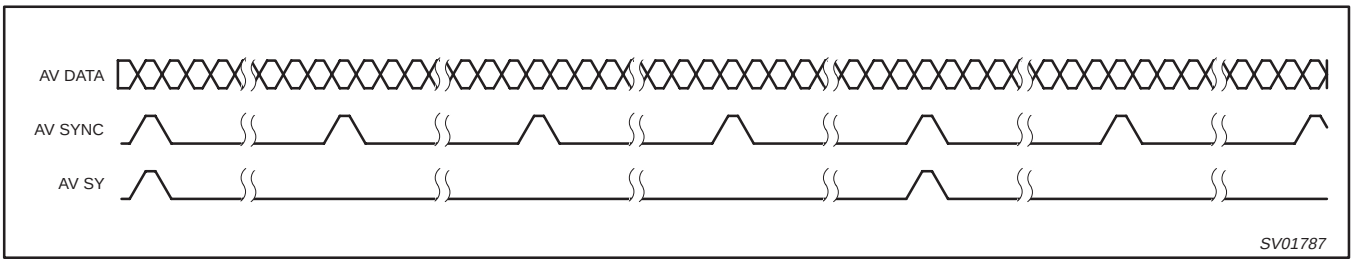


Figure 1. Behavior of SY signal at AV port of receiver

12.2.6 Programmable Buffer Memory

The PDI1394L40 maintains six distinct buffers that are highly configurable to optimize bandwidth capabilities. Buffers can be increased or decreased from the default value by accessing the indirect address range of 0x100 through 0x1FC (INDADDR, 0x0F8). If the AV Layer is configured to transmit or receive DVB compliant MPEG-2 type data, the default Isochronous (AV) buffer sizes are recommended. FIFO sizes cannot be changed dynamically; after a FIFO size change, transmitters and receivers must be reset.

Buffers can be programmed with 64 quadlet (256 Byte) granularity. Minimum buffer size is 64 quadlets, maximum buffer size is limited to 11 kB. The sum of all buffers cannot exceed 12K Bytes, or 3K Quadlets.

DEFAULT BUFFER SIZE

BUFFER MEMORY	SIZE (Quadlets)
Asynchronous Receive Response FIFO	256
Asynchronous Receive Request FIFO	256
Asynchronous Transmit Response FIFO	256
Asynchronous Transmit Request FIFO	256
Isochronous (AV) Transmit Buffer	1024
Isochronous (AV) Receive Buffer	1024

12.3 Bushold and Link/PHY single capacitor galvanic isolation

12.3.1 Bushold

The PDI1394L40 uses an internal bushold circuit on each of the indicated pins to keep these CMOS inputs from “floating” while being driven by a 3-Stated device or input coupling capacitor. Unterminated high impedance inputs react to ambient electrical noise which cause internal oscillation and excess power supply current draw.

The following pins have bushold circuitry enabled when the ISON pin is in the logic “1” state:

Name	Function
PHY CTL0	PHY control line 0
PHY CTL1	PHY control line 1
PHY D0	PHY data bus bit 0
PHY D1	PHY data bus bit 1
PHY D2	PHY data bus bit 2
PHY D3	PHY data bus bit 3
PHY D4	PHY data bus bit 4
PHY D5	PHY data bus bit 5
PHY D6	PHY data bus bit 6
PHY D7	PHY data bus bit 7
SYSCLK	System clock input to the link

Philips bushold circuitry is designed to provide a high resistance pull-up or pull-down on the input pin. This high resistance is easily overcome by the driving device when its state is switched. Figure 2 shows a typical bushold circuit applied to a CMOS input stage. Two weak MOS transistors are connected to the input. An inverter is also connected to the input pin and supplies gate drive to both transistors. When the input is LOW, the inverter output drives the lower MOS transistor and turns it on. This re-enforces the LOW on the input pin. If the logic device which normally drives the input pin were to be 3-Stated, the input pin would remain “pulled-down” by the weak MOS transistor. If the driving logic device drives the input pin HIGH, the inverter will turn the upper MOS transistor on, re-enforcing the HIGH on the input pin. If the driving logic device is then 3-Stated, the upper MOS transistor will weakly hold the input pin HIGH.

The PHY’s outputs can be 3-Stated and single capacitor isolation can be used with the Link; both situations will allow the Link inputs to float. With bushold circuitry enabled, these pins are provided with dc paths to ground, and power by means of the bushold transistors; this arrangement keeps the inputs in known logical states.

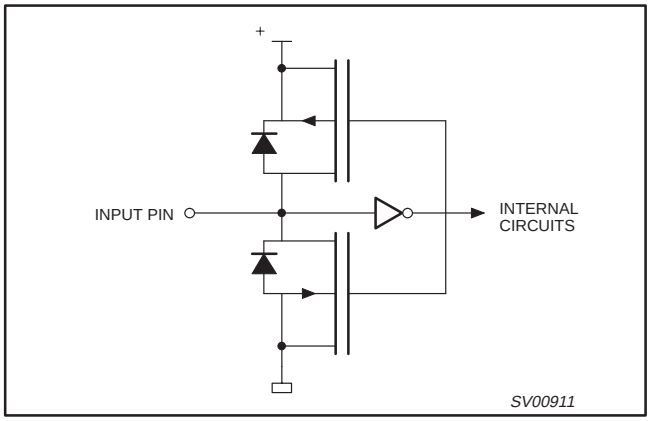


Figure 2. Bushold circuit

12.3.2 Single capacitor isolation

The circuit example (Figure 3) shows the connections required to implement basic single capacitor Link/PHY isolation.

NOTE: The isolation enablement pins on both devices are in their “1” states, activating the bushold circuits on each part. The bushold circuits provide local dc ground references to each side of the isolating/coupling capacitors. Also note that ground isolation/signal-coupling must be provided in the form of a parallel combination of resistance and capacitance as indicated in the IEEE 1394 standard.

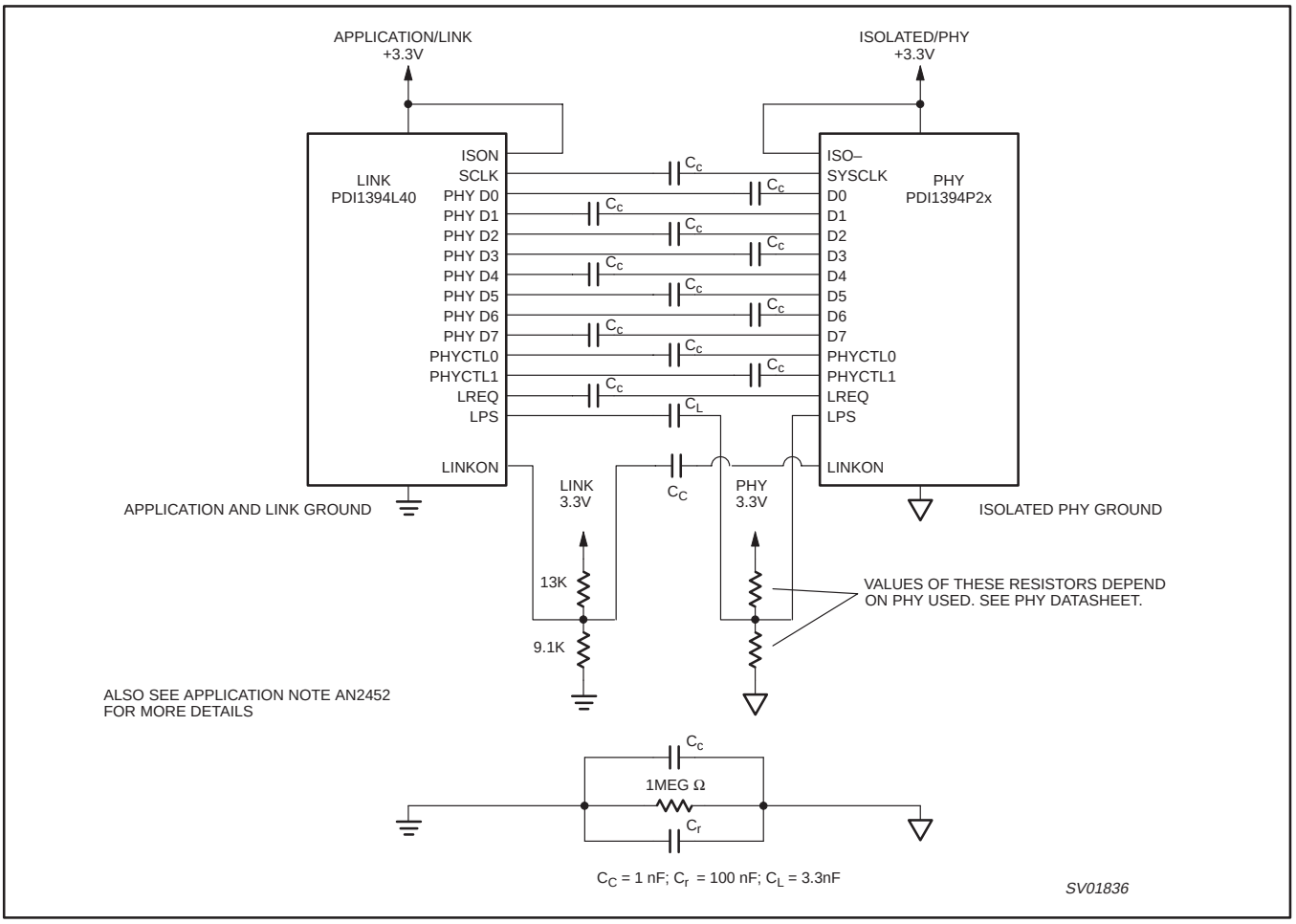


Figure 3. Single capacitor Link/PHY isolation

12.4 Power Management

The PDI1394L40 implements several features for power management as noted in IEEE 1394a.2000. These features include:

1. Reset of the Phy/Link interface by setting the RPL bit in the LNKCTL register.
2. Disable of the Phy/Link interface caused by either setting the SWPD bit in the RDI register –OR– asserting (high) the PD pin.
3. Initialization of the Phy/Link interface after it was disabled or reset.

The application can power up the Phy/Link interface by deasserting the PD pin –OR– clearing (low) the SWPD in the RDI register. This will cause the L40 to produce a pulsing signal on the LPS pin. When the L40 is in power down mode, reads and writes to the host interface will be restricted to those addressing only the RDI register (0x0B0). Please see Section 13.3.11 for further details.

There are 3 ways to power up the L40. (1) When the application wants the 1394 node to resume operation, it simply needs to de–assert the PD pin, or (2) clear the SWPD bit in the RDI register. The link can also be awakened by another bus node sending a link–on packet to the PHY of the application’s node. (3) The attached PHY will activate its LinkOn line and the L40 will see the signal and set the LOA bit of the RDI register. Assuming that the ELOA bit is in its enabled, ”1”, state, the L40 will generate an interrupt of the host processor. It will then be up to the host processor to decide whether to honor the link–on request of the other node. Then the host processor will de–assert the PD pin –OR– clear the SWPD bit in the RDI register. This activity will power up the L40 causing it to send the pulsing signal out on the LPS pin which notifies the PHYchip of link activity and allows the PHY to discontinue directing the link on signal to the L40. Subsequently, the host processor must acknowledge the LOA interrupt by writing a ”1” to the LOA bit position in the RDI register after the link on signal from the PHY has stopped.

12.5 The host interface

The host interface allows an 8 bit or 16 bit CPU to access all registers and the asynchronous packet queues. It is designed to be easy to use with a wide range of processors, including 8051, MIPS1900, ST20, PowerPC etc. The host interface can work with 8 bit or 16 bit wide data paths, and offers multiplexed or non-multiplexed access. There are 64 register addresses (for quadlet wide registers). To access bytes rather than quadlets the address space is 256 bytes, requiring 8 address lines.

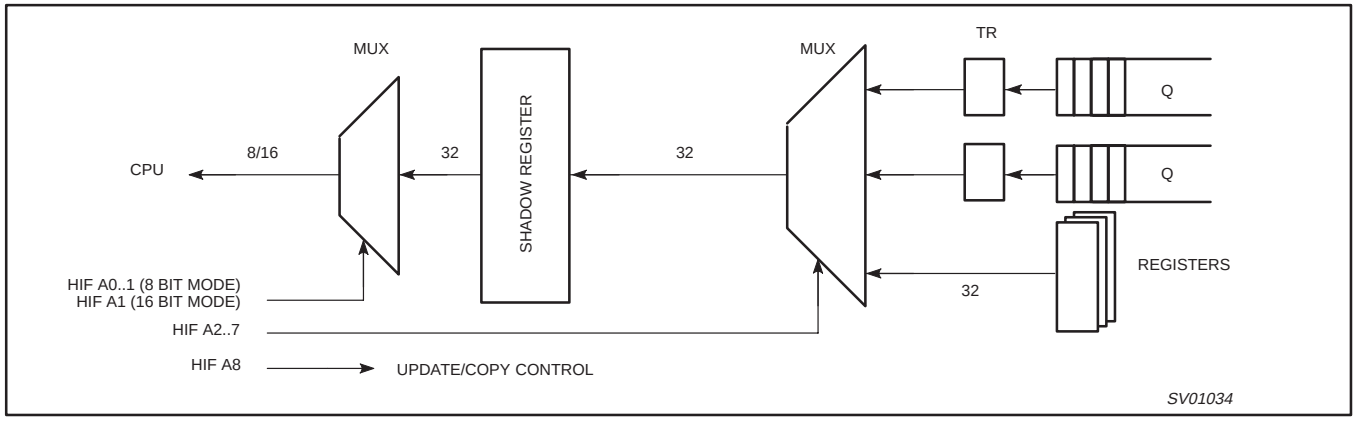
The use of an 8 bit or 16 bit interface introduces an inherent problem that must be solved: register fields can be more than 8 bits wide and be used (control) or changed (status) at every internal clock tick. If such a field is accessed through an 8 bit or 16 bit interface it requires more than one read or write cycle, and the value should not change in between to maintain consistency. To overcome this problem accesses to the chip's internal register space are always 32 bits, and the host interface must act as a converter between the internal 32 bit accesses and external 8 bit or 16 bit accesses. This is where the shadow register (0x0F4) is used.

12.5.1 Read accesses

To read an internal register the host interface can make a snapshot (copy) of that specific register which is then made available to the CPU 8 or 16 bits at a time. The register that holds the snapshot copy of the real register value inside the host interface is called the **shadow register**. During an 8-bit read cycle address lines HIF A0 and HIF A1 are used to select which of the 4 bytes currently stored in the **shadow register** is output onto the CPU data bus. This selection is done by combinatorial logic only, enabling external hardware to toggle these lines through values 0 to 3 while keeping the chip in a read access mode to get all 4 bytes out very fast (in a single extended read cycle), for example into an external quadlet register. During a 16 bit read cycle address line HIF A1 is used to select which pair of 4 bytes currently stored in the shadow register is output to the CPU bus. Again the selection is by combinatorial logic, enabling external hardware to toggle HIF A1 while keeping the chip in read access mode to get both words very quickly.

This solution requires a control line to direct the host interface to make a snapshot of an internal register when needed, as well as the internal address of the target register. The register address is connected to input address lines HIF A2..HIF A7, and the update control line to input address line HIF A8. To let the host interface take a new snapshot the target address must be presented on HIF A2..HIF A7 and HIF A8 must be raised while executing a read access. The new value will be stored in the **shadow register** and the selected byte (HIF A0, HIF A1, 8 bit mode) or word (HIF A1, 16 bit mode) appears on the output.

Not all registers can be accessed in Direct Address Space. Some of the registers are in an indirect address space, these registers control the FIFO size and content protection system. The correct internal register space has to be selected through the host interface, using directly addressable registers INDADDR (0x0F8) and INDDATA (0x0FC).



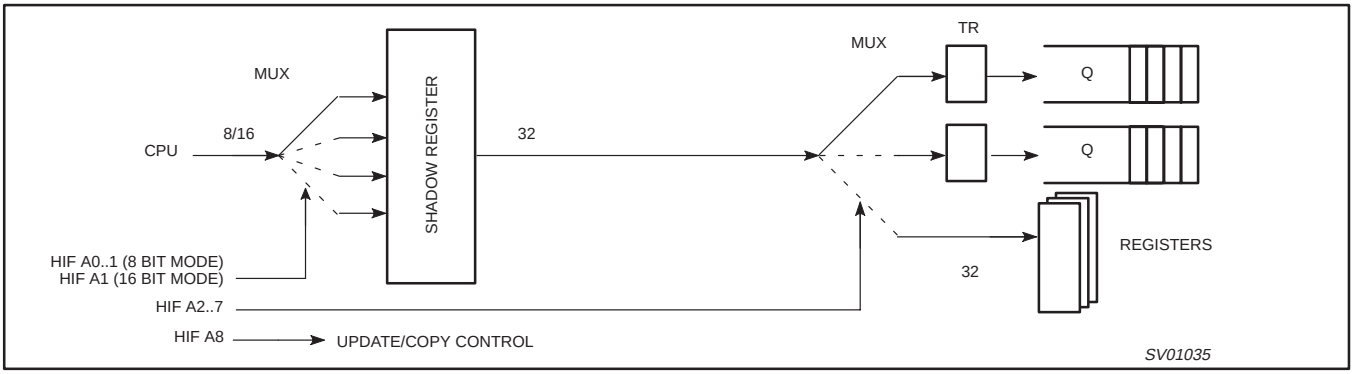
NOTES:

1. It is not required to read all 4 bytes of a register before reading another register. For example, in 8 bit mode, if only byte 2 of register 0x54 is required a read of byte address 0x100 + (0×54) + 2 = 0x156 is sufficient.
2. The update control line does not necessarily have to be connected to the CPU address line HIF A8. This input could also be controlled by other means, for example a combinatorial circuit that activates the update control line whenever a read access is done for byte 0. This makes the internal updating automatic for quadlet reading.
3. Reading the bytes of the shadow register can be done in any order and as often as needed.
4. It is possible to read/modify/write a register using the shadow register (0x0F4) without rewriting all 4 bytes. For example, to modify an enable bit in the fourth byte of the Asynchronous Interrupt Enable (0x0A4), a read of location 0x100+0x0A0+3=0x1A3, followed by a write of the modified byte to the same location 0x100+0x0A0+3=0x1A3 is sufficient. The other bytes remain unchanged.

12.5.2 Write accesses

To write to an internal register the host interface must collect the 4 byte values (8 bit mode) or 2 word values (16 bit mode) into a 32 bit value and then write the result to the target register in a single clock tick. This requires a register to hold the 32 bit value being compiled until it is ready to be written to the actual target register. This temporary register inside the host interface is called the **shadow register**. In 8 bit mode, address lines HIF A0 and HIF A1 are used to select which of the 4 bytes of the shadow register is to be written with the value on the CPU data bus. In 16 bit mode, HIF A1 is used to select which half of the shadow register is to be written with the value on the CPU data bus. Only one byte (8 bit mode) or one word (16 bit mode) can be written in a single write access cycle.

Not all registers can be accessed in Direct Address Space. Some of the registers are in an indirect address space, these registers control the FIFO size and content protection system. The correct internal register space has to be selected through the host interface, using directly addressable registers INDADDR (0x0F8) and INDDATA (0x0FC).



NOTES:

1. It is not required to write all 4 bytes, or both words of a register: those bytes that are either reserved (undefined) or don't care do not have to be written in which case they will be assigned the value that was left in the corresponding byte of the **shadow register** from a previous write access. For example, to acknowledge an interrupt for the isochronous receiver in 8 bit mode, a single byte write to location 0x100+(0x4C)+3 = 0x14F is sufficient. The value 256 represents setting HIF A8=1. The host interface cannot directly access the FIFOs, but instead reads from/writes into a transfer register (shown as TR in the Figures above). Data is moved between FIFO and TR by internal logic as soon as possible without CPU intervention.
2. The update control line does not necessarily have to be connected to the CPU address line HIF A8. This input could also be controlled by other means, for example a combinatorial circuit that activates the update control line whenever a write access is done for byte 3 or the upper 16 bits. This makes the internal updating automatic for quadlet writing.
3. Writing the bytes or words of the shadow register can be done in any order and as often as needed (new writes simply overwrite the old value).
4. It is now possible to read/modify/write a register using the shadow register (0x0F4) without rewriting all 4 bytes. For example, to modify an enable bit in the fourth byte of the Asynchronous Interrupt Enable (0x0A4), a read of location 0x100+0x0A0+3=0x1A3, followed by a write of the modified byte to the same location 0x100+0x0A0+3=0x1A3 is sufficient. The other bytes remain unchanged.

12.5.3 Accessing the RDI register (Power–down, Power–up)

Accessing the RDI register is a special situation, but software written to access all other link base registers can still be used. This register can be read and written with the link chip in power–down mode; this means that there is no system clock present within the link chip. The system clock is required to access all other link registers due to the fact that multiple clock cycles are required to fetch data to the shadow register or write data from the shadow register to the targeted internal register. Reading and writing to the RDI register is done through purely combinatoral logic, there is no access through the shadow register. The RDI register is accessed directly through the host interface using the same method of access required by other link base registers.

The RDI register contains control, status and interrupt bits. Operation of the status and interrupt bits in the RDI register differs slightly from these types of bits in other registers. Operation falls into four categories: (1) pure status bit, (2) interrupt/status bit, (3) control bit, (4) interrupt control bit.

LPSTAT is a pure status bit; this means that LPSTAT continually reflects the status of the LPS signal on the link–phy interface. If LPSTAT = 1, the LPS signal is active. If LPSTAT = 0, the LPS signal to the phy chip is inactive. It should be noted here that the LPSTAT bit should NOT be used as an indicator of link chip activity because the LPS signal may be inactive for short (25 uS) periods of time if the link chip is performing a phy–link interface reset function. SCI is also a pure status bit when it is not enabled as an interrupt. SCI will reflect the INVERSE status of the system clock at all times. When the system clock (SCLK) is active, SCI = 0. When the SCLK is inactive, SCI = 1. The SCI bit can also be used as an interrupt bit by setting ESCI = 1. In this mode of operation when the SCI = 1, an interrupt will be generated to indicate that the SCLK has become inactive. This interrupt is serviced in the same manner as all other link register interrupts... write a "1" back to the SCI bit position in order to acknowledge the interrupt.

PLI, LOA and SCA are interrupt/status bits. These bits may be enabled as interrupts (by setting the corresponding interrupt control bit EPLI, ELOA, or ESCA =1). These bits are ALSO status bits when the corresponding interrupt enabling bit is = 0. However, if any of these bits sets (=1) while in the status bit mode, it **must be written with a "1" to be reset**... similar operation to interrupt bit operation elsewhere in the link registers. Also, like other interrupt bits in the link registers, in order to acknowledge an interrupt of any of these bits, it is necessary to write a "1" back to the bit position to acknowledge the interrupt; this resets the bit to "0". [Please bear in mind that the functions represented by these bits

are continuous; so we recommend that before the interrupt is acknowledged, the corresponding enable bit should be set to “0”, else the interrupt will immediately happen again.]

SWPD is a control bit. There are two ways to affect a power–down of the link chip. Setting SWPD will stop the link chip from transmitting the LPS signal to the phy chip and thus cause the phy to withhold the SCLK, thus powering–down the link chip. Raising the link PD pin to the high level will also accomplish power–down in a similar manner. DO NOT USE BOTH METHODS to affect a power–down. The SWPD bit, being a control bit, will NOT reflect the state of the PD pin. If the SWPD bit is = 0 and the SCI bit is = 1, it’s a good bet that the PD pin is active if the phy chip is operating. In this case the PD pin MUST be reset low before the link will power–up.

EPLI, ELOA, ESCA, and ESCI are interrupt enable bits. Setting any of these bits = 1 will cause the corresponding interrupt bit to become an active interrupt when that bit sets. If these bits are set = 0, the corresponding PLI, LOA, SCA, and SCI bit is in the interrupt/status mode as described above.

(Also see the individual bit descriptions in the RDI register section of this data sheet... Section 13.3.1)

12.5.4 Big and little endianness, data invariance, and data bus width

The host interface offers programmable endianness, data invariance, and selectable 8 and 16 bit data widths. LTLEND (pin 121) and DATINV (pin 122) are multiplexed configuration pins that will be sampled on the trailing edge of RESET; the states of these pins are established by connecting each pin to the proper logic state, ground or V_{DD}, through a resistor, 22 kΩ is recommended. To verify the configuration, the shadow register (0x0F4) will be preset to a value of 0x0F0A0500 after a power reset. Table 1 describes the configurations.

Table 1. Configuration possible combinations

LTLEND (Little Endian)	DATINV (Data Invariant)	HIF 16BIT	Result
1	1	See Table 2	Byte/Word address is reversed
1	0	1	Bytes are swapped within the word
0	X	1	16-bit data bus, address as in PDI1394L21
0	X	0	8-bit data bus, address as in PDI1394L21

Table 2. Explanation of the mode LittleEnd = 1, DataInvariant = 1

HIF16 = 0		HIF16 = 1	
Outside Address (A1, A0)	Inside Address (A1, A0)	Outside Address (A1, A0)	Inside Address (A1, A0)
00	11	0X	1X
01	10	0X	1X
10	01	1X	0X
11	00	1X	0X

It is important to note that some operands in the indirect address space consist of more than one quadlet. For these operands, the lowest address always contains the most significant quadlet.

In Bit Endian mode and DATAINV = 0, the bytes in each quadlet are numbered 0..3 from left (most significant) to right (least significant) as shwon in Figure 4.

To access a register in 8 bit HIF mode, at address N the CPU should use addresses E:
E = N ; to access the upper 8 bits of the register.
E = N + 1 ; to access the upper middle 8 bits of the register.
E = N + 2 ; to access the lower middle 8 bits of the register.
E = N + 3 ; to access the lower 8 bits of the register.

To access a register in 16 bit HIF mode, at internal address N, the CPU should use addresses E:
E = N ;to access the upper 16 bits of the register
E = N + 2 ;to access the lower 16 bits of the register

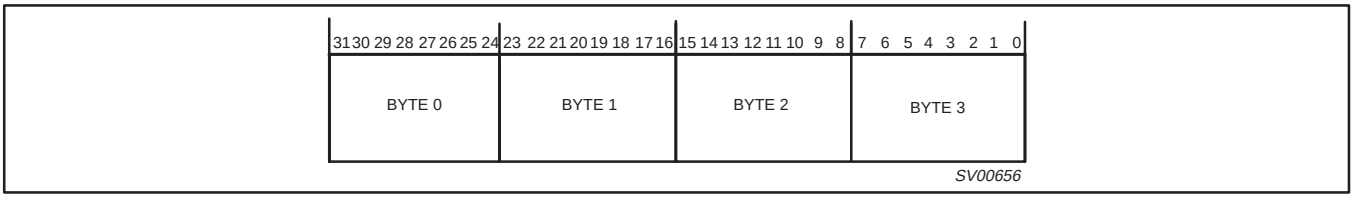


Figure 4. Byte order in quadlets as implemented in the host interface, HIF LTLEND = LOW

In Little Endian mode and DATAINV = 0, the bytes in each quadlet are numbered 3. .0 from the left (most significant) to right (least significant) as shown in Figure 5. To access a register in 8 bit HIF mode, at address N the CPU should use addresses E:

E = N + 3 ;to access the upper 8 bits of the register

E = N + 2 ;to access the upper middle 8 bits of the register

E = N + 1 ;to access the lower middle 8 bits of the register

E = N ;to access the lower 8 bits of the register

To access a register in 16 bit HIF mode, at internal address N, the CPU should used addresses E:

E = N ;to access the lower 16 bits of the register

E = N + 2 ;to access the upper 16 bits of the register

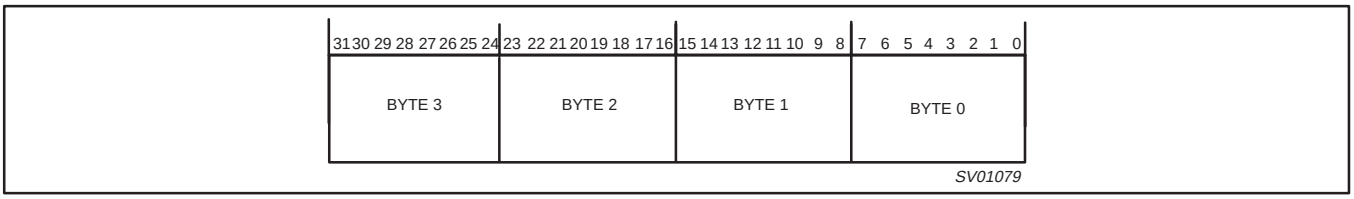


Figure 5. Byte order in quadlets as implemented in the host interface, HIF LTLEND = HIGH

12.5.5 Accessing the asynchronous packet queues

Although entire incoming packets are stored in the receiver buffer memory they are not randomly accessible. These buffers act like FIFOs and only the frontmost (oldest) data quadlet entry is accessible for reading. Therefore only one location (register address) is allocated to each of the two receiver queues. Reading this location returns the head entry of the queue, and at the same time removes it from the queue, making the next stored data quadlet accessible.

With the current host interface such a read is in fact a move operation of the data quadlet from the queue to the shadow register. Once the data is copied into the shadow register it is no longer available in the queue itself so the CPU should always read all 4 bytes, or both words, before attempting any other read access (be careful with interrupt handlers for the PDI1394L40!).

12.5.6 The CPU bus interface signals

The CPU interface is directly compatible with a wide range of microcontrollers, and supports both multiplexed and non-multiplex access. It uses separate HIF RDN, HIF WRN, HIF ALE, and HIF CSN chip select lines. There are 9 address inputs (HIF A0..HIF A8) and 8 or 16 data in/out lines HIF D[7:0] or HIF D [15:0]. The upper 8 bits of the data in/out lines are only used when the 8/16 bit mode pin (HIF16BIT) is held HIGH.

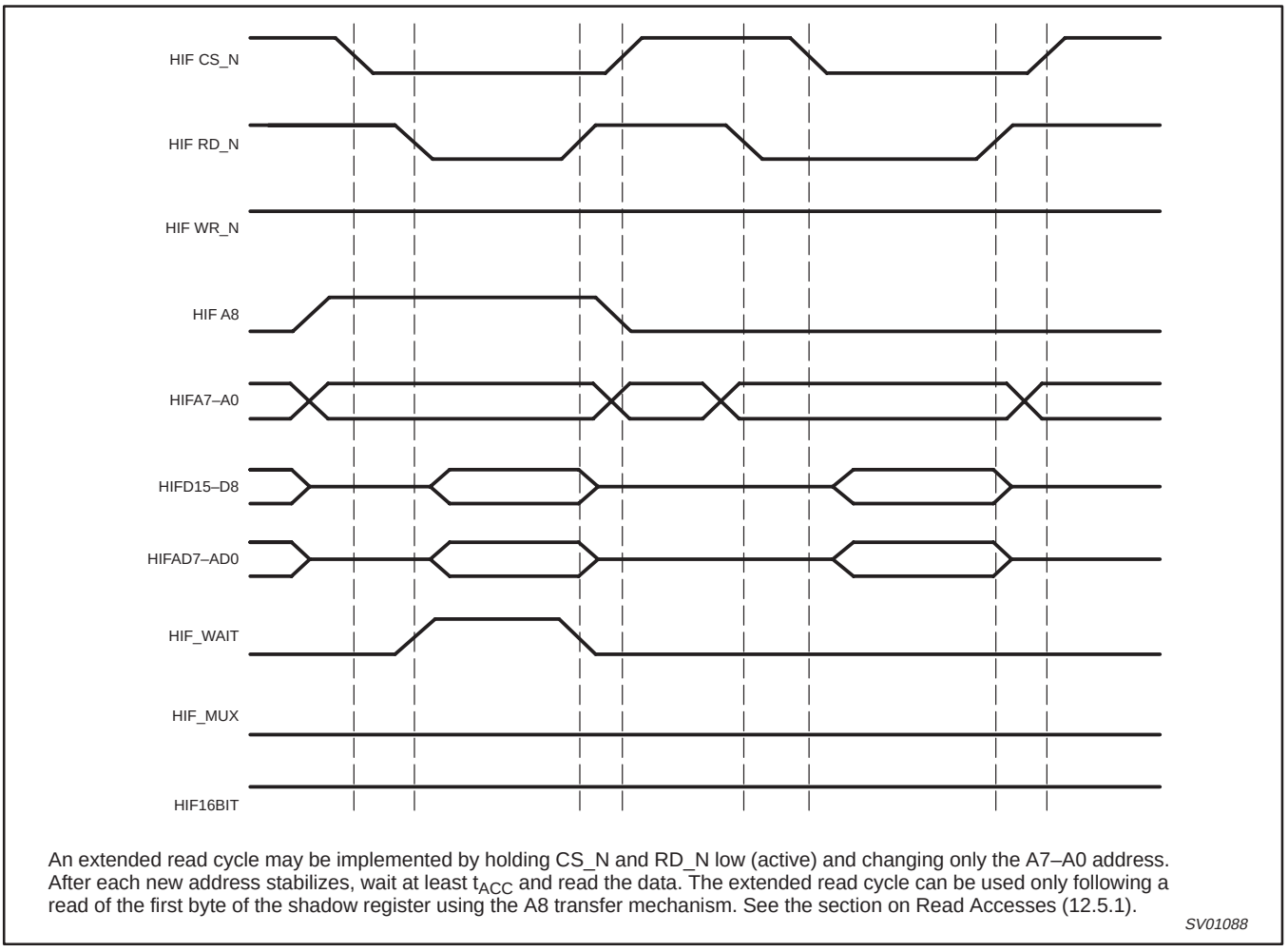
The CPU is not required to run a clock that is synchronous to the 1394 base clock. The control signals will be resampled by the host interface before being used internally.

In non-multiplex mode (HIF MUX = LOW), an access through the host interface starts when HIF CSN = 0 and either HIF WRN = 0 or HIF RDN = 0. Typically the chip select signal is derived from the upper address lines of the CPU (address decode stage), but it could also be connected to a port pin of the CPU to avoid the need for an external address decoder in very simple CPU systems. When both HIF CSN = 0 and HIF RDN = 0 the host interface will start a read access cycle, so the cycle is triggered at the falling edge of either HIF CSN or HIF RDN, whichever is later.

In multiplex mode (HIF MUX = HIGH), an access through the host interface starts when HIF CSN = 0 and either HIF WRN = 0 or HIF RD_N = 0. The address must now be presented on the HIF AD [7:0] lines, and will be latched on the falling edge of ALE. If HIF RDN = 0, data will be offered after the falling edge of ALE. If HIF WRN = 0, data has to be presented by the microcontroller.

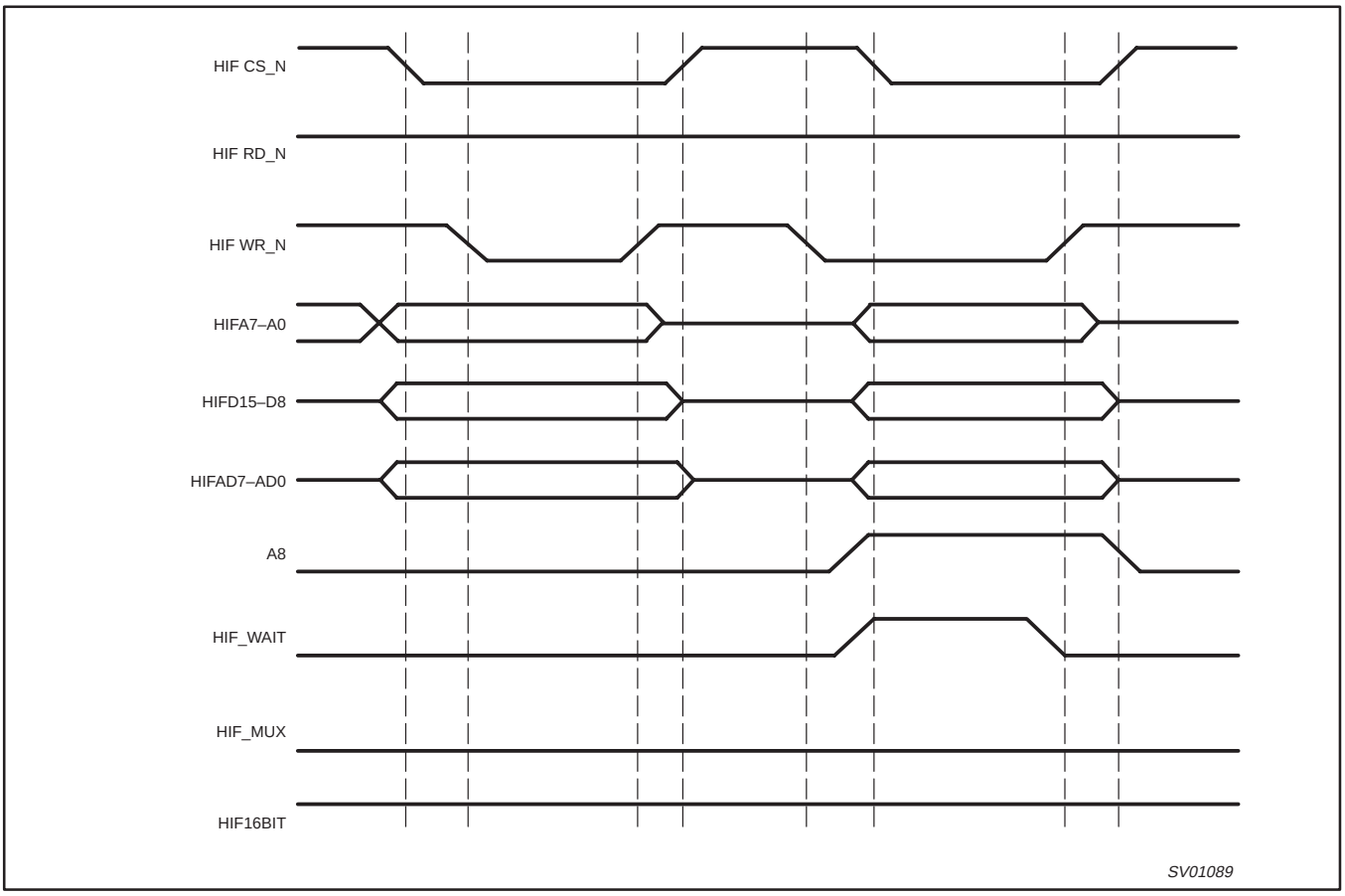
In both multiplexed and non-multiplexed mode, HIF WAIT can be used to signal to the controlling CPU that an extension of the current access cycle is needed. This allows the PDI1394L40 to work in the same address space as peripherals with a shorter access time. HIF WAIT will remain HIGH for the minimum duration of the access cycle. If HIF A[8] is HIGH, HIF WAIT will extend the access cycle to 120ns to allow for the shadow register transfer to take place. Subsequent access to the same register which does not required A[8] to be raised, can be executed much faster. By connecting HIF WAIT to the appropriate input on the controlling processor, the PDI1394L40 can be mapped in memory space with faster devices. The PDI1394L40 should not be mapped in memory space with devices that require access faster than 15 ns.

HIF A[7:0] can be used as a simple demultiplexer. In multiplex mode, the address on AD[7:0] will appear on A[7:0] immediately, and will remain there until the next rising edge of HIF ALE.



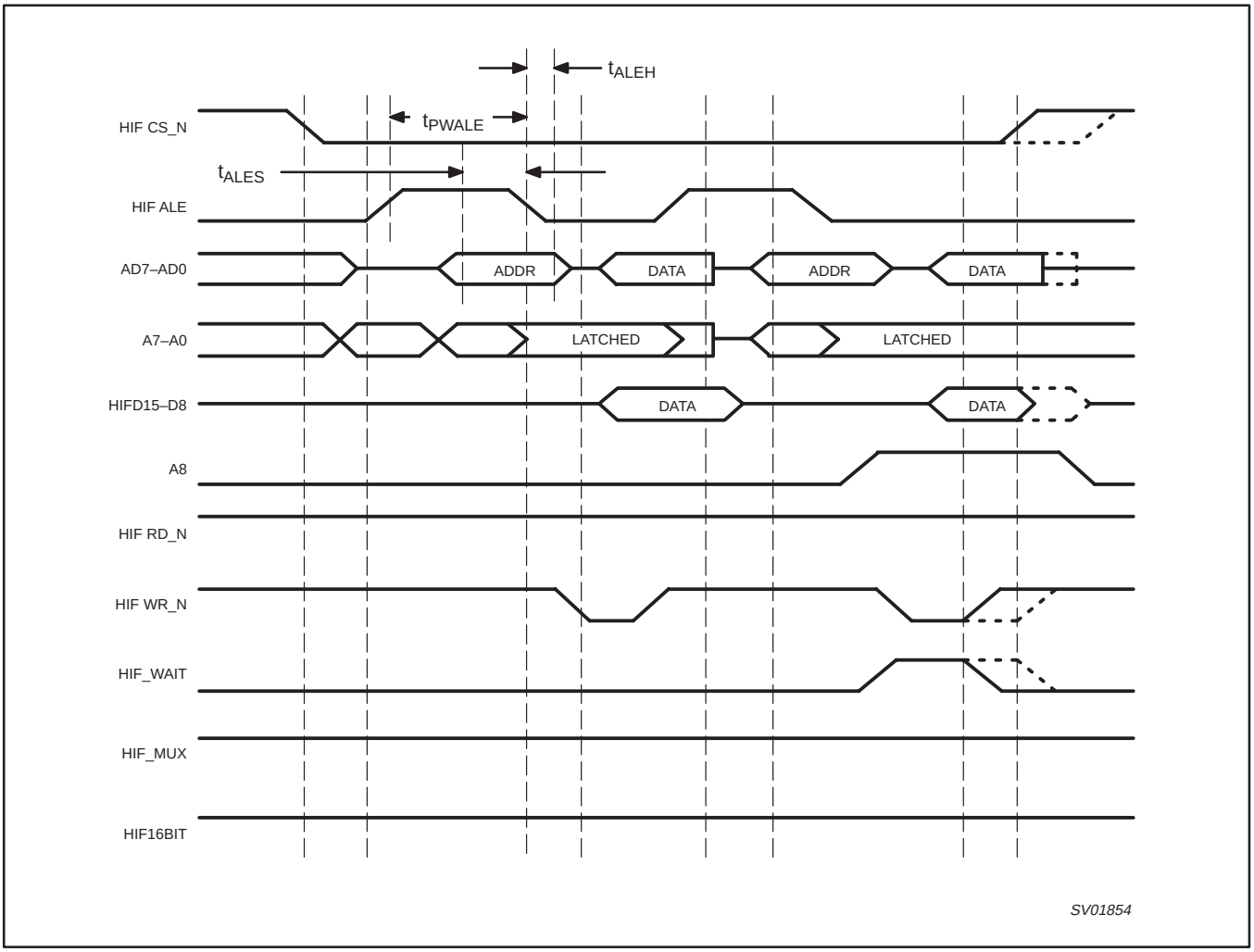
NOTE:
1. ALE line is held LOW.

Figure 6. 16 Bit Read Cycle Non-multiplexed



NOTE:
1. ALE line is held LOW.

Figure 7. 16 Bit Write Cycle Non-multiplexed



NOTE:
1. Second write cycle elongated by WAIT signal.

Figure 8. 16 Bit Write Cycle Multiplexed

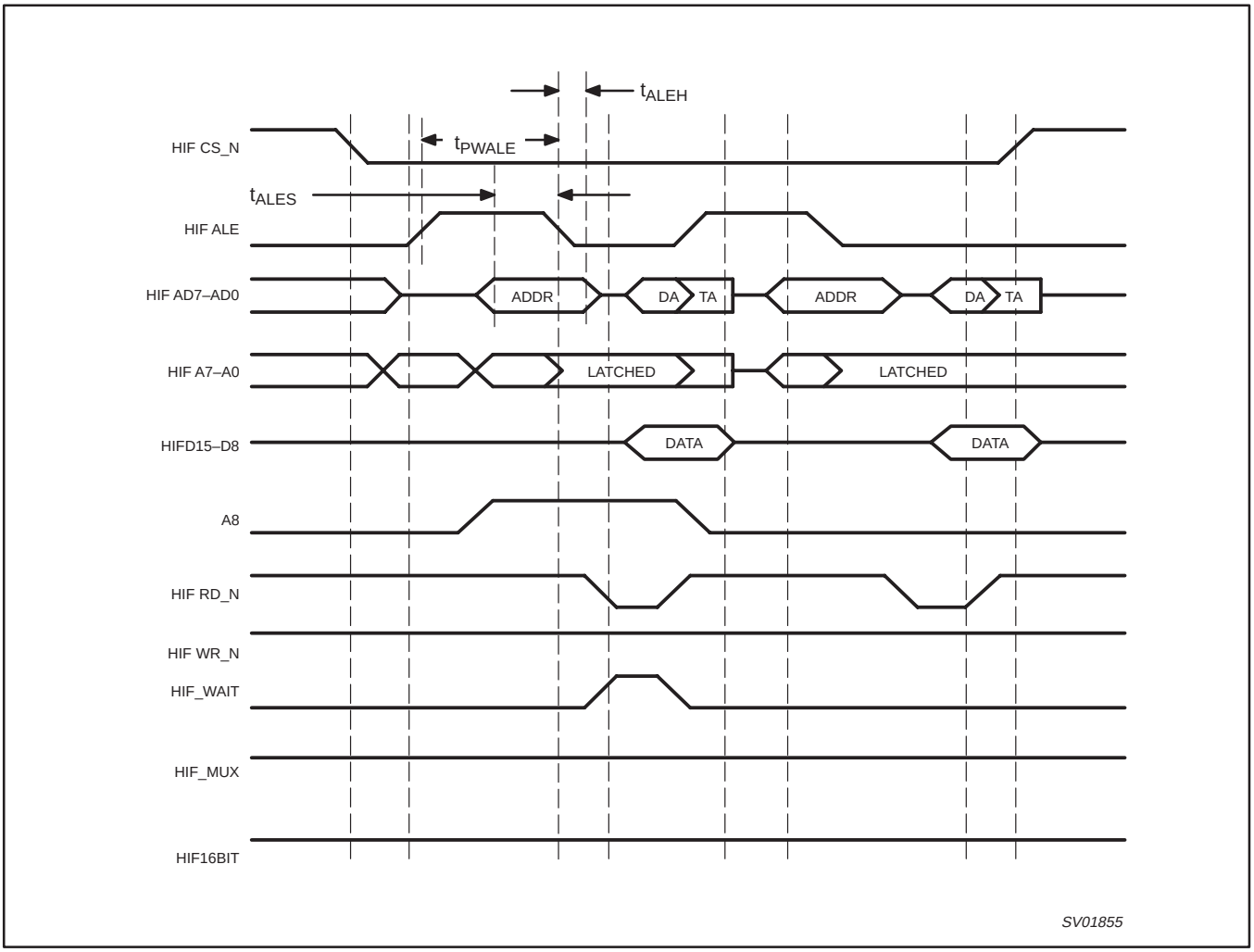


Figure 9. 16 Bit Read Cycle Multiplexed

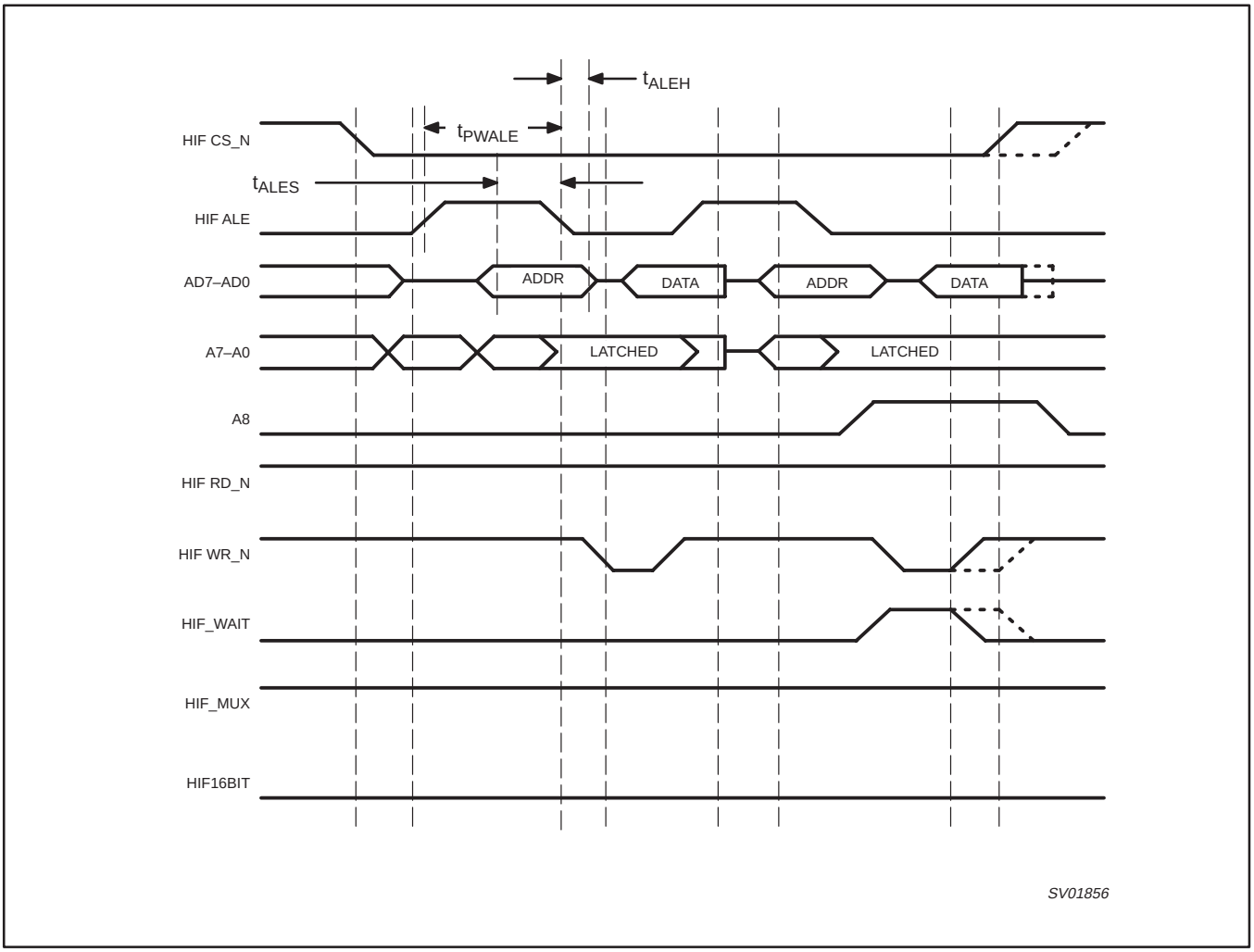


Figure 10. 8 Bit Write Cycle Multiplexed

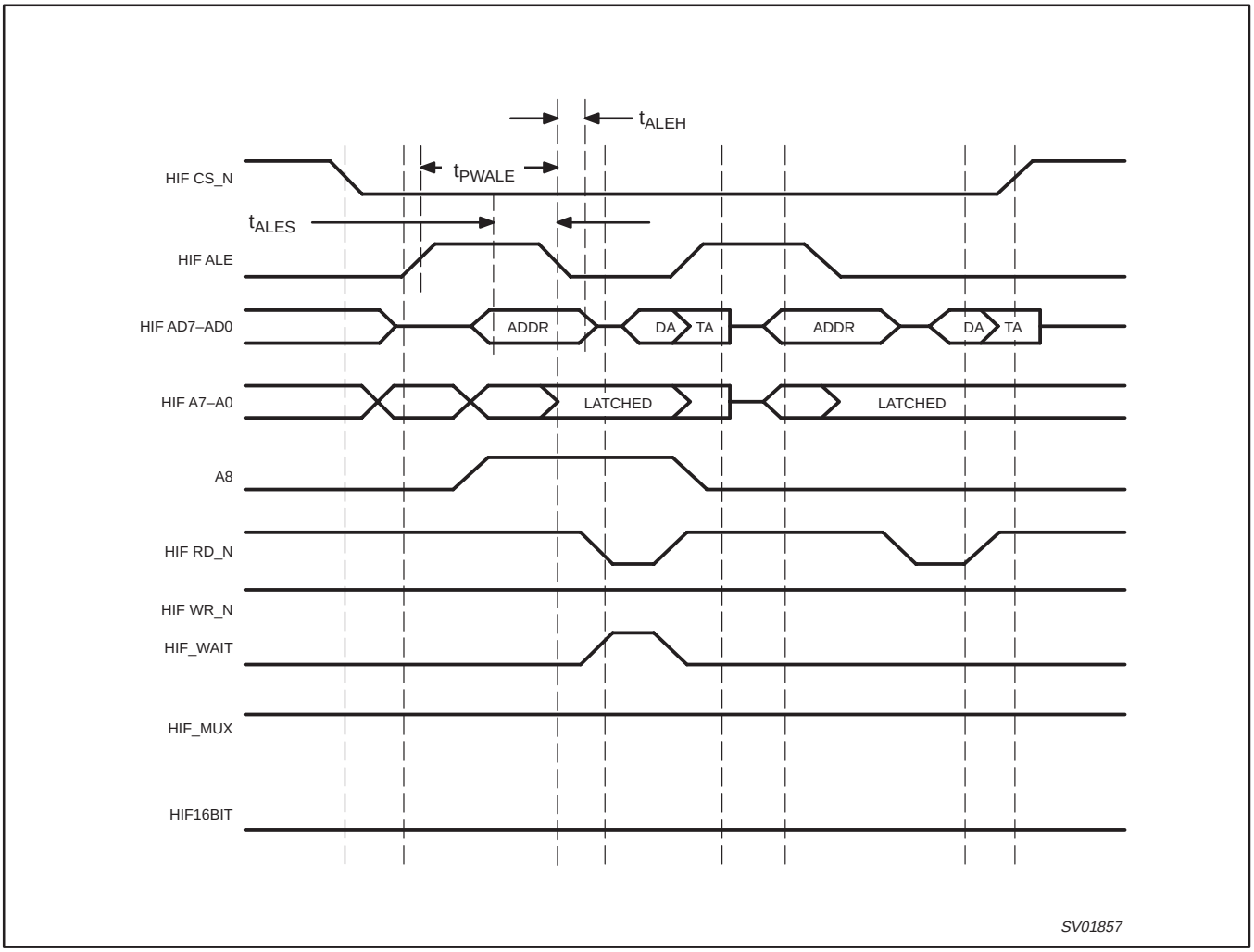
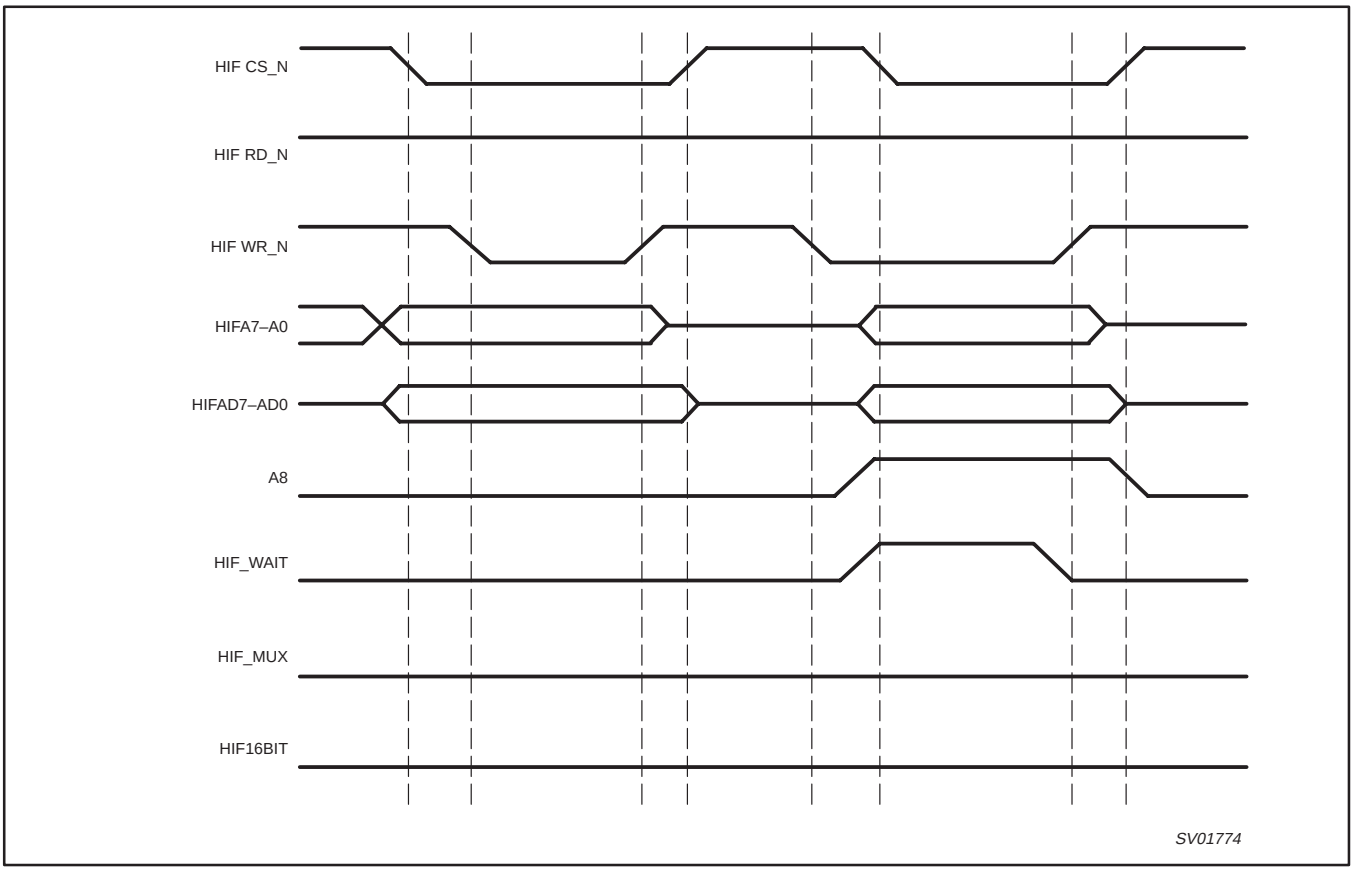
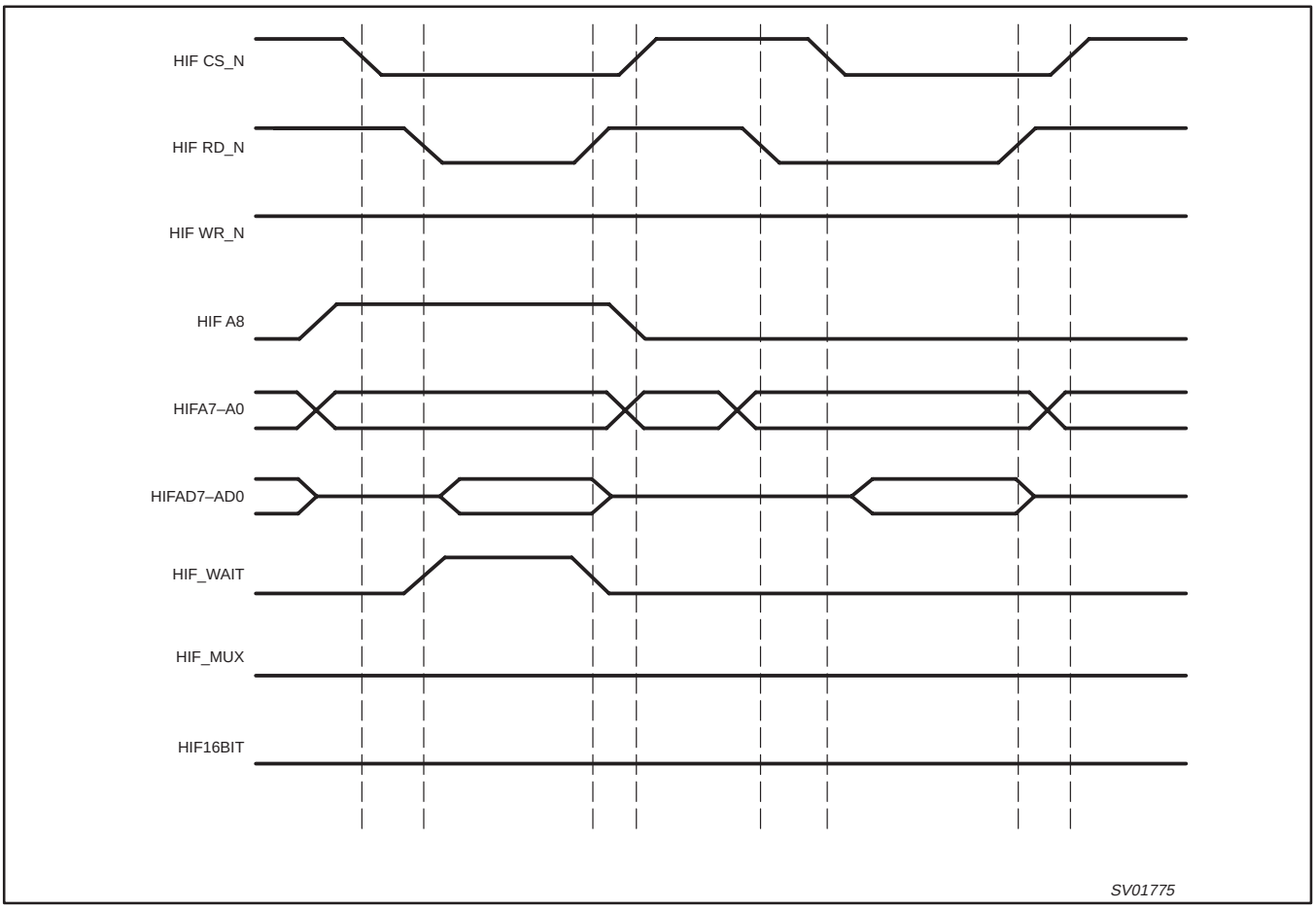


Figure 11. 8 Bit Read Cycle Multiplexed



NOTE:
1. ALE line is held LOW.

Figure 12. 8 Bit Write Cycle Non-multiplexed



NOTE:
1. ALE line is held LOW.

Figure 13. 8 Bit Read Cycle Non-multiplexed

12.6 The Asynchronous Packet Interface

The PDI1394L40 provides an interface to asynchronous data packets through the registers in the host interface. The format of the asynchronous packets is specified in the following sections.

12.6.1 Reading an Asynchronous Packet

Upon reception of a packet, the packet data is stored in the appropriate receive FIFO, either the Request or Response FIFO. The location of the packet is indicated by either the RREQQQAV or RRSPQAV status bit being set in the Asynchronous Interrupt Acknowledge (ASYINTACK) register. The packet is transferred out of the FIFO by successive reads of the Asynchronous Receive Request (RREQ) or Asynchronous Receive Response (RRSP) register. The end of the packet (the last quadlet) is indicated by either the RREQQLASTQ or RRSPQLASTQ bit set in ASYINTACK. Attempting to read the FIFO when either RREQQQAV bit or RRSPQQAV bit is set to 0 (in the Asynchronous RX/TX interrupt acknowledge, ASYINTACK, register) will result in a queue read error.

12.6.2 Link Packet Data Formats

The data formats for transmission and reception of data are shown below. The transmit format describes the expected organization for data presented to the link at the asynchronous transmit, physical response, or isochronous transmit FIFO interfaces.

12.6.2.1 Asynchronous Transmit Packet Formats

These sections describe the formats in which packets need to be delivered to the queues (FIFOs) for transmission. There are four basic formats as follows:

ITEM	FORMAT	USAGE	TRANSACTION CODE (tCode)
1	No-packet data	Quadlet read requests	4
		Quadlet/block write responses	2
2	Quadlet packet	Quadlet write requests	0
		Quadlet read responses	6
		Block read requests	5
3	Block Packet	Block write requests	1
		Block read responses	7
		Lock requests	9
		Lock responses	B_{hex}
		Asynchronous streams	A_{hex}
4	Unformatted transmit	Concatenated self-ID / PHY packets	E_{hex}

Each packet format uses several fields (see names and descriptions below). More information about these fields (not the format) can be found in the 1394 specification. Grey fields are reserved and should be set to zero values.

Table 1. Asynchronous Transmit Fields

Field Name	Description
spd	This field indicates the speed at which this packet is to be sent. 00=100 Mbs, 01=200 Mbs, and 10=400 Mbs. 11 = undefined
tLabel	This field is the transaction label, which is used to pair up a response packet with its corresponding request packet. tLabels are also used as identifiers to associate a Link data confirmation (see 12.6.2.13) with the corresponding request, response, or asynchronous stream packet.
rt	Only value 01 = retryX is supported.
tCode	The transaction code for this packet.
DestinationID	Contains a node ID value.
DestinationOffsetHigh DestinationOffsetLow	The concatenation of these two field addresses a quadlet in the destination node's address space.
rCode	Response code for write response packet. **rCode** **Meaning** 0 Node successfully completed requested operation. 1–3 Reserved 4 Resource conflict detected by responding agent. Request may be retried. 5 Hardware error. Data not available. 6 Field within request packet header contains unsupported or invalid value. 7 Address location within specified node not accessible. 8–Fh Reserved
channel	A channel allocated from the isochronous manager register CHANNELS_AVAILABLE.
tag	Used only for Asynchronous stream transmit fields. Values supplied, as appropriate, by the user.
sy	
priority	For responses, priority is set to 0000 if fair arbitration is to be used and to 0001 if priority arbitration is to be used, as allowed by the 1394a supplement to Std IEEE 1394–1995.
Quadlet data	For quadlet write requests and quadlet read responses, this field holds the data to be transferred.
Data length	The number of bytes requested in a block read request.
dataLength	The number of bytes of data to be transmitted in this packet
extendedTcode	The tCode indicates a lock transaction, this specifies the actual lock action to be performed with the data in this packet.
block data	The data to be sent. If dataLength=0, no data should be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block must appear in the high order byte of the first quadlet.
padding	If the dataLength mod 4 is not zero, then zero-value bytes are added onto the end of the packet to guarantee that a whole number of quadlets is sent.

12.6.2.2 No-data Transmit

The no-data transmit formats are shown in Figures 14 and 15. The first quadlet contains packet control information. The second and third quadlets contain 16-bit destination ID and either the 48-bit, quadlet aligned destination offset (for requests) or the response code (for responses).

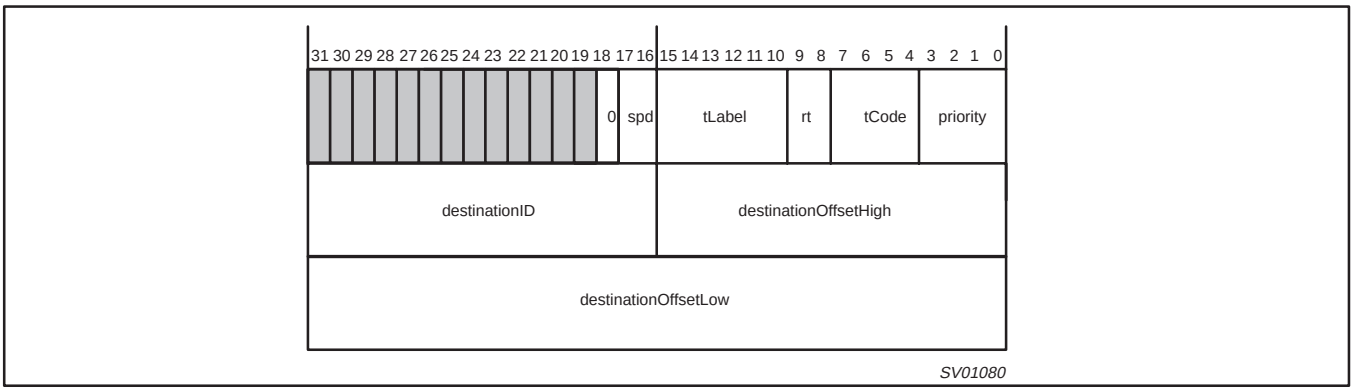


Figure 14. Quadlet Read Request Transmit Format

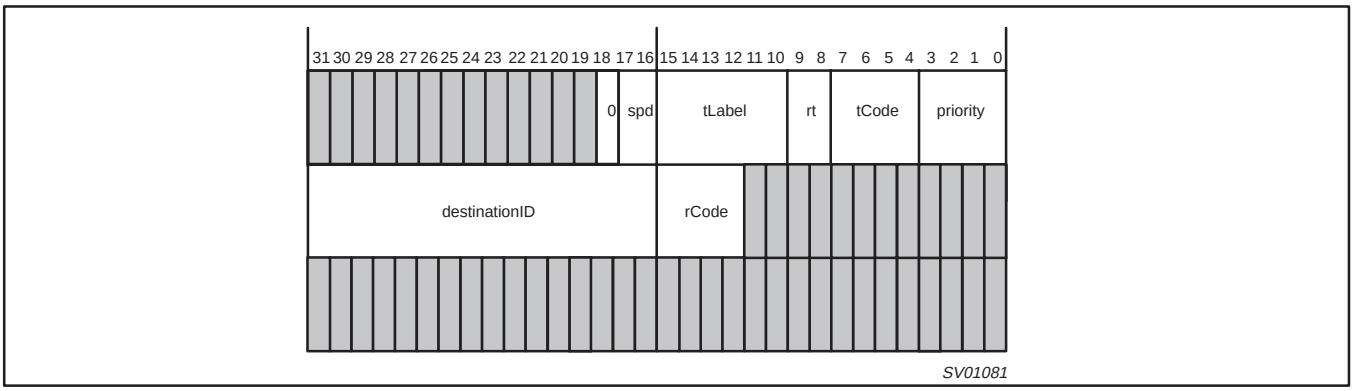


Figure 15. Quadlet/Block Write Response Transmit Format

12.6.2.3 Quadlet Transmit

Three quadlet transmit formats are shown below. In these figures: The first quadlet contains packet control information. The second and third quadlets contain 16-bit destination ID and either the 48-bit quadlet-aligned destination offset (for requests) or the response code (for responses).

The fourth quadlet contains the quadlet data for read response and write quadlet request formats, or the upper 16 bits contain the data length for the block read request format.

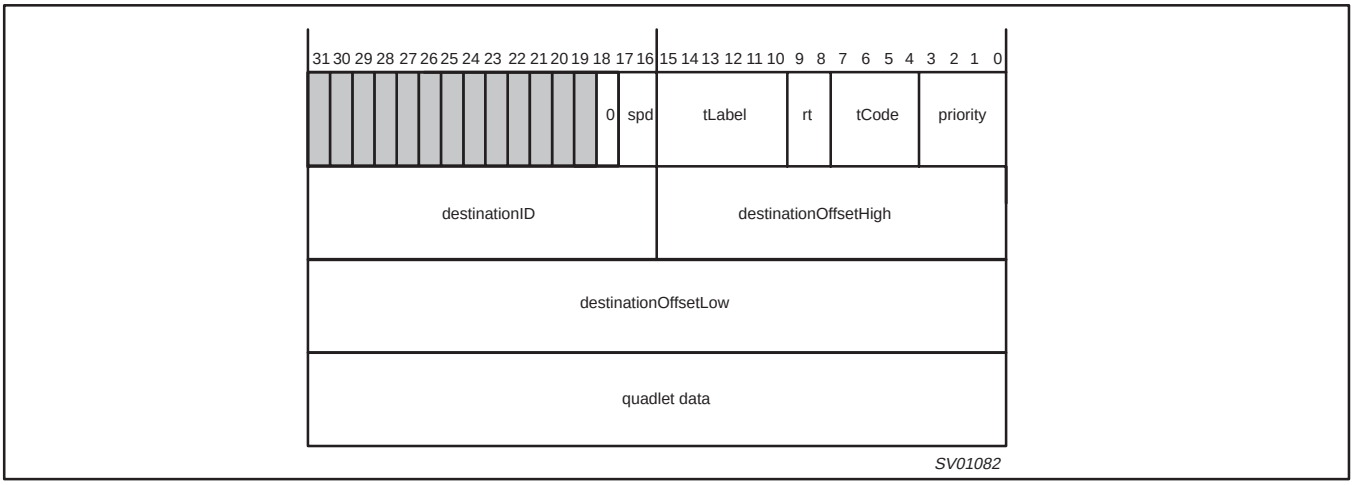


Figure 16. Quadlet Write Request Transmit Format

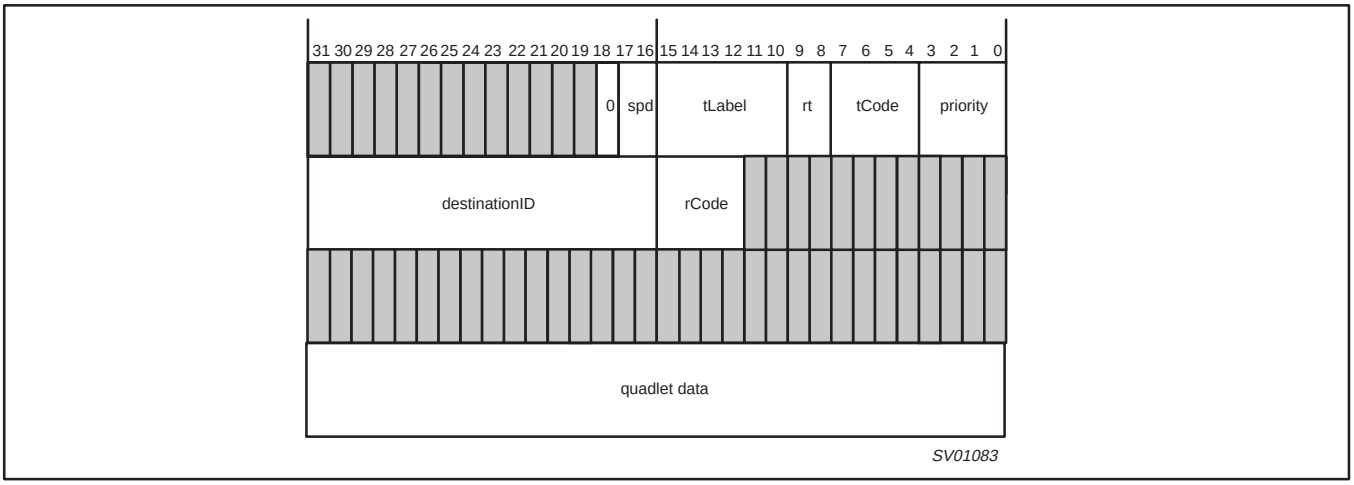


Figure 17. Quadlet Read Response Transmit Format

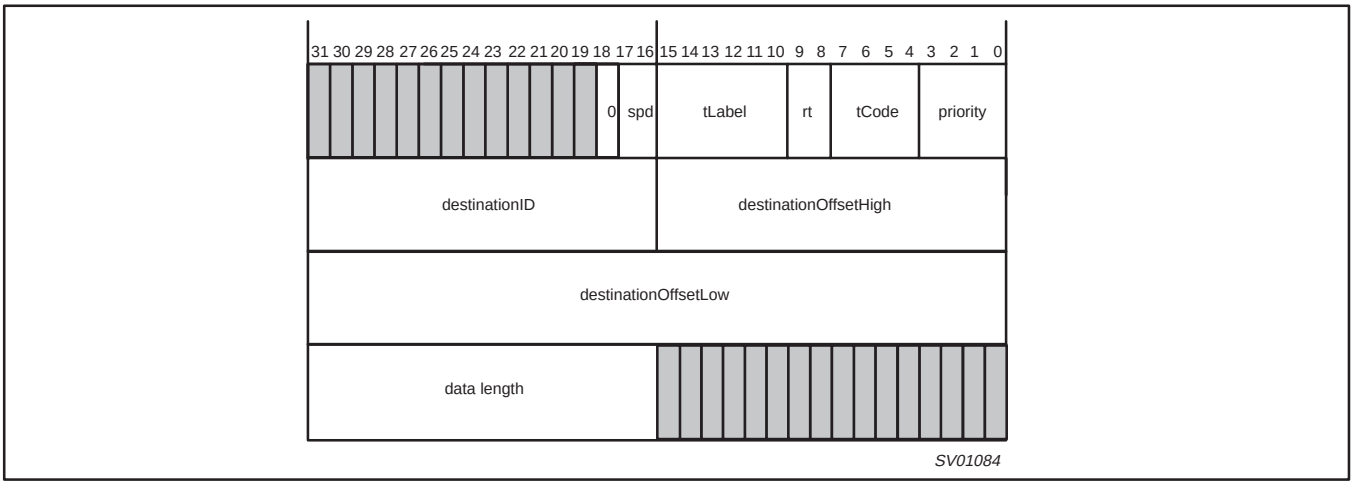


Figure 18. Block Read Request Transmit Format

12.6.2.4 Block Transmit

The block transmit format is shown below, this is the generic format for reads and writes. The first quadlet contains packet control information. The second and third quadlets contain the 16-bit destination node ID and either the 48-bit destination offset (for requests) or the response code and reserved data (for responses). The fourth quadlet contains the length of the data field and the extended transaction code (all zeros except for lock transaction). The block data, if any, follows the extended transaction code.

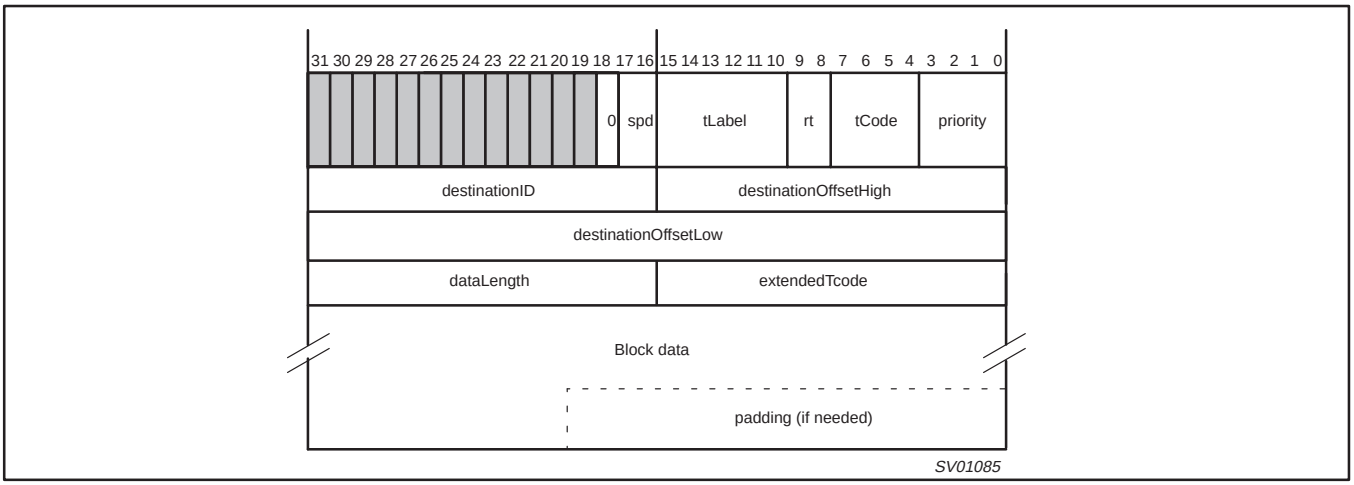


Figure 19. Block Packet Write Request Format

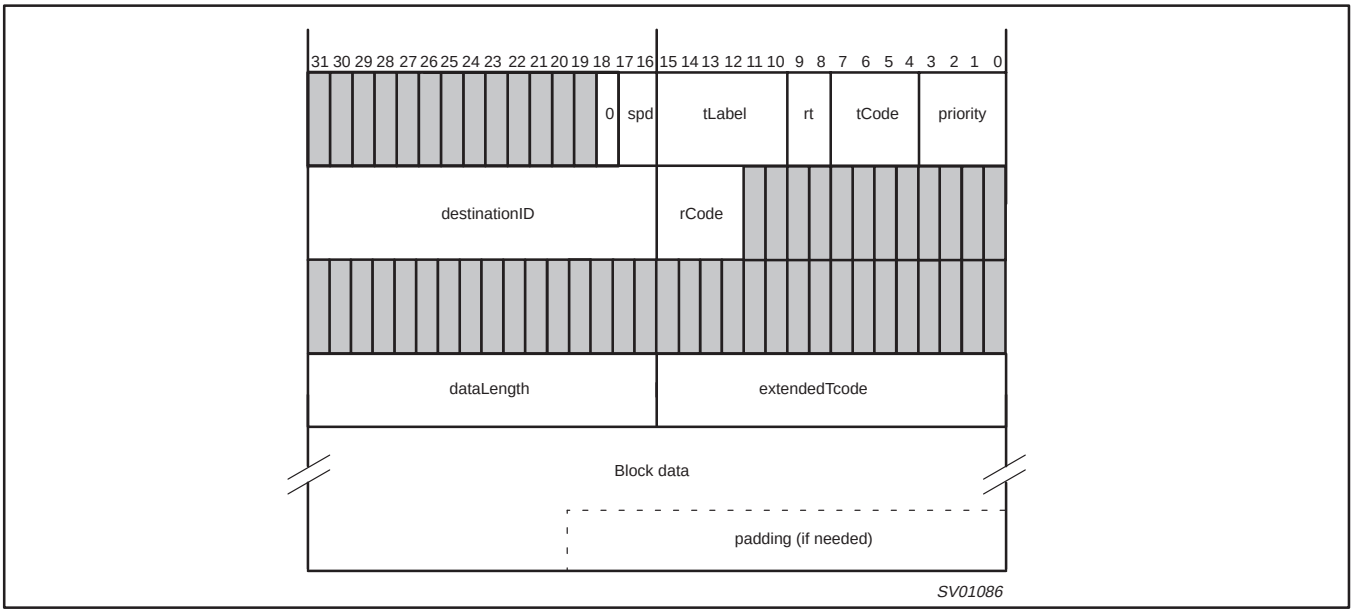


Figure 20. Block Read or Lock Response Transmit Format

12.6.2.5 Unformatted Transmit

The unformatted transmit format is shown in Figure 21. The first quadlet contains packet control information. The remaining quadlets contain data that is transmitted without any formatting on the bus. No CRC is appended on the packet, nor is any data in the first quadlet sent. This is used to send PHY configuration and Link-on packets. Note that the bit-inverted check quadlet must be included in the FIFO since the AV Link core will not generate it.

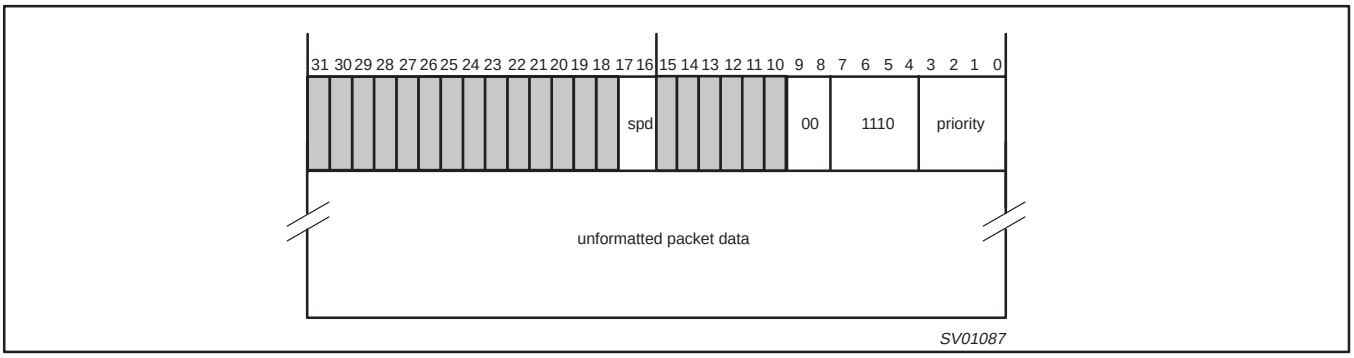


Figure 21. Unformatted Transmit Format

12.6.2.6 Asynchronous Stream Transmit

The PDI1394L40 supports asynchronous stream as specified in IEEE1394a-2000. The asynchronous stream packet format is shown below. The first quadlet contains packet control information. The second quadlet contains datalength, tag, channel number, and synchronization code. The third quadlet contains the datalength in quadlets. The datalength can be zero for empty asynchronous stream packets.

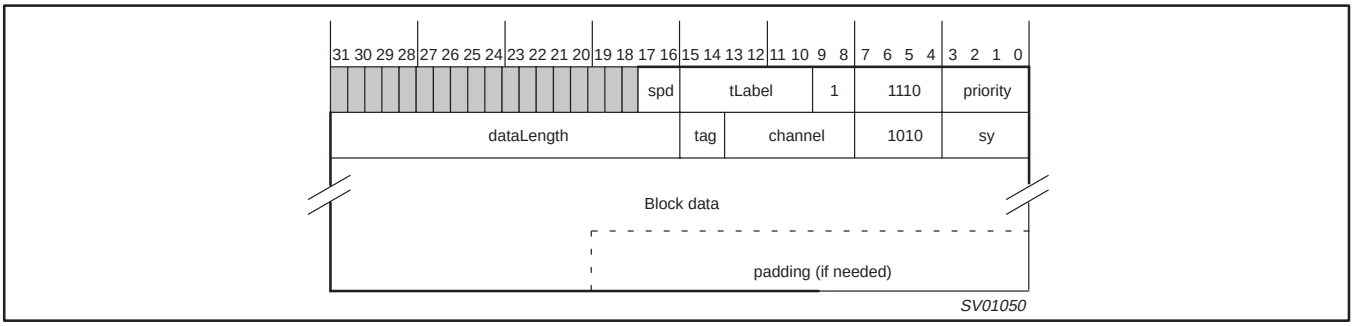


Figure 22. Asynchronous Stream Packet Transmit Format

When a packet conforming to this format is written to either asynchronous transmit FIFO, an asynchronous stream packet (identical on the cable to an isochronous packet) will be transmitted during the asynchronous phase of a bus cycle.

12.6.2.7 Asynchronous Receive Packet Formats

This section describes the asynchronous receive packet formats. Four basic asynchronous data packet formats and one confirmation format exist:

Table 2. Asynchronous Data Packet Formats

ITEM	FORMAT	USAGE	TRANSACTION CODE
1	No-packet data	Quadlet read requests	4
		Quadlet/block write responses	2
2	Quadlet packet	Quadlet write requests	0
		Quadlet read responses	6
3	Block Packet	Block read requests	5
		Block write requests	1
		Block read responses	7
		Lock requests	9
		Lock responses	B_{hex}
4	Self-ID / PHY packet	Concatenated self-ID / PHY packets	E_{hex}
5	Confirmation packet	Confirmation of packet transmission	8

Each packet format uses several fields. More information about most of these fields can be found in the 1394 specification.

Table 3. Asynchronous Receive Fields

Field Name	Description
destinationID	This field is the concatenation of busNumbers (or all ones for “local bus”) and nodeNumbers (or all ones for broadcast) for this node.
tLabel	This field is the transaction label, which is used to pair up a response packet with its corresponding request packet. tLables are also used as identifiers to associate a Link data confirmation (see 12.6.2.13) with the corresponding request, response, or asynchronous stream packet.
rt	The retry code of the received packet; see the 1394 specification.
tCode	The transaction code for this packet.
priority	The priority level for this packet (0000 for cable environment).
sourceID	This is the node ID of the sender of this packet.
destinationOffsetHigh, destinationOffsetLow	The concatenation of these two field addresses a quadlet in this node’s address space.
rCode	Response code for the received packet; see the 1394 specification.
quadlet data	For quadlet write requests and quadlet read responses, this field holds the data received.
dataLength	The number of bytes of data to be received in a block packet.
extendedTcode	If the tCode indicates a lock transaction, this specifies the actual lock action to be performed with the data in this packet.
block data	The data received. If dataLength=0, no data will be written into the FIFO for this field. Regardless of the destination or source alignment of the data, the first byte of the block will appear in the high order byte of the first quadlet.
padding	If the dataLength mod 4 is not zero, then zero-value bytes are added onto the end of the packet to guarantee that a whole number of quadlets is sent.
u	Unsolicited response tag bit. This bit is set to one (1) if the received response was unsolicited.
ackSent	This field contains the acknowledge code that the link layer returned to the sender of the received packet. For packets that do not need to be acknowledged (such as broadcasts) the field contains the acknowledge value that would have been sent if an acknowledge had been required. The values for this field are listed in Table 4 (they also can be found in the IEEE 1394 standard).
status	This field is used for asynchronous streams. 0000 Reserved. 0001 packet OK. 0010–1100 Reserved. 1101 Data CRC error and/or block size mismatch have been detected. 1110–1111 Reserved.

Table 4. Acknowledge codes

Code	Name	Description
0001	ack_complete	The node has successfully accepted the packet. If the packet was a request subaction, the destination node has successfully completed the transaction and no response subaction shall follow.
0010	ack_pending	The node has successfully accepted the packet. If the packet was a request subaction, a response subaction will follow at a later time. This code shall not be returned for a response subaction.
0100	ack_busy_X	The packet could not be accepted. The destination transaction layer may accept the packet on a retry of the subaction.
0101	ack_busy_A	The packet could not be accepted. The destination transaction layer will accept the packet when the node is not busy during the next occurrence of retry phase A.
0110	ack_busy_B	The packet could not be accepted. The destination transaction layer will accept the packet when the node is not busy during the next occurrence of retry phase B.
1101	ack_data_error	The node could not accept the block packet because the data field failed the CRC check, or because the length of the data block payload did not match the length contained in the dataLength field. This code shall not be returned for any packet that does not have a data block payload.
1110	ack_type_error	A field in the request packet header was set to an unsupported or incorrect value, or an invalid transaction was attempted (e.g., a write to a read-only address).
0000, 0011, 0111 – 1100, and 1111	reserved	This revision of the AV Link will not generate other acknowledge codes, but may receive them from newer (1394a-2000) links. In that case, these new values will show up here.

12.6.2.8 No-data Receive

The no-data receive formats are shown below. The first quadlet contains the destination node ID and the rest of the packet header. The second and third quadlet contain 16-bit source ID and either the 48-bit, quadlet-aligned destination offset (for requests) or the response code (for responses). The last quadlet contains packet reception status.

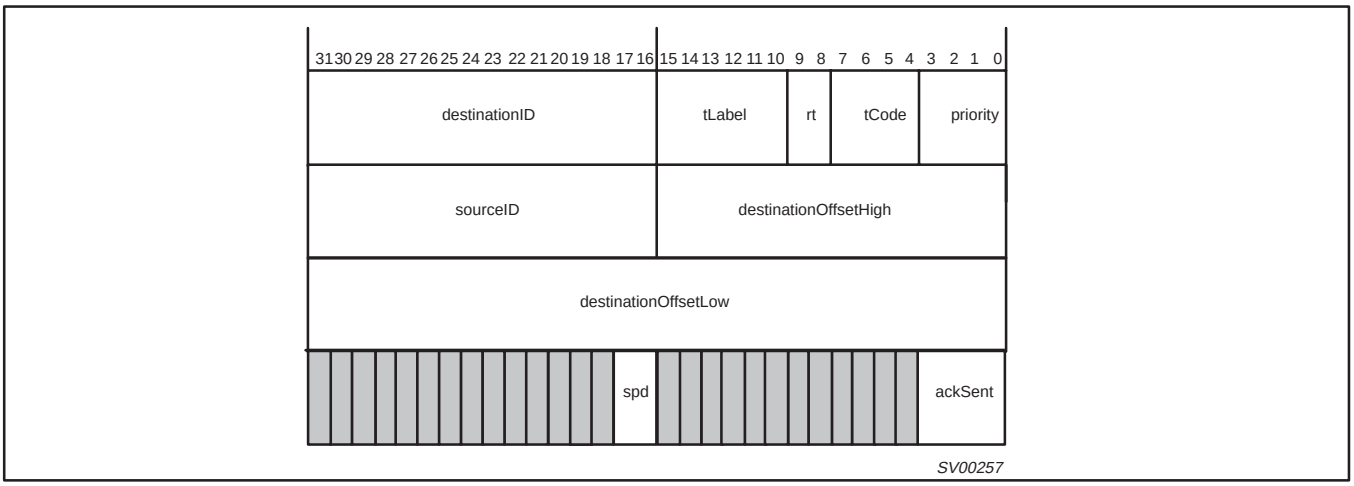


Figure 23. Quadlet Read Request Receive Format

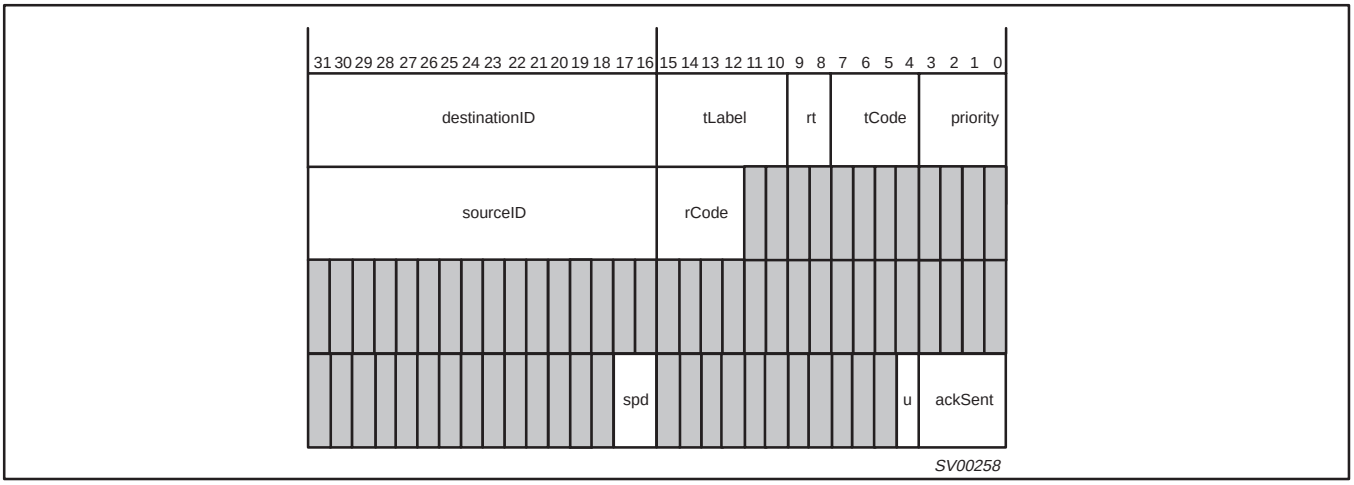


Figure 24. Write Response Receive Format

12.6.2.9 Quadlet Receive

The quadlet receive formats are shown below. The first quadlet contains the destination node ID and the rest of the packet header. The second and third quadlets contain 16-bit source ID and either the 48-bit, quadlet-aligned destination offset (for requests) or the response code (for responses). The fourth quadlet is the quadlet data for read responses and write quadlet requests, and is the data length and reserved for block read requests. The last quadlet contains packet reception status.

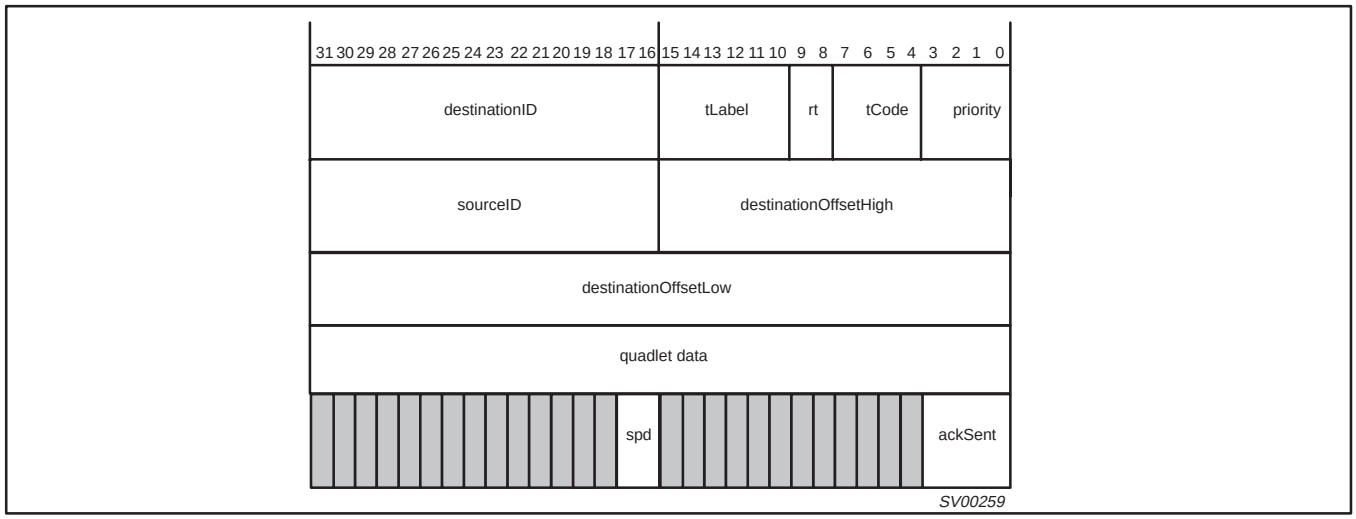


Figure 25. Quadlet Write Request Receive Format

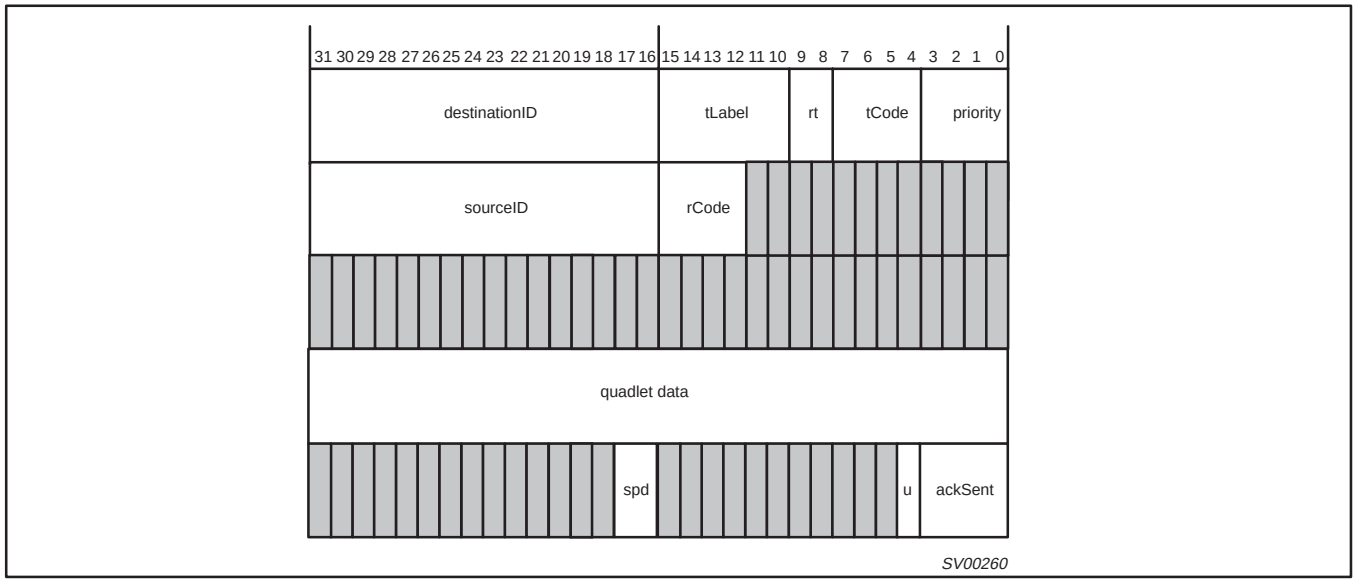


Figure 26. Quadlet Read Response Receive Format

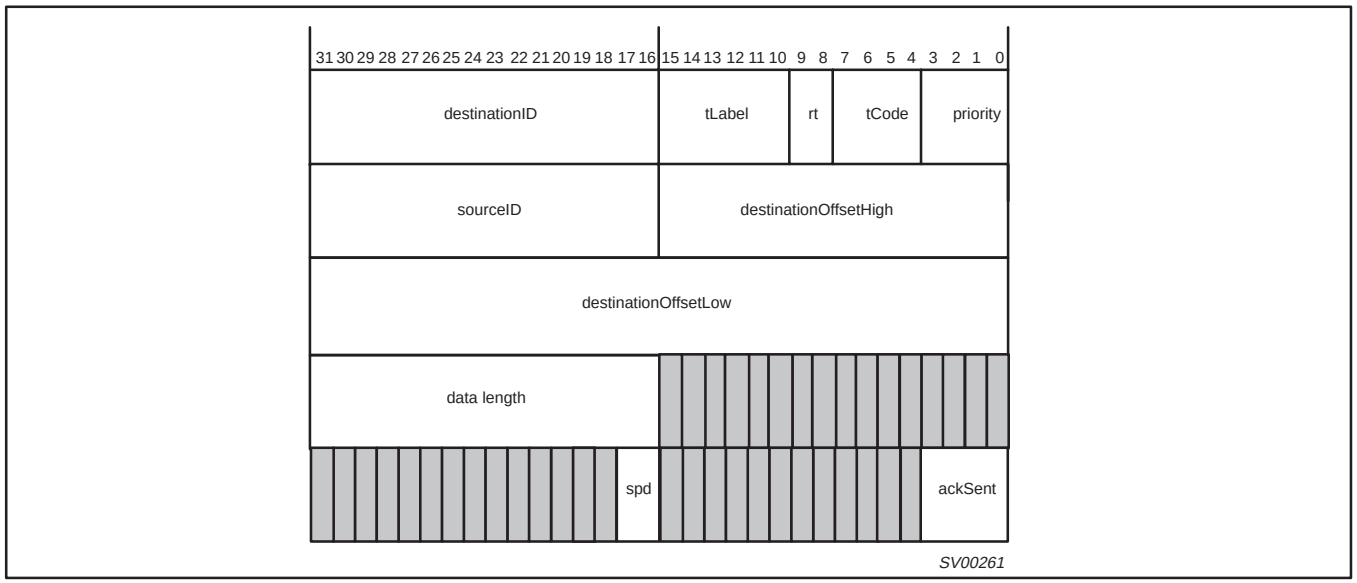


Figure 27. Block Read Request Receive Format

12.6.2.10 Block receive

The block receive format is shown below. The first quadlet contains the destination node ID and the rest of the packet header. The second and third quadlets contain 16-bit sourceID and either the 48-bit destination offset (for requests) or the response code and reserved data (for responses). The fourth quadlet contains the length of the data field and the extended transaction code (all zeros except for lock transactions). The block data, if any, follows the extended code. The last quadlet contains packet reception status.

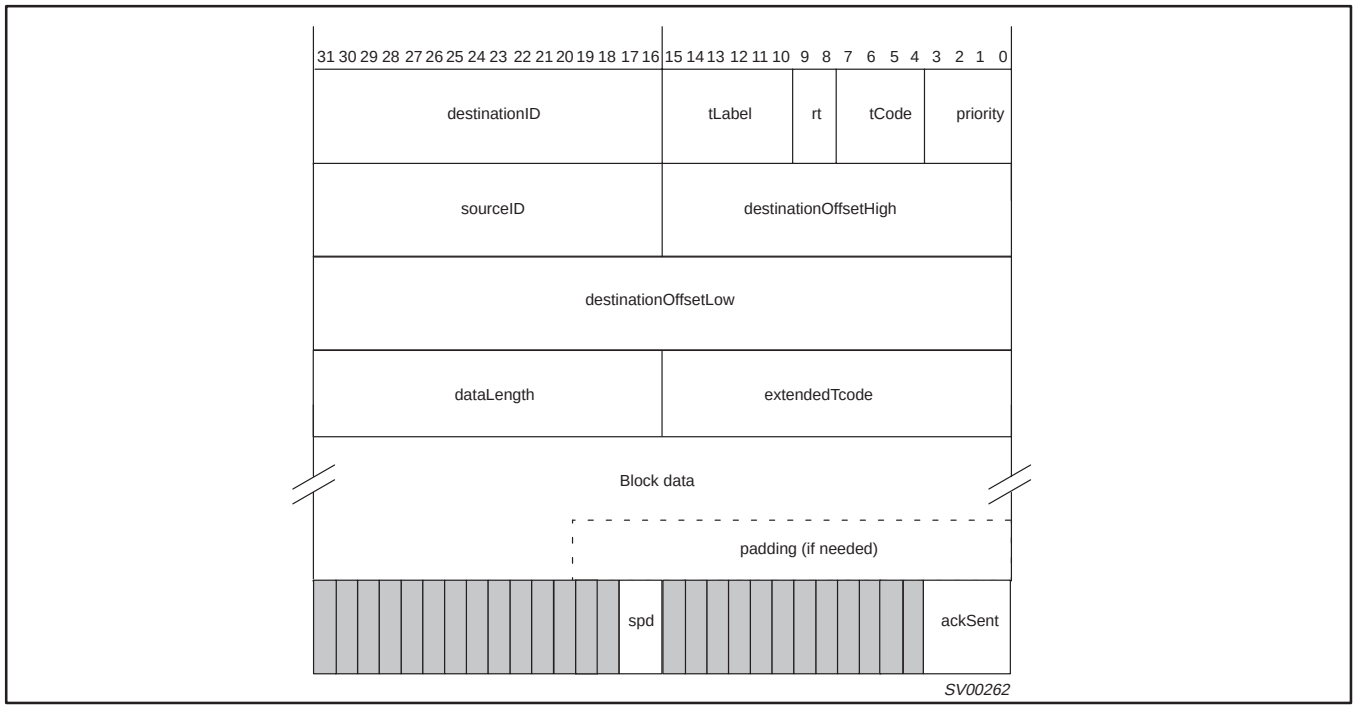


Figure 28. Block Write or Lock Request Receive Format

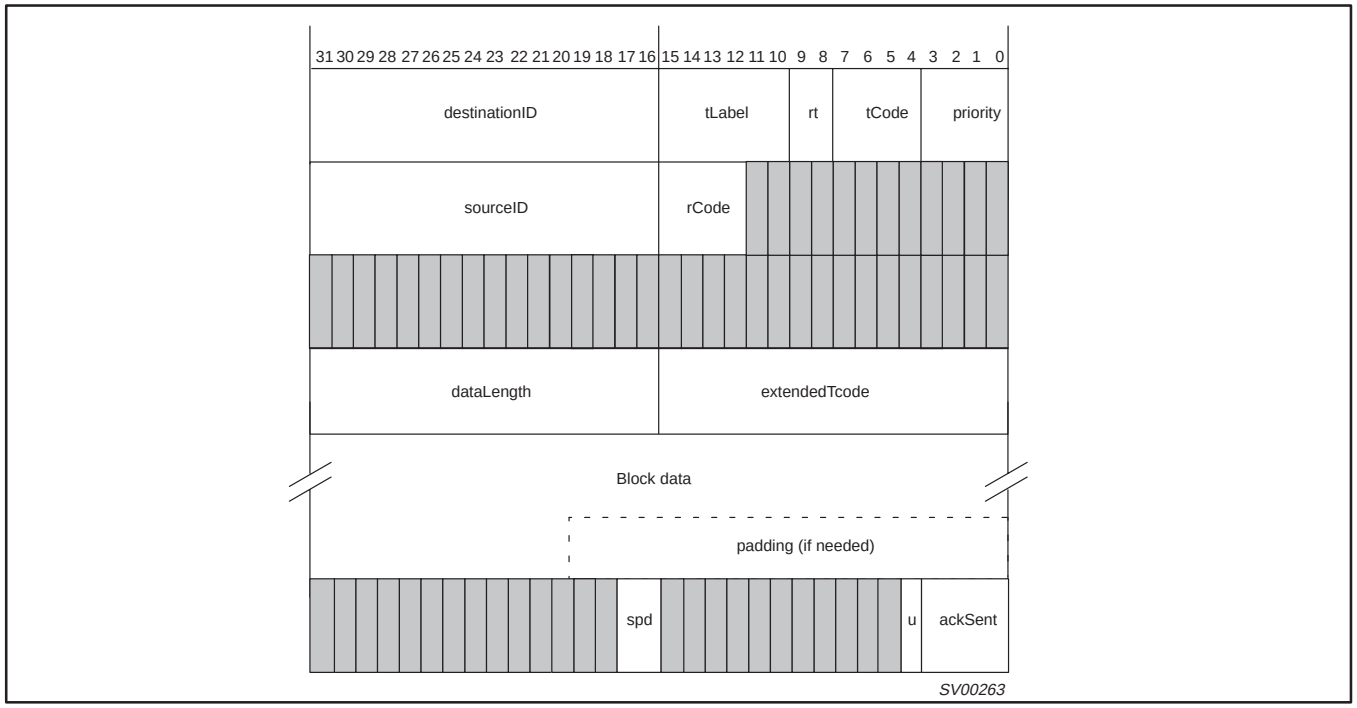


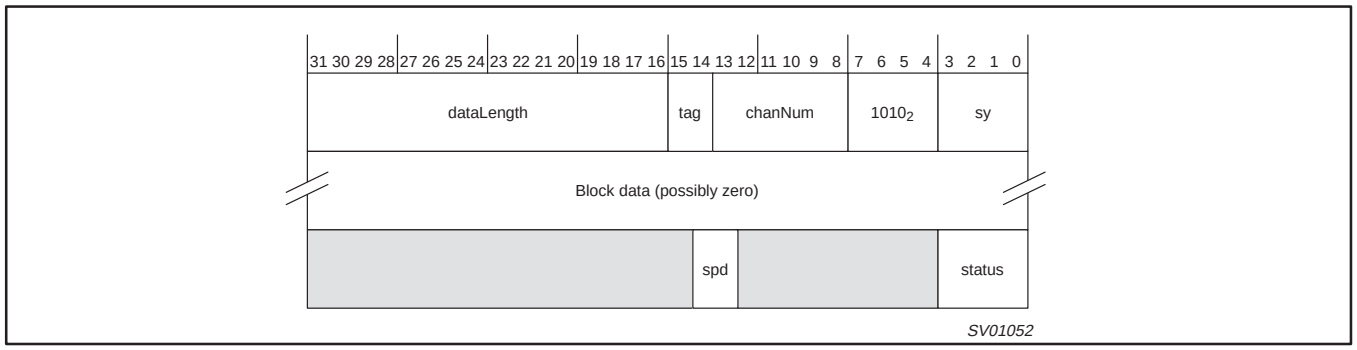
Figure 29. Block Read or Lock Response Receive Format

12.6.2.11 Asynchronous Stream Receive

The Asynchronous streaming receive packet format is shown below. The first quadlet contains dataLength, tag, and Channel number for source identification, and synchronization information. The following quadlets contain (possibly zero) quadlets of block information. The last quadlet contains transmission speed and status information. Asynchronous stream packets are placed in the Receive Response FIFO.

NOTE:

1. Due to the fact that an asynchronous stream packet is a type of isochronous packet, the STRICTISOCH bit (bit 12 in register 0x004) must be set to “0” for correct operation.



12.6.2.12 Self-ID and PHY packets receive

The self-ID and PHY packet receive formats are shown below. The first quadlet contains a synthesized packet header with a tCode of 0xE (hex). For self-ID information, the remaining quadlets contain data that is received from the time a bus reset ends to the first subaction gap. This is the concatenation of all the self-ID packets received. Note that the bit-inverted check quadlet is included in the Read Request FIFO and the application must check it.

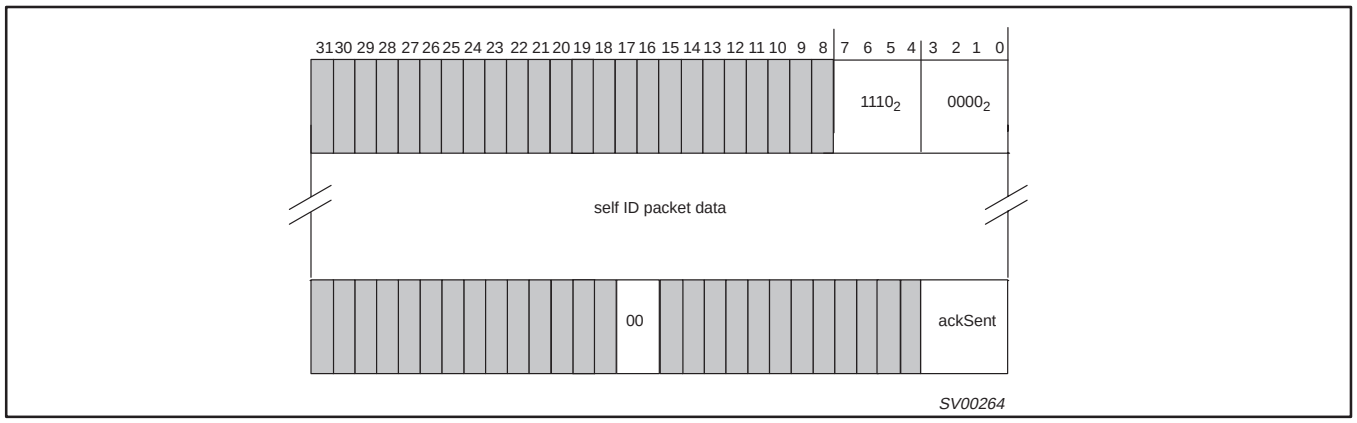


Figure 30. Self-ID Receive Format

The “ackSent” field will either be “ACK_DATA_ERROR” if a non-quadlet-aligned packet is received or there was a data overrun, or “ACK_COMPLETE” if the entire string of self-ID packets was received.

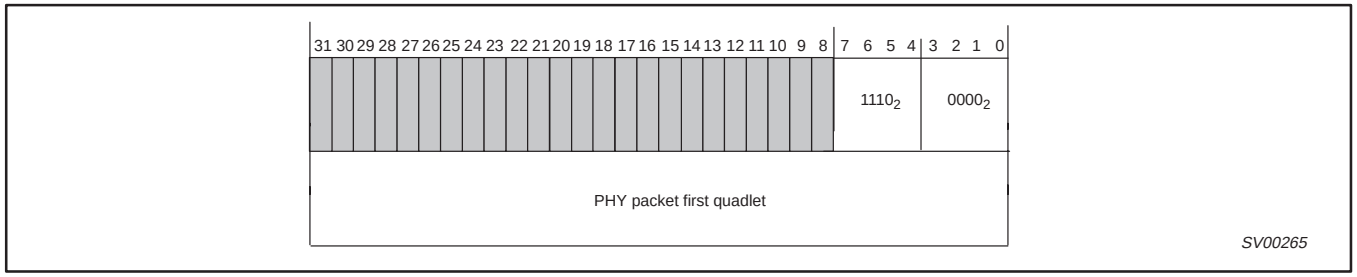


Figure 31. PHY Packet Receive Format

For PHY packets, there is a single following quadlet which is the first quadlet of the PHY packet. The check quadlet has already been verified and is not included.

12.6.2.13 Link data confirmation formats

After a request, response, or asynchronous stream packet is transmitted, the asynchronous transmitter assembles a Link data confirmation (see Figure 32) which is used to confirm the transmission to the higher layers. Packets transmitted from the Transmit Request FIFO are confirmed by a confirmation written into the Receive Request FIFO and packets transmitted from the Transmit Response FIFO are confirmed by a confirmation written into the Receive Response FIFO.

Outgoing packets and their confirmations are associated by their tLabels. It is the user's responsibility to assure the uniqueness of active tLabels.

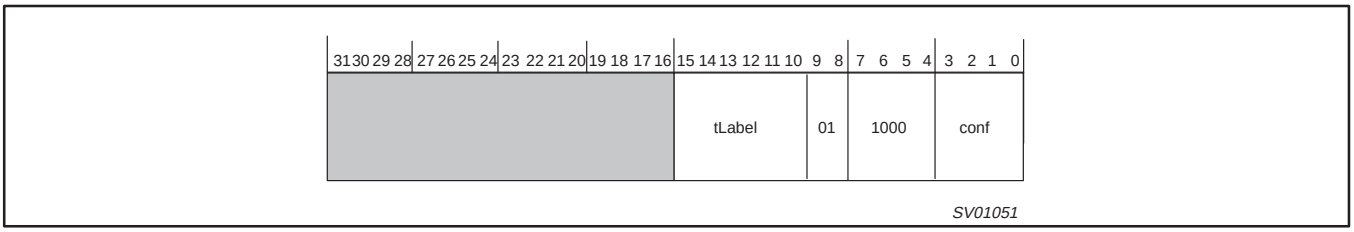


Figure 32. Request and response confirmation format

Table 5. Confirmation codes

CODE[1]	DESCRIPTION
0	Non-broadcast packet transmitted; addressed node returned no acknowledge (transaction complete).
1	Broadcast packet transmitted or non-broadcast packet transmitted; addressed node returned an acknowledge complete (transaction complete).
2	Non-broadcast packet transmitted; addressed node returned an acknowledge pending.
4	Retry limit exceeded; destination node hasn't accepted the non-broadcast packet within the maximum number of retries (transaction complete).
D_{16}	Acknowledge data error received (transaction complete).
E_{16}	Acknowledge type error received (transaction complete).

NOTE:
1. All other codes are reserved.

12.7 Interrupts

The PDI1394L40 provides a single interrupt line (HIF INTN) for connection to a host controller. Status indications from five major areas of the device are collected and ORed together to activate HIF INTN. Status from four major areas of the device are collected in five status registers; LNKPHYINTACK, ITXINTACK, IRXINTACK, ASYINTACK and RDI. At this level, each individual status can be enabled to generate a chip-level interrupt by activating HIF INTN. To aid in determining the source of a chip-level interrupt, the major area of the device generating an interrupt is indicated in the lower 4 bits of the GLOBCSR register. These bits are non-latching Read-Only status bits and do not need to be acknowledged. To acknowledge and clear a standing interrupt, the bit in LNKPHYINTACK, ITXINTACK, IRXINTACK, ASYINTACK or RDI causing the interrupt status has to be written to a logic '1'; Note: Writing a value of '0' to the bit has no effect.

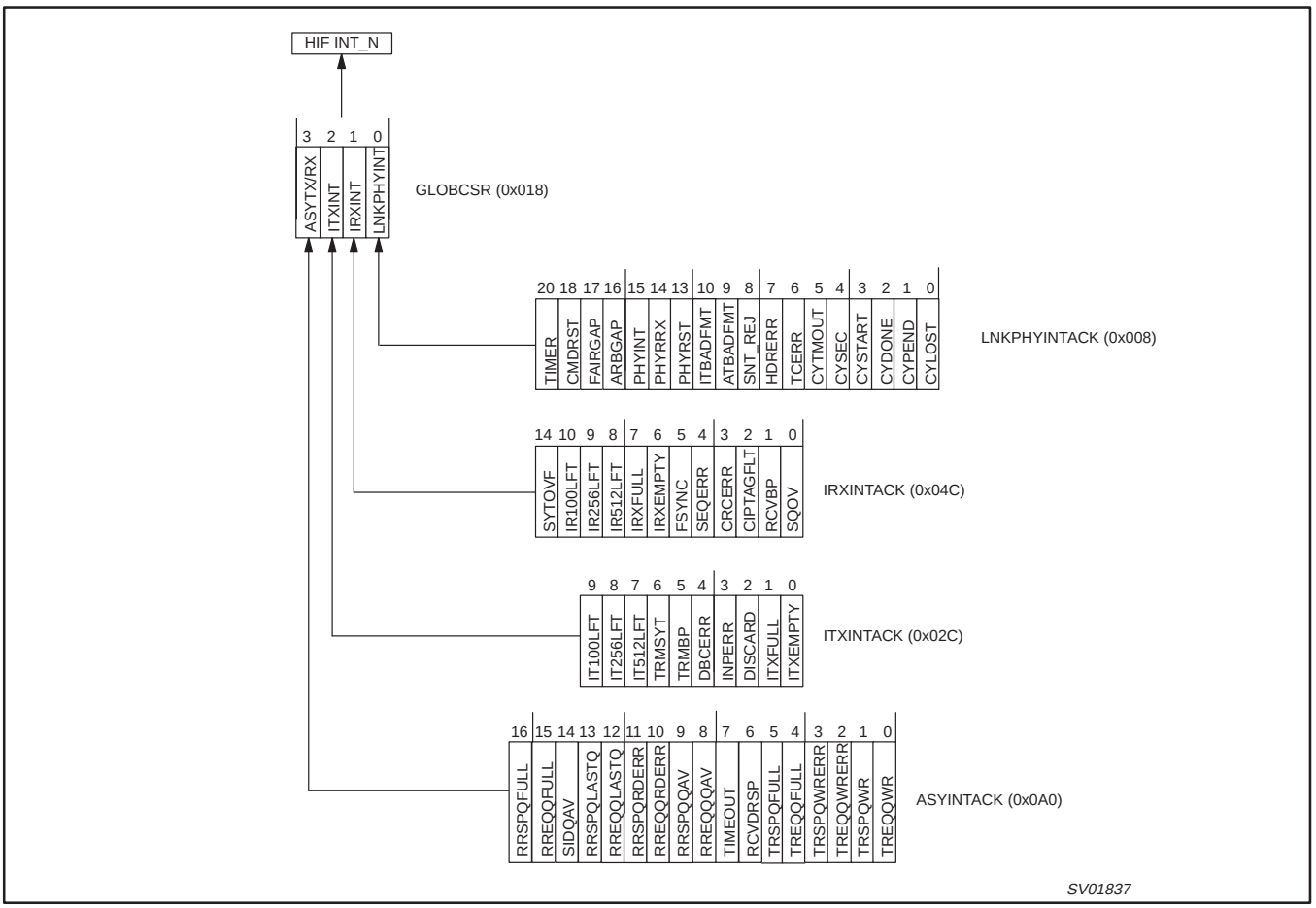
12.7.1 Determining and Clearing Interrupts

When responding to an interrupt event generated by the PDI1394L40, or operating in polled mode, the first register examined is the RDI register. Since the addition of the RDI register (at 0x0b0), it will be necessary to first interrogate the RDI register independent of the GLOBCSR register in order to locate the source of an interrupt. Embedded software should be built to perform this function. It is recommended that this interrogation take place BEFORE the read of the GLOBCSR register is accomplished. The reason for this added step stems from the fact that none of the other link registers can be accurately read if the link is in power–down mode. If an attempt to read the GLOBCSR is made during link power–down, a quadlet will be read, but the quadlet data will not be the contents of the GLOBCSR. Once it has been determined that the interrupt was not a result of a bit setting in the RDI register, the GLOBCSR register should be tested next. The least significant nibble contains interrupt status bits from general sections of the device; the link layer controller, the AV transmitter, the AV receiver, and the asynchronous transceiver. The bits in GLOBCSR[3:0] are self clearing status bits. They represent the logical OR of all the enabled interrupt status bits in their section of the AV Link Layer Controller.

Once an interrupt, or status is detected in GLOBCSR, the appropriate interrupt status register needs to be read, see the Interrupt Hierarchy diagram for more detail. After all the interrupt indications are dealt with in the appropriate interrupt status register, the interrupt status indication will automatically clear in the GLOBCSR.

All interrupt status bits in the various interrupt status registers are latching unless otherwise noted.

12.7.1.1 Interrupt Hierarchy



NOTE:
1. A read of the RDI register (0xB0) should be done before looking for an interrupt in the GLOBCSR register.

Figure 33. Interrupt Hierarchy

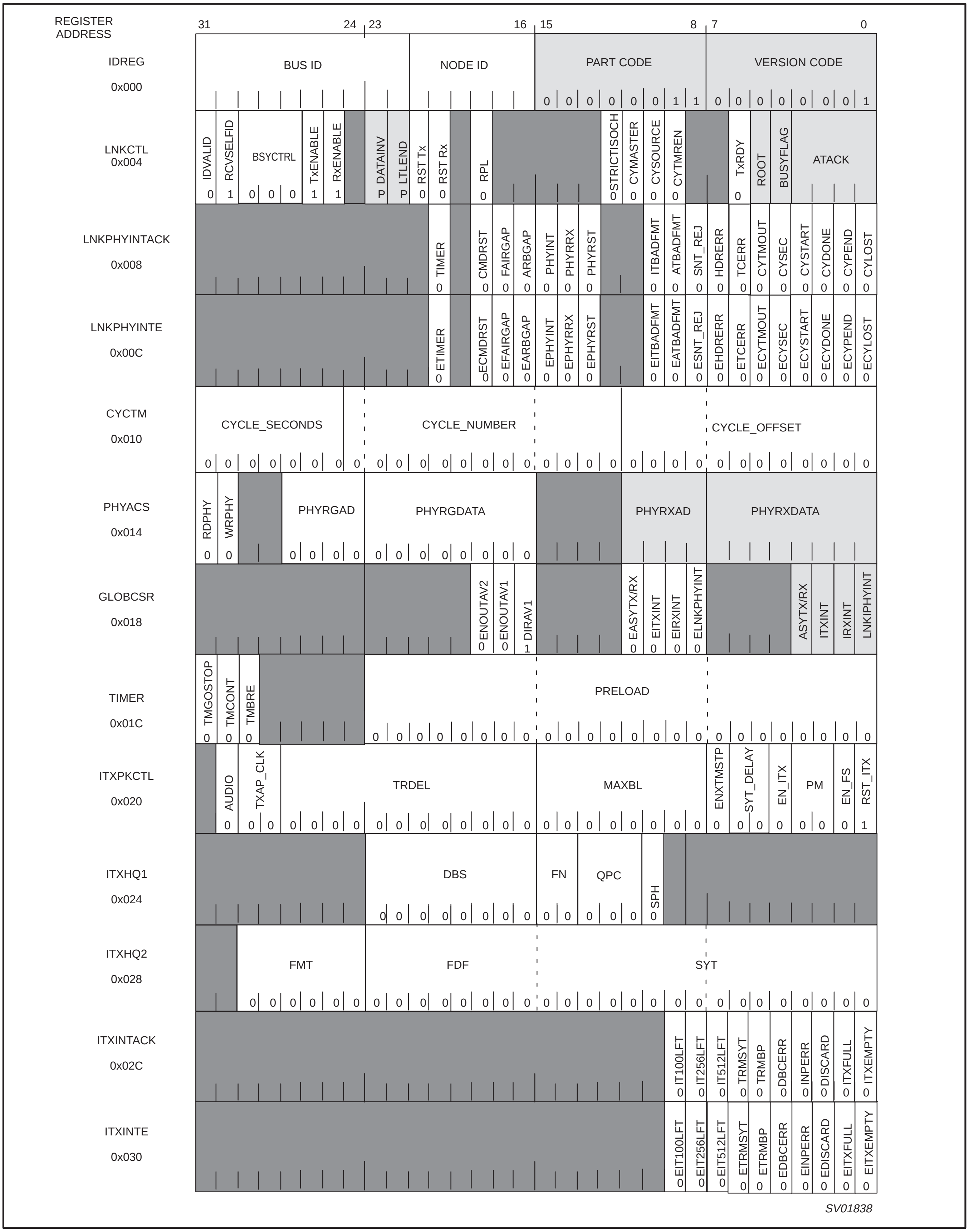
13.0 REGISTER MAP

Registers are 32 bits (quadlet) wide and all accesses are always done on a quadlet basis. This means that it is not possible to write just the lower 8 bits, and leave the other bits unaffected (see Section 12.5.2 for more information). The values written to undefined fields/bits are ignored and thus DON'T CARE.

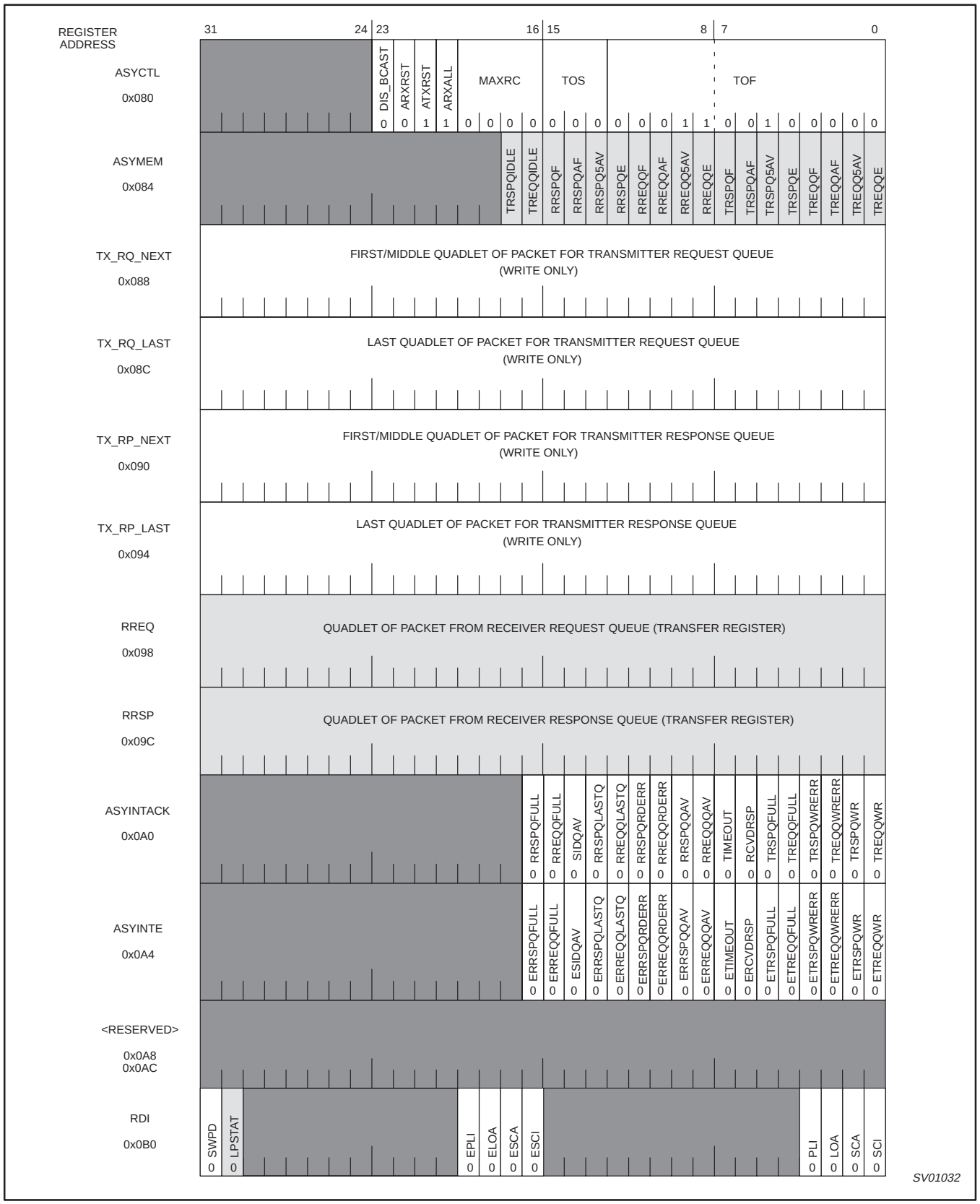
A full bitmap of all registers is listed in Table 6. The meaning of shading and bit cell values is as follows:

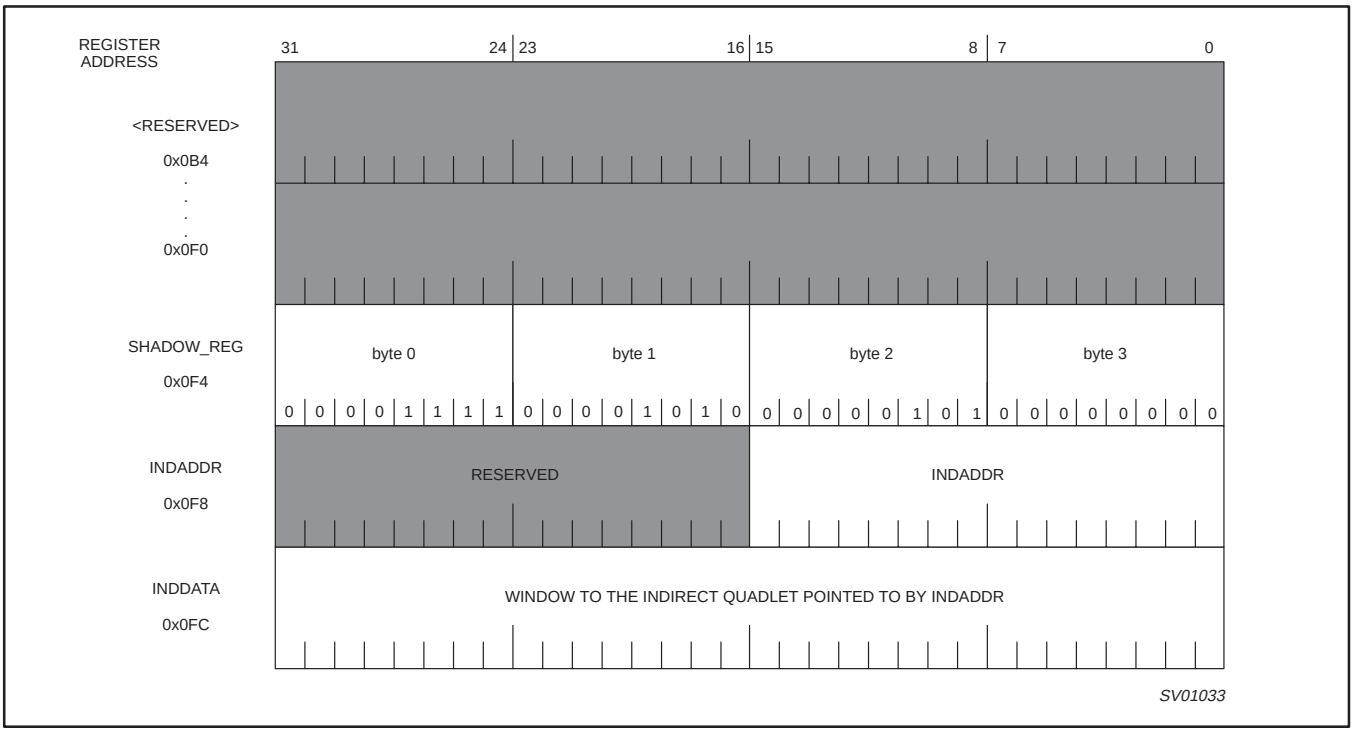
A bit/field with no name written in it and dark shading is reserved and not used.
A bit/field with a name in it and light shading is a READ ONLY (status) bit/field.
A one bit value (0 or 1) written at the bottom of a writable (control) bit is the default value after power-on-reset.

Table 6. Full Bitmap of all Registers (consists of four tables shown on the following pages)


REGISTER ADDRESS
31 24 23 16 15 8 7 0
IDREG 0x000
BUS ID
NODE ID
PART CODE
VERSION CODE
LNKCTL 0x004
IDVALID
RCVSELFID
BSYCTRL
TxENABLE
RxENABLE
DATAINV
LTLEND
RST Tx
RST Rx
RPL
STRICTISOCH
CYMASTER
CYSOURCE
CYTMREN
TxRDY
ROOT
BUSYFLAG
ATACK
LNKPHYINTACK 0x008
TIMER
CMDRST
FAIRGAP
ARBGAP
PHYINT
PHYRRX
PHYRST
ITBADFMT
ATBADFMT
SNT_REJ
HDRERR
TCERR
CYTMOUT
CYSEC
CYSTART
CYDONE
CYPEND
CYLOST
LNKPHYINTE 0x00C
ETIMER
ECMDRST
EFAIRGAP
EARBGAP
EPHYINT
EPHYRRX
EPHYRST
EITBADFMT
EATBADFMT
ESNT_REJ
EHDRERR
ETCERR
ECYTMOUT
ECYSEC
ECYSTART
ECYDONE
ECYPEND
ECYLOST
CYCTM 0x010
CYCLE_SECONDS
CYCLE_NUMBER
CYCLE_OFFSET
PHYACS 0x014
RDPHY
WRPHY
PHYRGAD
PHYRGDATA
PHYRXAD
PHYRXDATA
GLOBCSR 0x018
ENOUTAV2
ENOUTAV1
DIRAV1
EASYTX/RX
EITXINT
EIRXINT
ELNKPHYINT
ASYTX/RX
ITXINT
IRXINT
LNKIPHYINT
TIMER 0x01C
TMGOSTOP
TMCONT
TMBRE
PRELOAD
ITXPKCTL 0x020
AUDIO
TXAP_CLK
TRDEL
MAXBL
ENXTMSTP
SYT_DELAY
EN_ITX
PM
EN_FS
RST_ITX
ITXHQ1 0x024
DBS
FN
QPC
SPH
ITXHQ2 0x028
FMT
FDF
SYT
ITXINTACK 0x02C
IT100LFT
IT256LFT
IT512LFT
TRMSYT
TRMBP
DBCERR
INPERR
DISCARD
ITXFULL
ITXEMPTY
ITXINTE 0x030
EIT100LFT
EIT256LFT
EIT512LFT
ETRMSYT
ETRMBP
EDBCERR
EINPERR
EDISCARD
EITXFULL
EITXEMPTY
SV01838


REGISTER ADDRESS
31
24
23
16
15
8
7
0
ITXCTL
0x034
TAG
CHANNEL
SPD
SYNC
SY
ITXMEM
0x038
ITXM100LFT
ITXM256LFT
ITXM512LFT
ITXMF
ITXMAF
ITXM5AV
ITXME
<RESERVED>
0x03C
IRXPKCTL
0x040
RXAP_CLK
SNDIMM
DIS_TSC
RMVUAP
SPAV
EN_IRX
BPAD
EN_FS
RST_IRX
IRXHQ1
0x044
E0
F0
SID
DBS
FN
QPC
SPH
IRXHQ2
0x048
E1
F1
FMT
FDF
SYT
IRXINTACK
0x04C
SYTOVF
IR100LFT
IR256LFT
IR512LFT
IRXFULL
IRXEMPTY
FSYNC
SEQERR
CRCERR
CIPTAGFLT
RCVBP
SQOV
IRXINTE
0x050
ESYTOVF
EIR100LFT
EIR256LFT
EIR512LFT
EIRXFULL
EIRXEMPTY
EFSYNC
ESEQERR
ECRCERR
ECIPTAGFLT
ERCVBP
ESQOV
IRXCTL
0x054
SPD
TAG
CHANNEL
ERR
SYNC
SY
IRXMEM
0x058
IRXM100LFT
IRXM256LFT
IRXM512LFT
IRXMF
IRXMAF
IRXM5AV
IRXME
<RESERVED>
0x05C
<RESERVED>
0x07C
SV01839

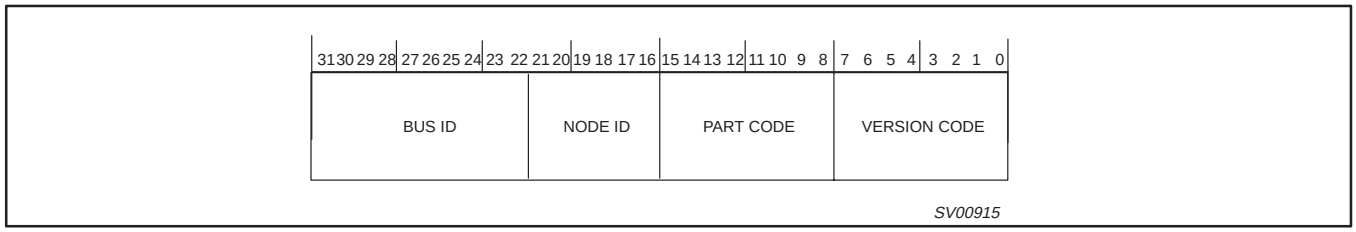

REGISTER ADDRESS
31
24
23
16
15
8
7
0
ASYCTL
0x080
DIS_BCAST
ARXRST
ATXRST
ARXALL
MAXRC
TOS
TOF
ASYMEM
0x084
TRSPQIDLE
TREQQIDLE
RRSPQF
RRSPQAF
RRSPQ5AV
RRSPQE
RREQQF
RREQQAF
RREQQ5AV
RREQQE
TRSPQF
TRSPQAF
TRSPQ5AV
TRSPQE
TREQQF
TREQQAF
TREQQ5AV
TREQQE
TX_RQ_NEXT
0x088
FIRST/MIDDLE QUADLET OF PACKET FOR TRANSMITTER REQUEST QUEUE (WRITE ONLY)
TX_RQ_LAST
0x08C
LAST QUADLET OF PACKET FOR TRANSMITTER REQUEST QUEUE (WRITE ONLY)
TX_RP_NEXT
0x090
FIRST/MIDDLE QUADLET OF PACKET FOR TRANSMITTER RESPONSE QUEUE (WRITE ONLY)
TX_RP_LAST
0x094
LAST QUADLET OF PACKET FOR TRANSMITTER RESPONSE QUEUE (WRITE ONLY)
RREQ
0x098
QUADLET OF PACKET FROM RECEIVER REQUEST QUEUE (TRANSFER REGISTER)
RRSP
0x09C
QUADLET OF PACKET FROM RECEIVER RESPONSE QUEUE (TRANSFER REGISTER)
ASYINTACK
0x0A0
RRSPQFULL
RREQQFULL
SIDQAV
RRSPQLASTQ
RREQQLASTQ
RRSPQRDERR
RREQQRDERR
RRSPQQAV
RREQQQAV
TIMEOUT
RCVDRSP
TRSPQFULL
TREQQFULL
TRSPQWRERR
TREQQWRERR
TRSPQWR
TREQQWR
ASYINTE
0x0A4
ERRSPQFULL
ERREQQFULL
ESIDQAV
ERRSPQLASTQ
ERREQQLASTQ
ERRSPQRDERR
ERREQQRDERR
ERRSPQQAV
ERREQQQAV
ETIMEOUT
ERCVDRSP
ETRSPQFULL
ETREQQFULL
ETRSPQWRERR
ETREQQWRERR
ETRSPQWR
ETREQQWR
<RESERVED>
0x0A8
0x0AC
RDI
0x0B0
SWPD
LPSTAT
EPLI
ELOA
ESCA
ESCI
PLI
LOA
SCA
SCI
SV01032


REGISTER ADDRESS
31
24
23
16
15
8
7
0
<RESERVED>
0x0B4
0x0F0
SHADOW_REG
0x0F4
byte 0
byte 1
byte 2
byte 3
0 0 0 0 1 1 1 1 0 0 0 0 1 0 1 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0
INDADDR
0x0F8
RESERVED
INDADDR
INDDATA
0x0FC
WINDOW TO THE INDIRECT QUADLET POINTED TO BY INDADDR
SV01033

13.1 Link Control Registers

13.1.1 ID Register (IDREG) – Base Address: 0x000

The ID register is automatically updated by the attached PHY with the proper Node ID after completion of the bus reset.



Reset Value 0xFFFF0301

Bit 31..22: R/W BUS ID: The 10-bit bus number that is used with the Node ID in the source address for outgoing packets and used to accept or reject incoming packets. This field reverts to all ‘1’s (0x3FF) upon bus reset.

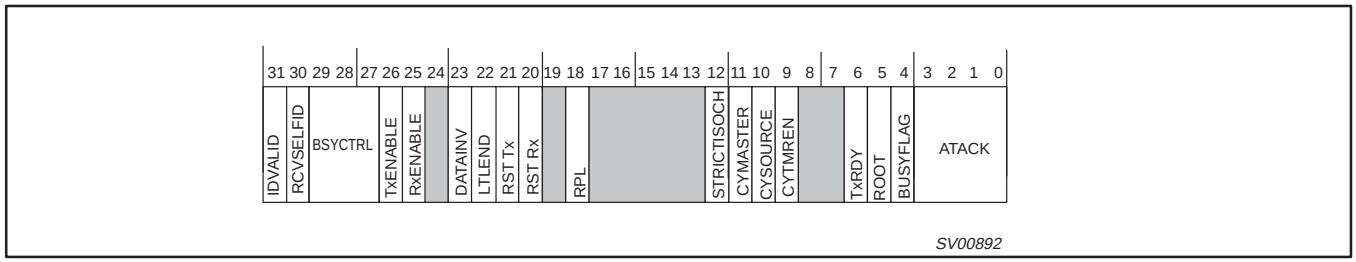
Bit 21..16: R/W NODE ID: Used in conjunction with Bus ID in the source address for outgoing packets and used to accept or reject incoming packets. This register auto-updates with the node ID assigned after the 1394 bus Tree-ID sequence.

Bit 15..8: R PART CODE: “03” designates PDI1394L40.

Bit 7..0: R VERSION CODE: “01” shows this is revision level 1 of this part.

13.1.2 General Link Control (LNKCTL) – Base Address: 0x004

The General Link control register is used to program the Link Layer isochronous transceiver, as well as the overall link transceiver. It also provides general link status.



Reset Value 0x46000002

Bit 31: R/W IDValid (IDVALID): When equal to one, the PDI1394L40 accepts the packets addressed to this node. This bit is automatically set after selfID complete and node ID is updated.

Bit 30: R/W Receive Self ID (RCVSELFID): When asserted, the self-identification packets, generated by each PHY device on the bus, during bus initialization are received and placed into the asynchronous request queue as a single packet. Bit 30 also enables the reception of PHY configuration packets in the asynchronous request queue.

Bit 29..27: R/W Busy Control (BSYCTRL): These bits control what busy status the chip returns to incoming packets. The field is defined below:

- 000 = use protocol requested by received packet (either dual phase or single phase)
- 001 = RESERVED
- 010 = RESERVED
- 011 = use single phase retry protocol
- 100 = use protocol requested in packet, always send a busy ack (for all packets)
- 101 = RESERVED
- 110 = RESERVED
- 111 = use single phase retry protocol, always send a busy ack

Bit 26: R/W Transmitter Enable (TxENABLE): When this bit is set, the link layer transmitter will arbitrate and send packets.

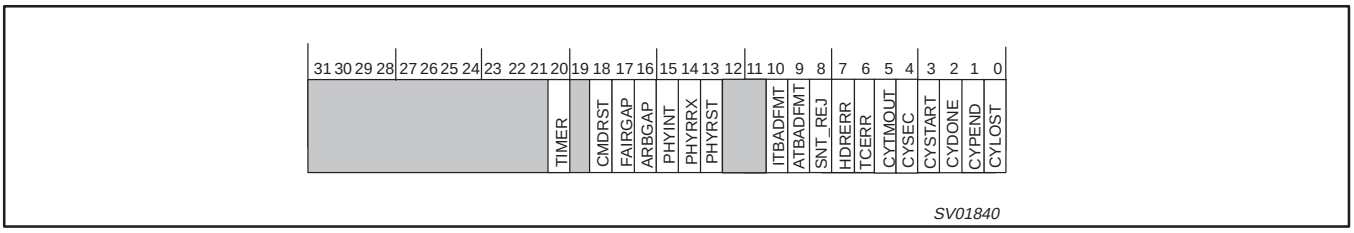
Bit 25: R/W Receiver Enable (RxENABLE): When this bit is set, the link layer receiver will receive and respond to bus packets.

Bit 23: R Data Invariant (DATAINV) refers to the byte ordering of data being presented to the Link through the host interface (HIF) port and the handling of the address and data lines by the link chip. When DATAINV = 0, the Link is in address invariant mode. When DATAINV = 1, the Link is in data invariant mode. This bit is only important if the LTLEND (Little Endian) bit is set (1), otherwise it is ignored. Interpretation of address and data information varies with the settings of these bits and with the data format being presented. See the section on Big and Little Endian Modes for more information (Section 12.5.3).

Bit 22:	R	Little Endian (LTLEND): Refers to the state of the endianess of the data and address lines connected to the ’L40. This bit reflects the state of the AV2ERR0/LTLEND pin during power reset. The state of this pin is read during reset and that state is latched into this bit position. When LTLEND = 0, the chip is set to receive BIG ENDIAN address and data on its host interface (HIF). When LTLEND = 1, the Link chip will receive LITTLE ENDIAN oriented data and address information. If this bit is set (1), the state of the DATAINV pin will also become important for determination of data positions in the internal link registers. See the section on Big and Little Endian Modes for more information (Section 12.5.3).
Bit 21:	R/W	Reset Transmitter (RSTTx): When set to one, this synchronously resets the transmitter within the link layer.
Bit 20:	R/W	Reset Receiver (RSTRx): When set to one, this synchronously resets the receiver within the link layer.
Bit 18:	R/W	Reset PHY-Link interface (RPL): Resets the PHY–Link interface in accordance with 1394a requirements. **Note:** This bit automatically resets to “0” when the interface reset operation has been completed. The PHY–Link reset operation occurs very quickly, reading this bit accurately is not usually possible. Before asserting the RPL bit, SWPD or setting the PD pin high, the user should assure that the link chip is in the following state of operation: 1) The isochronous transmit FIFO is not receiving data for transmission 2) The isochronous transmitter is disabled 3) No asynchronous packets are being generated for transmission 4) Both the ASYNC request and response queues are empty
Bit 12:	R/W	Strict Isochronous (STRICTISOCH): Used to accept or reject isochronous packets sent outside of specified isochronous cycles (between a Cycle Start and subaction gap). A ‘1’ rejects packets sent outside the specified cycles, a “0” accepts isochronous packets sent outside the specified cycle.
Bit 11:	R/W	Cycle Master (CYMASTER): When asserted and the PDI1394L40 is attached to the root PHY (ROOT bit = 1), and the cycle_count field of the cycle timer register increments, the transmitter sends a cycle-start packet. Cycle Master function will be disabled if a cycle timeout is detected (CYTMOUT bit 5 in LNKPHYINTACK). To restart the Cycle Master function in such a case, first reset CYMASTER, then set it again.
Bit 10:	R/W	Cycle Source (CYSOURCE): When asserted, the cycle_count field increments and the cycle_offset field resets for each positive transition of CYCLEIN. When deasserted, the cycle count field increments when the cycle_offset field rolls over.
Bit 9:	R/W	Cycle Timer Enable (CYTIMREN): When asserted, the cycle offset field increments. When deasserted, the Cycle Timer Register (0x010, CYCTM) can be used as a general read write register for Host Interface Firmware testing.
Bit 6:	R	Transmitter Ready (TxRDY): The transmitter is idle and ready.
Bit 5:	R	Root (ROOT): Indicates this device is the root on the bus. This automatically updates after the self_ID phase.
Bit 4:	R	Busy Flag (BUSYFLAG): The type of busy acknowledge which will be sent next time an acknowledge is required. 0 = Busy A, 1 = Busy B (only meaningful during a dual-phase busy/retry operation).
Bit 3..0:	R	AT acknowledge received (ATACK): The last acknowledge received by the transmitter in response to a packet sent from the transmit-FIFO interface while the ATF is selected (diagnostic purposes).

13.1.3 Link /Phy Interrupt Acknowledge (LNKPHYINTACK) – Base Address: 0x008

The Link/Phy Interrupt Acknowledge register indicates various status and error conditions in the Link and Phy which can be programmed to generate an interrupt. The interrupt enable register (LNKPHYINTE) is a mirror of this register. Acknowledgment of an interrupt is accomplished by writing a '1' to a bit in this register that is set. This action reset the bit indication to a '0'. Writing a '1' to a bit that is already "0" will have no effect on the register.



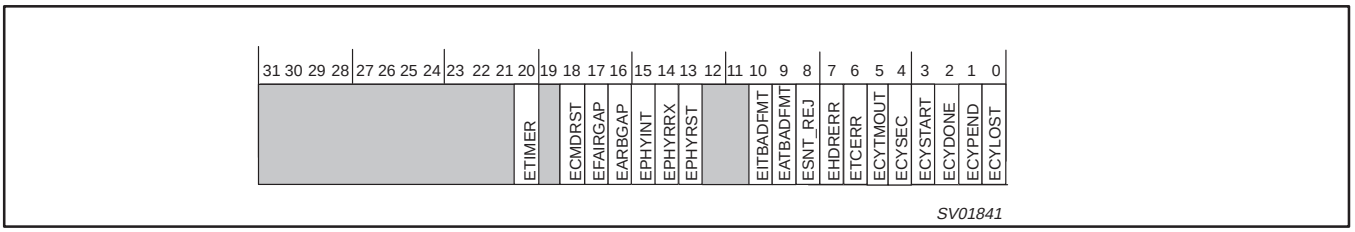
Reset Value 0x00000000

Bit 20:	R/W	Timer (TIMER): When TIMER = 1, this bit indicates that the timer has counted down to zero. This interrupt may occur only once or may occur repeatedly, according to the setting of the TMCONT bit in the TIMER register. Acknowledge this interrupt by writing a "1" back into this bit position.
Bit 18:	R/W	Command Reset Received (CMDRST): A write request to RESET-START has been received.
Bit 17:	R/W	Fair Gap (FAIRGAP): The serial bus has been idle for a fair-gap time (called subaction gap in the IEEE 1394 specification).
Bit 16:	R/W	Arbitration Reset Gap (ARBGAP): The serial bus has been idle for an arbitration reset gap.
Bit 15:	R/W	Phy Chip Int (PHYINT): The Phy chip has signaled an interrupt through the Phy interface after a bus reset or PHY reset. This bit becomes active for any of the following reasons (1) PHY has detected a loop on the bus, (2) cable power has fallen below the minimum voltage, (3) the PHY arbitration state machine has timed-out usually indicative of a bus loop, (4) a bus cable has been disconnected. Typically, recognition and notification of any of the above events by the PHY requires between 166 and 500 microseconds; therefore, this bit is not instantaneously set.
Bit 14:	R/W	Phy Register Information Received (PHYRRX): A register has been transferred by the Physical Layer device into the Link.
Bit 13:	R/W	Phy Reset Started (PHYRST): A Phy-layer reconfiguration has started. This interrupt clears the ID valid bit. (Called Bus Reset in the IEEE 1394 specification). The Async queues will be flushed during a bus reset.
Bit 10:	R/W	Isochronous Transmitter is Stuck (ITBADFMT): The transmitter has detected invalid data at the transmit-FIFO interface when the Isochronous Transmit FIFO is selected. Reset the isochronous transmitter to clear.
Bit 9:	R/W	Asynchronous Transmitter is Stuck (ATBADFMT): The transmitter expected start of new async packet in queue, but found other data (out of sync with user). Reset the asynchronous transmitter to clear.
Bit 8:	R/W	Busy Acknowledge Sent by Receiver (SNT_REJ): The receiver was forced to send a busy acknowledge to a packet addressed to this node because the receiver response/request FIFO overflowed.
Bit 7:	R/W	Header Error (HDRERR): The receiver detected a header CRC error on an incoming packet that may have been addressed to this node.
Bit 6:	R/W	Transaction Code Error (TCERR): The transmitter detected an invalid transaction code in the data at the transmit FIFO interface.
Bit 5:	R/W	Cycle Timed Out (CYTMOUT): ISOCH cycle lasted more than 125µs from Cycle-Start to Fair Gap: Disables cycle master function
Bit 4:	R/W	Cycle Second incremented (CYSEC): The cycle second field in the cycle-timer register incremented. This occurs approximately every second when the cycle timer is enabled.
Bit 3:	R/W	Cycle Started (CYSTART): The transmitter has sent or the receiver has received a cycle start packet.
Bit 2:	R/W	Cycle Done (CYDONE): A fair gap has been detected on the bus after the transmission or reception of a cycle start packet. This indicates that the isochronous cycle is over; Note: Writing a value of '0' to the bit has no effect.
Bit 1:	R/W	Cycle Pending (CYPEND): Cycle pending is asserted when cycle timer offset is set to zero (rolled over or reset) and stays asserted until the isochronous cycle has ended.
Bit 0:	R/W	Cycle Lost (CYLOST): The cycle timer has rolled over twice without the reception of a cycle start packet. This only occurs when cycle master is not asserted.

13.1.4 Link / Phy Interrupt Enable (LNKPHYINTE) – Base Address: 0x00C

This register is a mirror of the Link/Phy Interrupt Acknowledge (LNKPHYINTACK) register. Enabling an interrupt is accomplished by writing a '1' to the bit corresponding to the interrupt desired.

This register enables the interrupts described in the Link /Phy Interrupt Acknowledge register (LNKPHYINTACK) description. A one in any of the bits enables that function to create an interrupt. A zero disables the interrupt, however the status is readable in the Link /Phy Interrupt Acknowledge register.

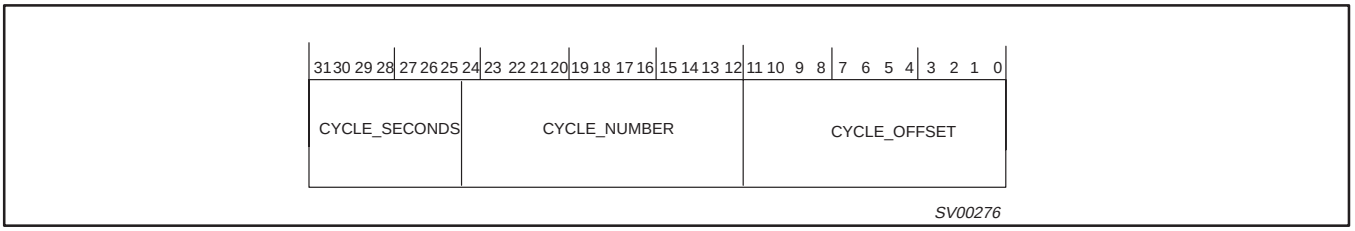


Reset Value 0x00000000

Bits 21..0 are interrupt enable bits for the Link/Phy Interrupt Acknowledge (LNKPHYINTACK).

13.1.5 Cycle Timer Register (CYCTM) – Base Address: 0x010

Cycle Timer Register operation is controlled by the Cycle Timer Enable (CYTMREN) bit in the Link Control Register (LNKCTL, 0x004). If the Cycle Timer Register is disabled, it can be used as a general read write register for Host Interface Firmware testing.

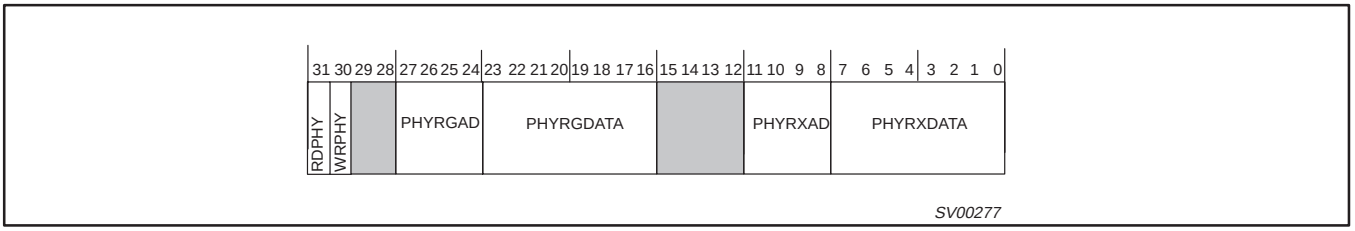


Reset Value 0x00000000

Bit 31..25:	R/W	Seconds count: 1-Hz cycle timer counter.
Bit 24..12:	R/W	Cycle Number: 8kHz cycle timer counter.
Bit 11..0:	R/W	Cycle Offset: 24.576MHz cycle timer counter.

13.1.6 Phy Register Access (PHYACS) – Base Address: 0x014

This register provides access to the internal registers on the Phy. There are special considerations when reading or writing to this register. When reading a PHY register, the address of the register is written to the PHYRGAD field with the RDPHY bit set. The PHY data will be valid when the PHYRRX bit (LNKPHYINTACK register bit 14) is set. Once this happens the register data is available in the PHYRXDATA, the address of the register just read is also available in the PHYRXAD fields. When writing a Phy register, the address of the register to be written is set in the PHYRGAD field and the data to be written to the register is set in PHYRGDATA, along with the WRPHY bit being set. Once the write is complete, the WRPHY bit will be cleared. Do not write a new Read/Write command until the previous one has been completed. After the Self-ID phase, PHY register 0 will be read automatically.



Reset Value 0x00000000

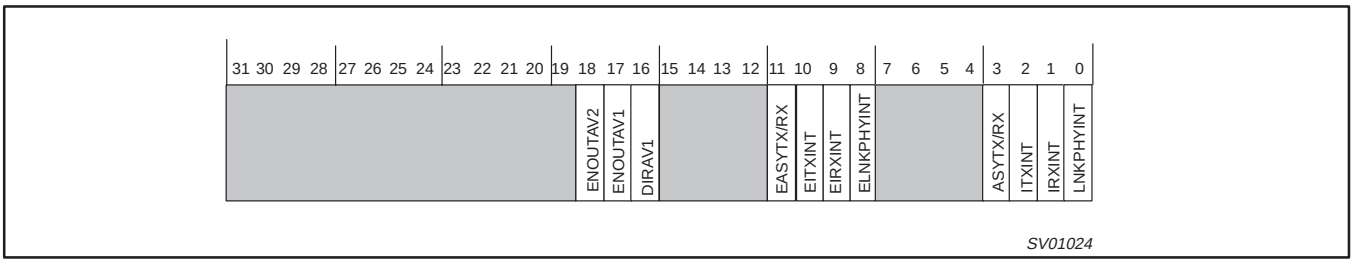
Bit 31:	R/W	Read Phy Chip Register (RDPHY): When asserted, the PDI1394L40 sends a read register request with address equal to Phy Rg Ad to the Phy interface. This bit is cleared when the request is sent.
Bit 30:	R/W	Write Phy Chip Register (WRPHY): When asserted, the PDI1394L40 sends a write register request with address equal to Phy Rg Ad to the Phy interface. This bit is cleared when the request is sent.
Bit 27..24:	R/W	Phy Chip Register Address (PHYRGAD): This is the address of the Phy-chip register that is to be accessed.
Bit 23..16:	R/W	Phy Chip Register Data (PHYRGDATA): This is the data to be written to the Phy-chip register indicated in Phy Rg Ad.
Bit 11..8:	R	Phy Chip Register Received Address (PHYRXAD): Address of register from which Phy Rx Data came.
Bit 7..0:	R	Phy Chip Register Received Data (PHYRXDATA): Data from register addressed by Phy Rx Ad.

13.1.7 Global Interrupt Status and TX Control (GLOBCSR) – Base Address: 0x018

This register is the top level interrupt status register. If the external interrupt line is set, this register will indicate which major portion of the AV Link generated the interrupt. There is no interrupt acknowledge required at this level. These bits auto clear when the interrupts in the appropriate section of the device are cleared or disabled. Control of the AV transceiver is also provided by this register.

Bits 0 to 3 are used to identify which internal modules are currently generating an interrupt. After identifying the module, the appropriate register in that module must be read to determine the exact cause of the interrupt.

A timer is available to aid the implementation of higher level protocols such as AV/C and HAVi. The timer can be started and stopped, and automatically reloads with 1s (TIMLOAD = 1) or 100ms (TIMLOAD = 0). When the set time has expired, an interrupt will be generated through TIMER (Bit 20, LNKPHYINTACK 0x008). In normal timer mode (TIMMODE = 0), the timer will generate an interrupt, reload and restart every time it expires, until TIMRNSTP is cleared. In bus reset timer mode (TIMMODE = 1), even when already running the timer will reload with 1s and restart automatically after a bus reset. If another bus reset occurs before the timer expires, the timer will again reload and restart. No interrupt will be generated until the timer expires.



NOTES

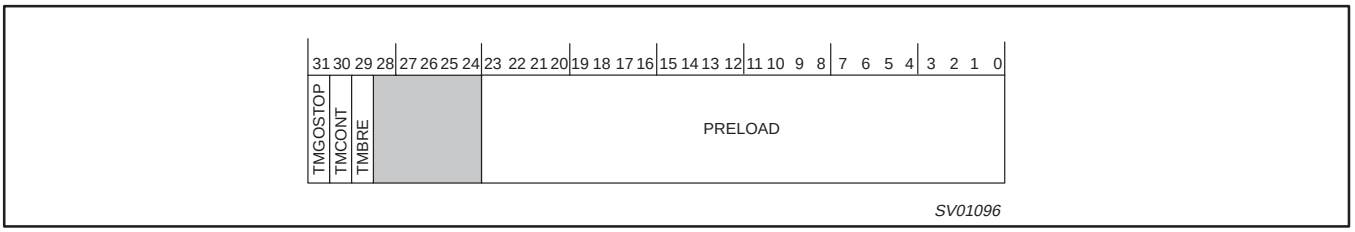
1. There can be more than one interrupt source active at the same time.
2. The HIF INT_N signal (pin 28) remains active as long as there is at least one more enabled active interrupt status bit.

Reset Value 0x00010000

Bit 18:	R/W	Enable output AVPORT2: A ‘1’ enables AVPORT2 as an output. A ‘0’ sets the 3-State condition on the port. In 3-State condition the port may be used as an input or unused output according to the state of DIRAV1 (bit 16).
Bit 17:	R/W	Enable output AVPORT1: A ‘1’ enables AVPORT1 as an output. A ‘0’ sets the 3-State condition on the port. In 3-State condition the port may be used as an input or unused output according to the state of DIRAV1 (bit 16).

Bit 16:	R/W	Direction of AVPORT1 (DIRAV1): A ‘1’ enables AVPORT1 as a transmitter, thus AVPORT1 pins are inputs. A ‘0’ configures AVPORT1 as a receiver, AVPORT1 pins are outputs in this configuration. The configuration of AVPORT2 pins is opposite of AVPORT1 pins. When AVPORT1 is set to transmit, AVPORT2 receives and vice versa.
Bit 11:	R/W	Enables generation of external interrupt by asynchronous transmitter and receiver module (ASYTX/RX, bit 3) when set (1). Disables such interrupts when clear (0) (regardless of ASYINTE contents).
Bit 10:	R/W	Enables generation of external interrupt by the isochronous transmitter module (ITXINT, bit 2) when set (1). Disables such interrupts when clear (0) (regardless of ITXINTE contents).
Bit 9:	R/W	Enables generation of external interrupt by the isochronous receiver module (IRXINT, bit 1) when set (1). Disables such interrupts when clear (0) (regardless of IRXINTE contents).
Bit 8:	R/W	Enables generation of external interrupt by general link/phy module (LKPHYINT, bit 0) when set (1). Disables such interrupts when clear (0) (regardless of LNKPHYINTE contents).
Bit 3:	R	Asynchronous Transmitter/Receiver Interrupt (ASYITX/RX): Interrupt source is in the Asynchronous Transmitter/ Receiver Interrupt Acknowledge/Source register.
Bit 2:	R	AV Transmitter Interrupt (ITXINT): Interrupt source is in the AV Transmitter Interrupt Acknowledge/Source register.
Bit 1:	R	AV Receiver Interrupt (IRXINT): Interrupt source is in the AV Receiver Interrupt Acknowledge/Source register.
Bit 0:	R	Link-Phy Interrupt (LNKPHYINT): Interrupt source is in the Link Phy Interrupt Acknowledge register.

13.1.8 Timer (TIMER) – Base Address: 0x01C



Reset Value

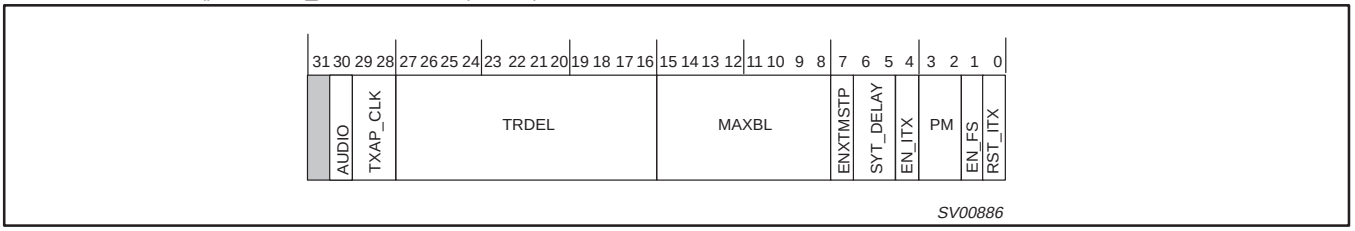
Bit 31:	R/W	TMGOSTOP: Timer Go/Stop, when = 1 start timer; when = 0 stop timer.
Bit 30:	R/W	TMCONT: Timer Continuous, when = 1 continuously operate timer; when = 0 operate timer for one timing cycle, then stop.
Bit 29:	R/W	TMBRE: Timer Bus Reset Enable, when = 1, start the timer at the beginning of a bus reset; when = 0 start the timer from the TMGOSTOP bit setting.
Bit 23..0:	R/W	Timer preload bits. Load a number into the timer preload bits with the most significant bit in the higher numbered bit position; the least significant bit in the timer preload register is bit 0. The basic timing unit is 1/(2*CLK25) or 80.14 nanoseconds. The maximum timer time-out is about 1.34 seconds ((2^24)–1 units). The timer uses the preload value inputted by the host into bits 0 through 23 of this register. The preload value is placed in the actual timer/counter (invisible to outside world) and this value is decremented by 1 for each unit of time. The timer eventually counts down to zero and then it sets the TIMER interrupt flag bit in register 0x008, LINKPHYINTACK (assuming the interrupt was enabled by the ETIMER bit). Depending on the setting of the TMCONT bit in this register, the timer preload value may be automatically reloaded into the timer/counter (when TMCONT = 1) with the timing cycle automatically re-starting, or the timer will simply interrupt and stop (when TMCONT bit = 0). TMBRE adds a mode to the timer operation which starts the timing automatically at the start of a 1394 bus reset. When TMBRE is set (1), the TMGOSTOP bit function is disabled; the TMCONT bit function is still available. **NOTE:** When TMCONT = 1, failing to acknowledge a TIMER interrupt has no effect on the starting/restarting of the timer; if an interrupt is not acknowledged (bit reset), the timer will continue to time out and restart.

13.2 AV (Isochronous) Transmitter and Receiver Registers

13.2.1 Isochronous Transmit Packing Control and Status (ITXPKCTL) – Base Address: 0x020

This register allows the user to set up the appropriate AV packets from data entered into the AV interface. The packing and control parameters (TRDEL, MAXBL, DBS, FN, QPC, and SPH) should never be changed while the transmitter is operating. The only exception to this is the MAXBL parameter when in MPEG-2 packing mode.

NOTE: When reset of isochronous transmitter is necessary, first disable the transmitter (place bit 4, EN_ITX, LOW), wait for FIFO to empty, then reset the transmitter (place RST_ITX, bit 0, HIGH). This procedure will ensure that data in the FIFO is transmitted before reset.



Reset Value 0x00000001

Bit 30: R/W AUDIO mode bit: When = 1, SYT system is in AUDIO mode. When AUDIO = 0 normal SYT time stamping operation is assumed. With AUDIO = 1, the SYT time stamp for an FSYNC pulse will NOT be appended to an empty bus packet. Any pending SYT stamp will be held until the next non-empty bus packet is sent. As an FSYNC pulse is input to the transmitting node's link chip, an SYT stamp will be made. This SYT stamp will point to a time in the future dictated by the SYT DELAY value (in register 0x020) added to the current least significant nibble (lsn) of the cycle number, plus the current cycle offset value. This mode automatically increases SYT_DELAY value by two additional cycles beyond the value programmed in the SYT_DELAY bits.

Bit 29..28: R/W TXAP_CLK: Application Clock, default mode, '00' the AVxCLK pin is an input. This pin can become an application clock for the isochronous Transmitter (and output) by programming it to '01', '10', or '11'.

The programming values are:

00 Input
01 24.576MHz
10 12.288MHz
11 6.144MHz

Note that when enabled as '01', '10', or '11', the AV port that is configured as transmitter and enabled will output this clock signal on its AVxCLK pin.

Bit 27..16: R/W TRDEL: Transport delay. Value added to cycle timer to produce time stamps. Lower 4 bits add to upper 4 bits of cycle_offset, (Cycle Timer Register, CYCTM). Remainder adds to cycle_count field.

Bit 15..8: R/W MAXBL: The (maximum) number of data blocks to be put in a payload.

Bit 7: R/W ENXTMSTP: Enable External time stamp control. Allows an external time stamp (generated by the application) to be inserted in place of the link-generated time stamp. Defaults to link generated time stamp. The application must present the first byte of a quadlet-wide time stamp accompanied by the AVSYNC pulse (and AVVALID) to the AVPORT. The external time stamp quadlet is inputted first, followed by the application data packet. The transmitted packet size is now one quadlet larger than the original isochronous data packet—Set up the isochronous transmitter accordingly with SPH = 1. **CAUTION**: Unless valid IEC 61883 time stamp format (based on the link cycle timer) is used, the receiving node link chip must be equipped with a time stamp check disabling function similar to the DIS_TSC bit (register 0x040, Bit 7). Please see section 13.2.8 for details.

Bit 6..5: R/W SYT_DELAY: Programmable delay of AV1FSYNC and AV2FSYNC. Each cycle is 1 bus cycle, 125 μs.
Reset value is "00", a 3 cycle delay.

01 = 2 cycles
00 = 3 cycles
10 = 4 cycles
11 = Reserved

Bit 4: R/W EN_ITX: Enable receipt of new application packets and generation of isochronous bus packets in every cycle. This bit also enables the Link Layer to arbitrate for the transmitter in each subsequent bus cycle. When this bit is disabled (0), the current packet will be transmitted and then the transmitter will shut down.

Bit 3..2: R/W PM: packing mode:

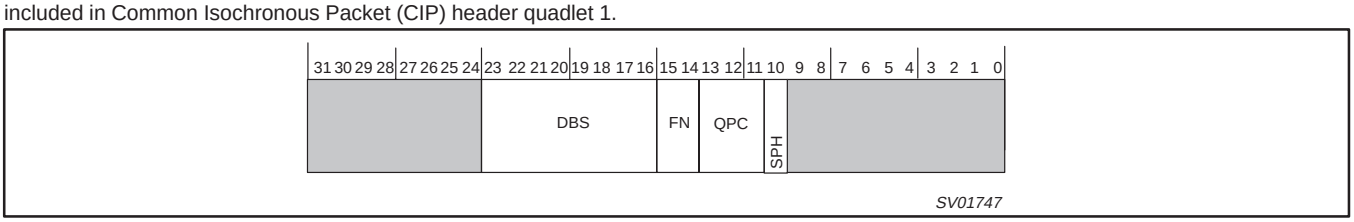
00 = variable sized bus packets, most generic mode.
01 = fixed size bus packets.
10 = MPEG–2 packing mode.
11 = No data, just CIP headers are transmitted.

Bit 1: R/W EN_FS:enable generation/insertion of SYT stamps (Time Stamps) in CIP header.

Bit 0: R/W Reset Isochronous Transmitter (RST_ITX): causes transmitter to be reset when '1'. In order for synchronous reset of ITX to work properly, an AVxCLK (from either the internal or external source) must be present and ensure that the reset bit is kept (programmed) HIGH for at least the duration of one AVxCLK period. Failure to do so may cause the application interface of this module to be improperly reset (or not reset at all). When reset is enabled, all bytes will be flushed from the FIFO and transmission will cease immediately.

13.2.2 Common Isochronous Transmit Packet Header Quadlet 1 (ITXHQ1) – Base Address: 0x024

The AV Transmit Packing Control register holds the specification for the packing scheme used on the AV data stream. This information is included in Common Isochronous Packet (CIP) header quadlet 1.



Reset Value 0x00000000

Bit 16..23: R/W DBS: Size of the data blocks from which AV payload is constructed. The value 0 represents a length of 256 quadlets.

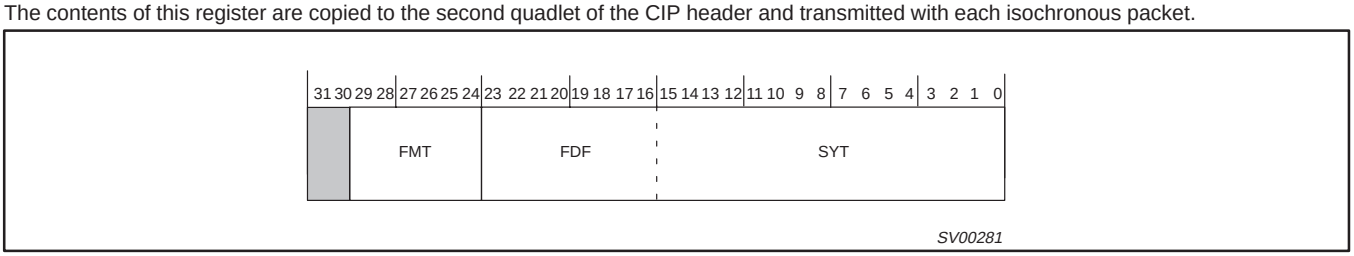
Bit 14..15: R/W FN: (Fraction Number) The encoding for the number of data blocks into which each source packet shall be divided (00 = 1, 01 = 2, 10 = 4, 11 = 8).

Bit 11..13: R/W QPC: Number of dummy quadlets to append to each source packet before it is divided into data blocks of the specified size. The value QPC must be less than DBS and less than 2^{FN}.

Bit 10: R/W SPH: Indicates that a 25-bit CYCTM based time stamp has to be inserted before each application packet.

13.2.3 Common Isochronous Transmit Packet Header Quadlet 2 (ITXHQ2) – Base Address: 0x028

The contents of this register are copied to the second quadlet of the CIP header and transmitted with each isochronous packet.



Reset Value 0x00000000

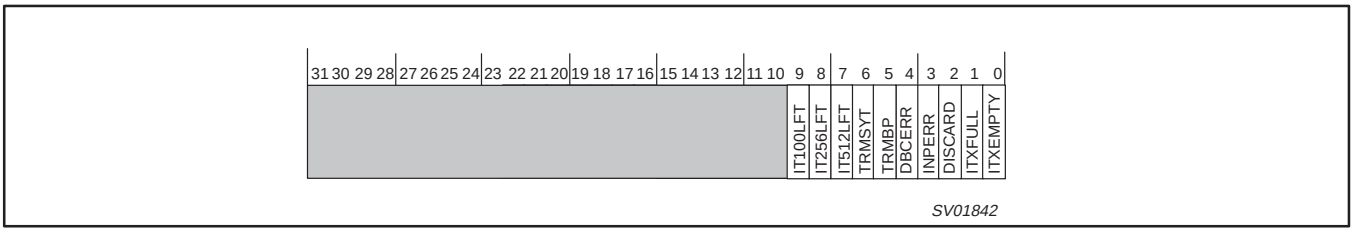
Bit 29..24: R/W FMT: Value to be inserted in the FMT field in the AV header.

Bit 23..0: R/W FDF/SYT: Value to be inserted in the FDF field. When the EN_FS bit in the Transmit Control and Status Register (ITXPKCTL) is set (=1), the lower 16 bits of this register are replaced by an SYT stamp if a rising edge on AVFSYNCIN has been detected or all ‘1’s if no such edge was detected since the previous packet. The upper 8 bits of the register are sent as they appear in the FDF register. When the EN_FS bit in the Transmit Control and Status Register is unset (=0), the full 24 bits can be set to any application specified value.

13.2.4 Isochronous Transmitter Interrupt Acknowledge (ITXINTACK) – Base Address: 0x02C

The AV Transmitter Interrupt Control and Status register is the interrupt register for the AV transmitter.

Bits 2, 3, and 4 “auto repair” themselves, i.e. AVLINK will detect the situation and attempt to recover on its own. The host controller still needs to clear these interrupts to be alerted the next time.



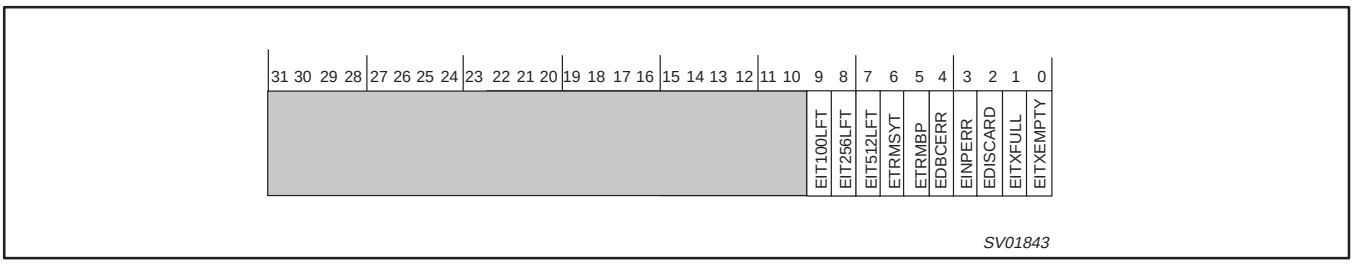
Reset Value 0x00000000

Bits 9 .. 0 are interrupt acknowledge bits; and are defined as:

Bit 9:	R/W	IT100LFT: Interrupt when transmitter queue reaches 100 quadlets from full.
Bit 8:	R/W	IT256LFT: Interrupt when transmitter queue reaches 256 quadlets from full.
Bit 7:	R/W	IT512LFT: Interrupt when transmitter queue reaches 512 quadlets from full. This bit is disabled if 0.5K Byte buffer size is set.
Bit 6:	R/W	TRMSYT: Interrupt on transmission of a SYT in CIP header quadlet 2
Bit 5:	R/W	TRMBP: Interrupt on payload transmission/discard complete.
Bit 4:	R/W	DBCERR: Acknowledge interrupt on Data Block Count (DBC) synchronization loss.
Bit 3:	R/W	INPERR: Acknowledge interrupt on input error (input data discarded).
Bit 2:	R/W	DISCARD: Interrupt on lost cycle (payload discarded).
Bit 1:	R/W	ITXFULL: Interrupt on isochronous memory bank full. This is a fatal error. The ITX transmitter will reset itself automatically when this occurs.
Bit 0:	R/W	ITXEMPTY: Interrupt on isochronous memory bank empty.
		Other bits will always read ‘0’.

13.2.5 Isochronous Transmitter Interrupt Enable (ITXINTE) – Base Address: 0x030

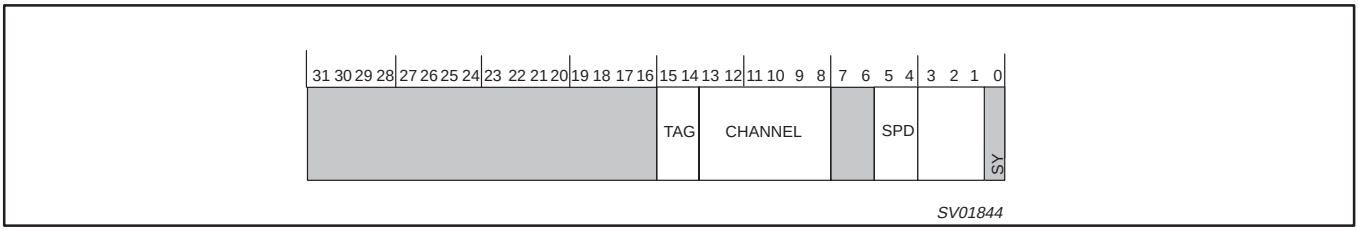
These are the enabled bits for the AV Transmitter Control.



Reset Value 0x00000000

Bits 13..0 are interrupt enable bits for the Isochronous Transmitter Interrupt Acknowledge register (ITXINTACK).

13.2.6 Isochronous Transmitter Control Register (ITXCTL) – Base Address: 0x34

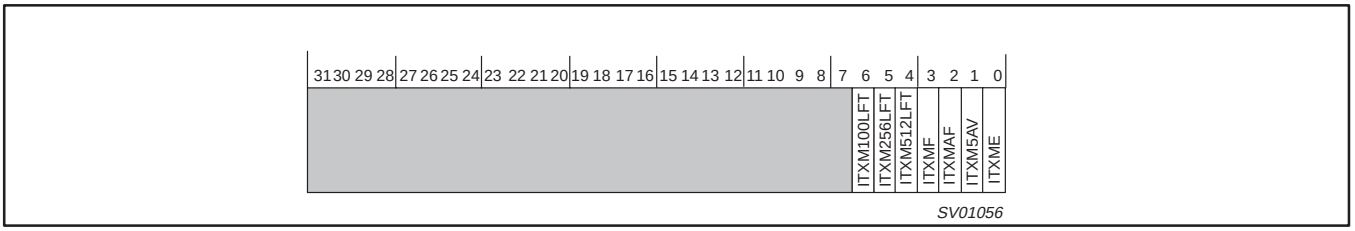


Reset Value 0x00000000

Bit 15..14:	R/W	Tag: Tag code to insert in isochronous bus packet header. Should be ‘01’ for IEC 61883 International Standard data.
Bit 13..8:	R/W	Channel: Isochronous channel number.
Bit 5..4:	R/W	Speed: Cable transmission speed (S100, S200, S400). 00 = 100Mbs 01 = 200Mbs 10 = 400Mbs 11 = reserved
Bit 0	R	SY: Sync code to insert in SY field of isochronous bus packet header. This bit reflects the value of the AVx SY pin and is synchronized with the data payload that was associated with it.

13.2.7 Isochronous Transmitter Memory Status (ITXMEM) – Base Address: 0x038

The AV Transmitter Memory Status register reports on the condition of the internal memory buffer used to store incoming AV data streams before transmission over the 1394 bus. This register is used primarily for diagnostics; several memory status flags are also available in the ITXINTACK register.

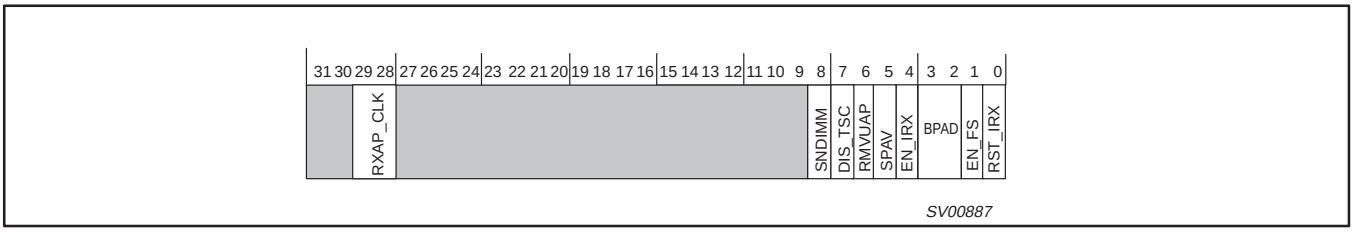


Reset Value 0x00000003

BIT 6:	R	ITXM100LFT: 100 or less quadlets of storage available.
Bit 5:	R	ITXM256LFT: Memory has 256 quadlets of space remaining before becoming full.
Bit 4:	R	ITXM512LFT: Memory has 512 quadlets of space remaining before becoming full.
Bit 3:	R	ITXMF: memory is completely full, no storage available.
Bit 2:	R	ITXMAF: almost full, exactly one quadlet of storage available.
Bit 1:	R	ITXM5AV: at least 5 more quadlets of storage available.
Bit 0:	R	ITXME: memory bank is empty (zero quadlets stored).

13.2.8 Isochronous Receiver Unpacking Control (IRXPKCTL) – Base Address: 0x040

NOTE: When receiver reset is required, first disable receiver (EN_IRX = 0), then wait until Rx FIFO is emptied, then perform the reset. This will allow previously received packets to go to the application instead of being lost.



Reset Value 0x00000041

AV Receiver Control Bits.

Bit 29..28: R/W — RXAP_CLK: Receiver Application Clock, default mode, ‘00’ the AVxCLK pin is an input. This pin can become an application clock and output for the isochronous Receiver by programming it to ‘01’, ‘10’, or ‘11’.

The programming values are:

00 Input
01 24.576MHz
10 12.288MHz
11 6.144MHz

Note that when enabled as ‘01’, ‘10’, or ‘11’, the AV port that is configured as receiver and enabled will output this clock signal on its AVxCLK pin.

Bit 8: R/W — SNDIMM: Send immediately; when set to “1”, this bit will allow a received isochronous packet containing a CRC error to be output immediately (without regard to the time stamp value). This bit defaults to “0”. In default (reset) mode, the packet will be output with respect to the time stamp value, even if there is a CRC error.
CAUTION: If there is an error in the time stamp, the packet may be held far into the future. This will affect subsequently received packets.

Bit 7: R/W — DIS_TSC: Disable Time Stamp Checking. Defaults to “0”, time stamp checking is enabled. When time stamp checking is disabled, the time stamp accompanying a packet is output before the packet to the application for use by the application. This adds an extra quadlet of data to the received data stream; the application must be capable of handling this extra 4 bytes.

Bit 6: R/W — RMVUAP: Remove unreliable packets from memory, do not attempt delivery

Bit 5: R — SPAV: Source packet available for delivery in buffer memory.

Bit 4: R/W — EN_IRX: Enable receiver operation. Value is only checked whenever a new bus packet arrives, so enable/disable while running is ‘graceful’, meaning any transfers in process will be completed before this bit is asserted.

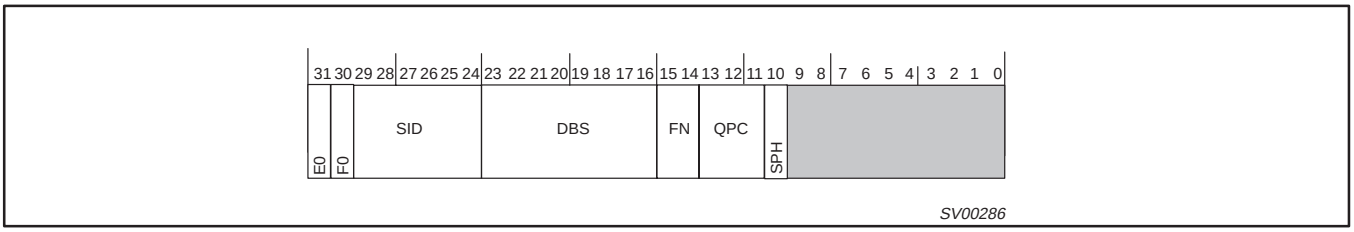
Bit 2..3: R/W — BPAD: Value indicating the amount of byte padding to be removed from the last data quadlet of each source packet, from 0 to 3 bytes. This is in addition to quadlet padding as defined in IEC 61883 International Standard.

Bit 1: R/W — EN_FS: Enable processing of SYT stamps.

Bit 0: R/W — RST_IRX: causes the receiver to be reset when ‘1’. In order for synchronous reset of IRX to work properly, the application must supply an AVCLK and ensure that the reset bit is kept (programmed) HIGH for at least the duration of one AVCLK period. Failure to do so may cause the application interface of this module to be improperly reset (or not reset at all).

13.2.9 Common Isochronous Receiver Packet Header Quadlet 1 (IRXHQ1) – Base Address: 0x044

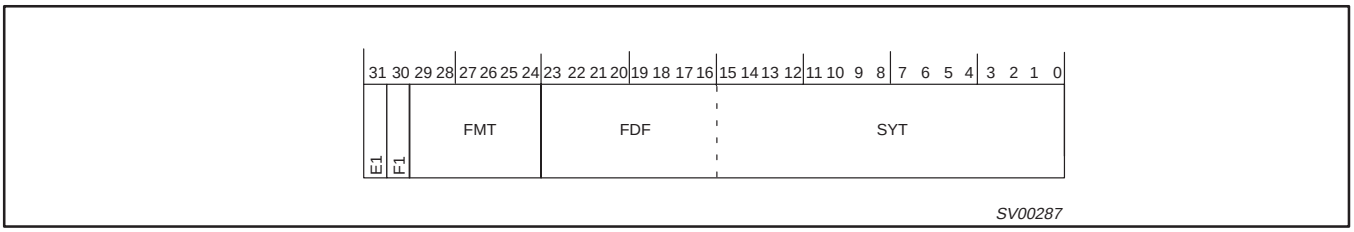
This quadlet represents the last received header value when AV receiver is operating.



Reset Value 0x00000000

Bit 31..30:	R	E0: End of Header, F0: Format: Always set to 00 for first AV header quadlet.
Bit 29..24	R	SID: Source ID, contains the node address of the sender of the isochronous data.
Bit 23.16:	R	DBS: Size of the data blocks from which AV payload is constructed. The value 0 represents a length of 256 quadlets.
Bit 15..14:	R	FN (Fraction Number): The encoding for the number of data blocks into which each source packet has been divided (00 = 1, 01 = 2, 10 = 4, 11 = 8) by the transmitter of the packet.
Bit 13..11:	R	QPC: Number of dummy quadlets appended to each source packet before it was divided into data blocks of the specified size.
Bit 10:	R	SPH: Indicates that a CYCTM based time stamp is inserted before each application packet (25 bits specified in the IEC 61883 International Standard).

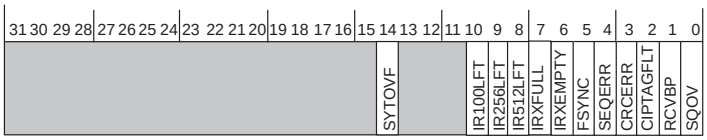
13.2.10 Common Isochronous Receiver Packet Header Quadlet 2 (IRXHQ2) – Base Address: 0x048



Reset Value 0x0000FFFF

Bit 31..30:	R	E1: End of Header, F1: Format: Should be set to 10 for second AV header quadlet.
Bit 29..24:	R	FMT: Value inserted in the Format field.
Bit 23..0:	R	FDF/SYT: If ‘‘EN FS” in Register IRXPKCTL (0x040) is set to ‘1’, then lower 16-bits are interpreted as SYT.

13.2.11 Isochronous Receiver Interrupt Acknowledge (IRXINTACK) – Base Address: 0x04C



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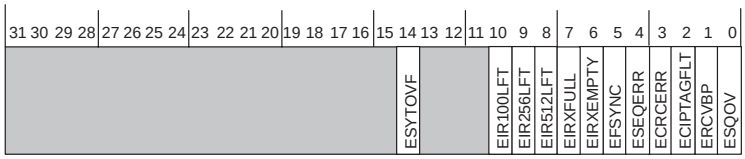
Reset Value 0x00000000

Bit 14:	R/W	SYTOVF: SYT FIFO overflow. The isochronous receiver's SYT field FIFO has overflowed and has been automatically reset and cleared. This interrupt alerts the host controller that up to 7 AVFSYNC pulses may be missing due to an SYT field reception error.
Bit 10:	R/W	IR100LFT: Interrupt when receiver queue reaches 100 quadlets from full.
Bit 9:	R/W	IR256LFT: Interrupt when receiver queue reaches 256 quadlets from full.
Bit 8:	R/W	IR512LFT: Interrupt when receiver queue reaches 512 quadlets from full. This bit is disabled if 0.5K Byte buffer size is set.
Bit 7:	R/W	IRXFULL: Isochronous data memory bank has become full. this is a fatal error, the recommended action is to reset and re-initialize the receiver.
Bit 6:	R/W	IRXEMPTY: Isochronous data memory bank has become empty.
Bit 5:	R/W	FSYNC: Pulse at fsync output.
Bit 4:	R/W	SEQERR: Sequence error of data blocks.
Bit 3:	R/W	CRCERR: CRC error in bus packet.
Bit 2:	R/W	CIPTAGFLT: Faulty CIP header tag (E,F bits). i.e.: The CIP header did not meet the standard and the whole packet is ignored.
Bit 1:	R/W	RCVBP: Bus packet processing complete.
Bit 0:	R/W	SQOV: Status queue overflow. This is a fatal error, the recommended action is to reset and re-initialize the receiver.

13.2.12 Isochronous Receiver Interrupt Enable (IRXINTE) – Base Address: 0x050

Interrupt enable bits for AV Receiver.

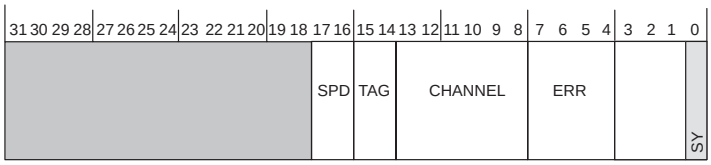


SV01847

Reset Value 0x00000000

Bit 14..0 are interrupt enable bits for the Isochronous Receiver Interrupt Acknowledge (IRXINTACK).

13.2.13 Isochronous Receiver Control Register (IRXCTL) – Base Address: 0x054



Reset Value 0x00000000

Bit 17..16: R SPD: Speed of last received isochronous packet (S100 .. S400).
- 00 = 100 Mbps
- 01 = 200 Mbps
- 10 = 400 Mbps
- 11 = Reserved

Bit 15..14: R/W TAG: Isochronous tag value (must match) for AV format, '01' for IEC 61883 International Standard data.

Bit 7..4: R ERR: Error code for last received isochronous AV packet.

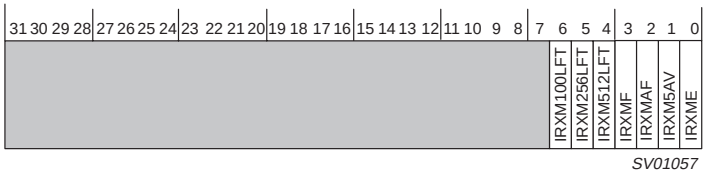
Bit 0: R SY: Sync code to insert in SY field of isochronous bus packet header. This bit reflects the value of the SY bit received from the isochronous header and is synchronized in the receiver FIFO with the data payload that was associated with it. **Note:** The SY value at the AV port may differ due to aging as it progresses through the IRx FIFO.

Table 7. Error Codes

Code	Name	Meaning
0000	reserved	
0001	complete	The node has successfully accepted the packet. If the packet was a request subaction, the destination node has successfully completed the transaction and no response subaction shall follow.
0010 through 1100	reserved	
1101	data_error	The node could not accept the block packet because the data field failed the CRC check, or because the length of the data block payload did not match the length contained in the dataLength field. this code shall not be returned for any packet that does not have a data block payload.
1110 and 1111	reserved	

13.2.14 Isochronous Receiver Memory Status (IRXMEM) – Base Address: 0x058

The AV Receiver Memory Status register reports on the condition of the internal memory buffer used to store outgoing AV data streams after reception from the 1394 bus. This register is used primarily for diagnostics; several memory flags are also available in the IRXINTACK register.



Reset Value 0x00000003

Bit 6: R IRXM100LFT: FIFO is 100 quadlets from full.

Bit 5: R IRXM256LFT: FIFO is 256 quadlets from full.

Bit 4: R IRXM512LFT: FIFO is 512 quadlets from full.

Bit 3: R IRXMF: Full: no space available.

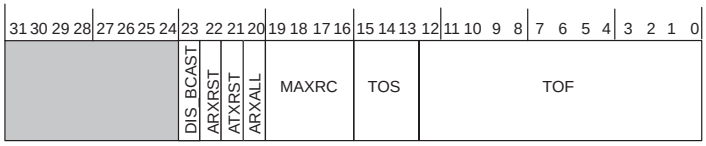
Bit 2: R IRXMAF: Almost full: exactly one quadlet of storage available.

Bit 1: R IRXM5AV: At least 5 more quadlets of storage available.

Bit 0: R RXME: Memory bank is empty (no data committed).

13.3 Asynchronous Control and Status Interface

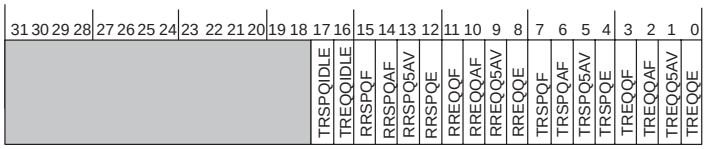
13.3.1 Asynchronous RX/TX Control (ASYCTL) – Base Address: 0x080



Reset Value 0x00300320

Bit 23:	R/W	DIS_BCAST: Disable the reception of broadcast packets (async packets address to 0x3F).
Bit 22:	R/W	ARXRST: Asynchronous receiver reset. This bit will auto clear when the link layer state machine is idle.
Bit 21:	R/W	ATXRST: Asynchronous transmitter reset. the power-up reset value of this bit is “0”, however, after every bus reset this bit is set (1). this effectively disables the asynchronous transmitter; re-enable the async transmitter by clearing this bit after each bus reset, especially if asynchronous transmission is to be used.
Bit 20:	R/W	ARXALL: Receive and filter only RESPONSE packets. When set (1), all responses are stored. When clear (0), only solicited responses are stored.
Bit 19..16:	R/W	MAXRC: Maximum number of asynchronous transmitter single phase retries
Bit 15..13:	R/W	TOS: Time out seconds, integer of 1 second
Bit 12..0:	R/W	TOF: Time out fractions, integer of 1/8000 second. Resets to 0320h, which is 100 milliseconds.

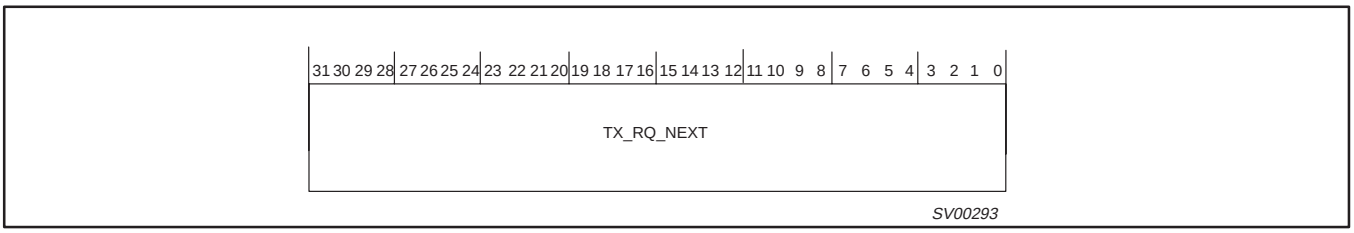
13.3.2 Asynchronous RX/TX Memory Status (ASYMEM) – Base Address: 0x084



Reset Value 0x00033333

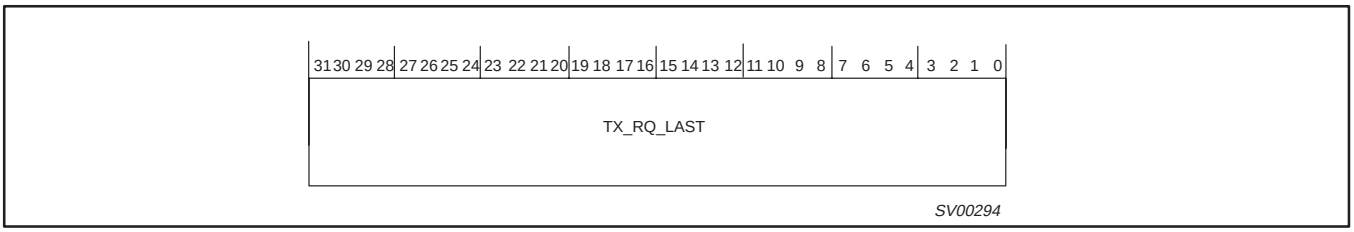
		Unused bits read ‘0’. The information in this register is primarily used for diagnostics.
Bit 17:	R	TRSPQIDLE: Transmitter response queue is idle. Indicates that the transfer register for this queue is empty.
Bit 16:	R	TREQQIDLE: Transmitter request queue is idle. Indicates that the transfer register for this queue is empty.
Bit 15:	R	RRSPQF: Receiver response queue full.
Bit 14:	R	RRSPQAF: Receiver response queue almost full (precisely 1 more quadlet available).
Bit 13:	R	RRSPQ5AV: Receiver response queue at least 5 quadlets available.
Bit 12:	R	RRSPQE: Receiver response queue empty.
Bit 11:	R	RREQQF: Receiver request queue full.
Bit 10:	R	RREQQAF: Receiver request queue almost full (precisely 1 more quadlet available).
Bit 9:	R	RREQQ5AV: Receiver request queue at least 5 quadlets available.
Bit 8:	R	RREQQE: Receiver request queue empty.
Bit 7:	R	TRSPQF: Transmitter response queue full.
Bit 6:	R	TRSPQAF: Transmitter response queue almost full (precisely 1 more quadlet available).
Bit 5:	R	TRSPQ5AV: Transmitter response queue at least 5 quadlets available.
Bit 4:	R	TRSPQE: Transmitter response queue empty.
Bit 3:	R	TREQQF: Transmitter request queue full.
Bit 2:	R	TREQQAF: Transmitter request queue almost full (precisely 1 more quadlet available).
Bit 1:	R	TREQQ5AV: Transmitter request queue at least 5 quadlets available.
Bit 0:	R	TREQQE: Transmitter request queue empty.

13.3.3 Asynchronous Transmit Request Next (TX_RQ_NEXT) – Base Address: 0x088



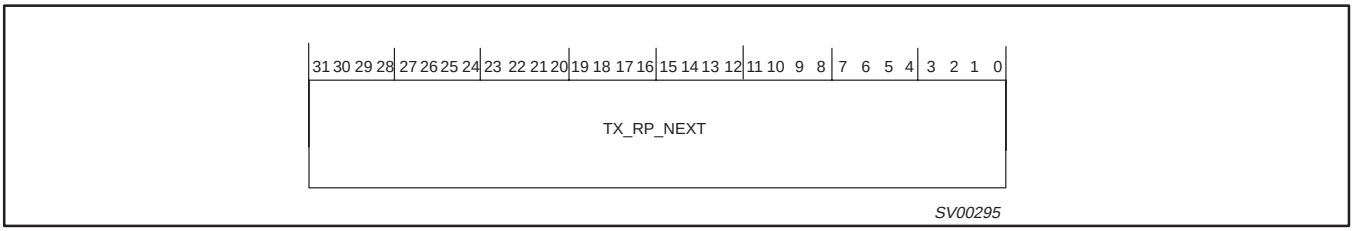
Bit 31..0: W TX_RQ_NEXT: First/middle quadlet of packet for transmitter request queue (write only).
Writing this register will clear the TREQQWR flag until the quadlet has been written to its queue.

13.3.4 Asynchronous Transmit Request Last (TX_RQ_LAST) – Base Address: 0x08C



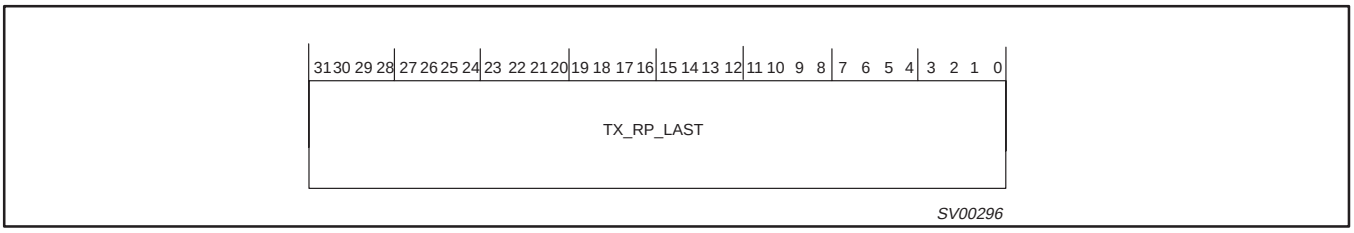
Bit 31..0: W TX_RQ_LAST: Last quadlet of packet for transmitter request queue (write only).
Writing this register will clear the TREQQWR flag until the quadlet has been written to its queue.

13.3.5 Asynchronous Transmit Response Next (TX_RP_NEXT) – Base Address: 0x090



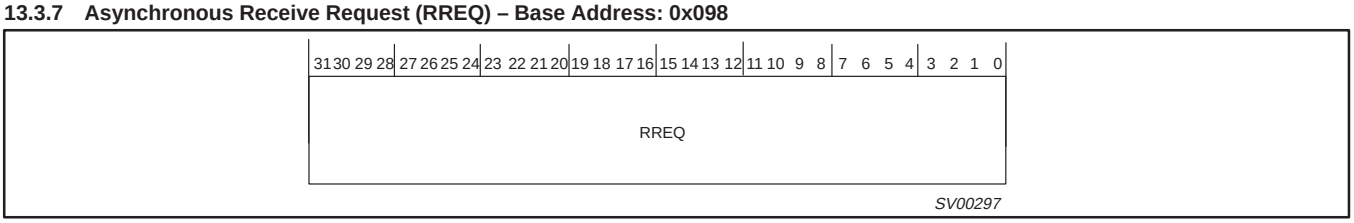
Bit 31..0: W TX_RP_NEXT: First/middle quadlet of packet for transmitter response queue (write only).
Writing this register will clear the TRSPQWR flag until the quadlet has been written to its queue.

13.3.6 Asynchronous Transmit Response Last (TX_RP_LAST) – Base Address: 0x094



Bit 31..0: W TX_RP_LAST: Last quadlet of packet for transmitter response queue (write only).
Writing this register will clear the TRSPQWR flag until the quadlet has been written to its queue.

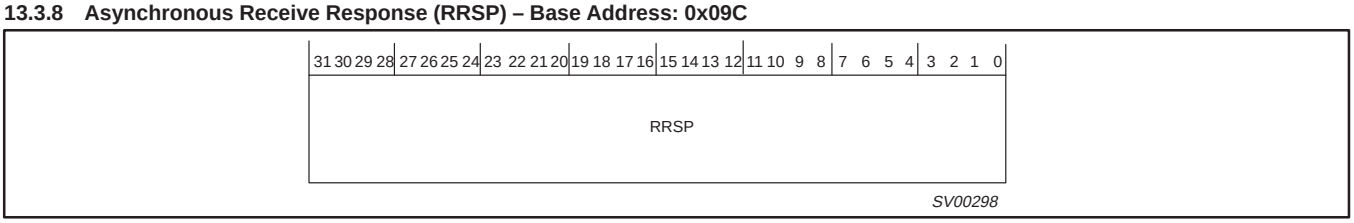
13.3.7 Asynchronous Receive Request (RREQ) – Base Address: 0x098



Reset Value 0x00000000

Bit 31..0: R RREQ:Quadlet of packet from receiver request queue (transfer register).
Reading this register will clear the RREQQQAV flag until the next received quadlet is available for reading.

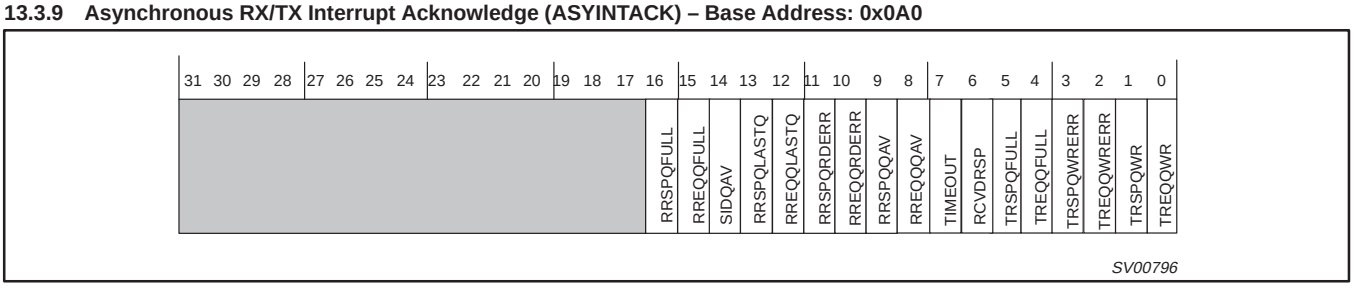
13.3.8 Asynchronous Receive Response (RRSP) – Base Address: 0x09C



Reset Value 0x00000000

Bit 31..0: R RRSP:Quadlet of packet from receiver response queue (transfer register).
Reading this register will clear the RRSPQQAV flag until the next received quadlet is available for reading.

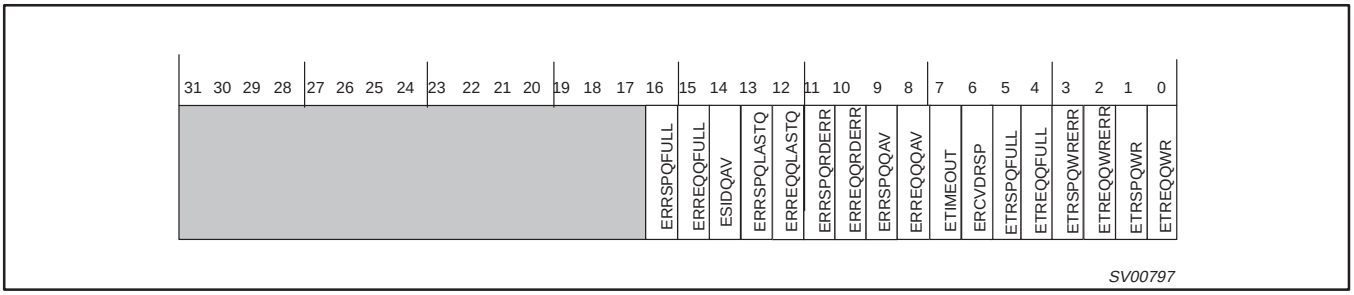
13.3.9 Asynchronous RX/TX Interrupt Acknowledge (ASYINTACK) – Base Address: 0x0A0



Reset Value 0x00000C00

Bit 31..17:	R/W	Unused bits read ‘0’
Bit 16:	R/W	RRSPQFULL: Receiver response queue did become full. Write a “1” to this bit to reset the interrupt.
Bit 15:	R/W	RREQQFULL: Receiver request queue did become full. Write a “1” to this bit to reset the interrupt.
Bit 14:	R/W	SIDQAV: Current quadlet in RREQ is selfID data. This bit is set only after a bus reset, not after reception of PHY packets other than self IDs. This interrupt automatically resets when the quadlet is read.
Bit 13:	R/W	RRSPQLASTQ: Current quadlet in RRSP is last quadlet of packet. This interrupt automatically resets when the quadlet is read.
Bit 12:	R/W	RREQQLASTQ: Current quadlet in RREQ is last quadlet of packet. This interrupt automatically resets when the quadlet is read.
Bit 11:	R/W	RRSPQRDERR: Receiver response queue read error (transfer error) or bus reset occurred. When set (1), this queue is blocked for read access. Write a “1” to this bit to reset the interrupt.
Bit 10:	R/W	RREQQRDERR: Receiver request queue read error (transfer error) or bus reset occurred. When set (1), this queue is blocked for read access. Write a “1” to this bit to reset the interrupt.
Bit 9:	R/W	RRSPQQAV: Receiver response queue quadlet available (in RRSP). This interrupt automatically resets when the quadlet is read.
Bit 8:	R/W	RREQQQAV: Receiver request queue quadlet available (in RREQ). This interrupt automatically resets when the quadlet is read.
Bit 7:	R/W	TIMEOUT: Split transaction response timeout. Write a “1” to this bit to reset the interrupt.
Bit 6:	R/W	RCVDRSP: Solicited response received (within timeout interval). Write a “1” to this bit to reset the interrupt.
Bit 5:	R/W	TRSPQFULL: Transmitter response queue did become full. Write a “1” to this bit to reset the interrupt.
Bit 4:	R/W	TREQQFULL: Transmitter request queue did become full. Write a “1” to this bit to reset the interrupt.
Bit 3:	R/W	TRSPQWRERR: Transmitter response queue write error (transfer error). Write a “1” to this bit to reset the interrupt.
Bit 2:	R/W	TREQQWRERR: Transmitter request queue write error (transfer error). Write a “1” to this bit to reset the interrupt.
Bit 1:	R/W	TRSPQWR: Transmitter response queue written (transfer register emptied). Write a “1” to this bit to reset the interrupt.
Bit 0:	R/W	TREQQWR: Transmitter request queue written (transfer register emptied). Write a “1” to this bit to reset the interrupt.

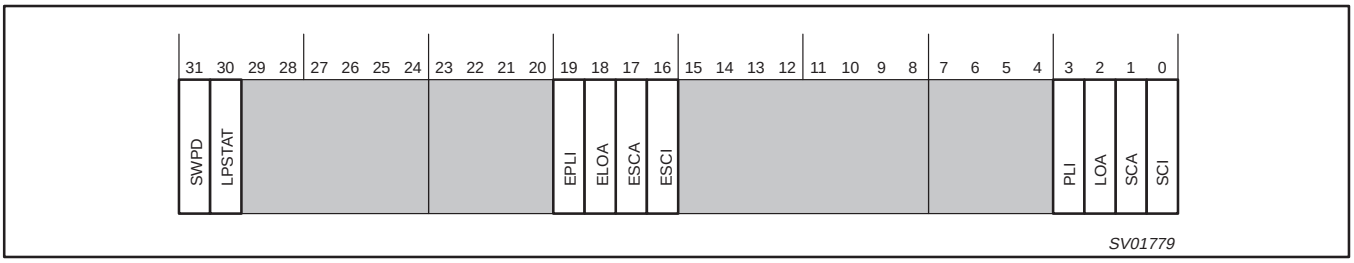
13.3.10 Asynchronous RX/TX Interrupt Enable (ASYINTE) – Base Address: 0x0A4



Reset Value 0x00000000

Bits16..0 are interrupt enable bits for the Asynchronous RX/TX Interrupt Acknowledge (ASYINTACK).

13.3.11 RDI Register – Base Address: 0x0B0



NOTE:

1. Also refer to Section 12.5.3 for functional descriptions.

Reset Value 0x00000000

Note: Before asserting the RPL bit, SWPD or setting the PD pin high, the user should assure that the link chip is in the following state of operation:

1) The isochronous transmit FIFO is not receiving data for transmission

2) The isochronous transmitter is disabled

3) No asynchronous packets are being generated for transmission

4) Both the ASYNC request and response queues are empty

Bit 31: R/W SWPD: Software power–down. Writing a 1 to this register bit will cause the link to de–activate its LPS pin causing the PHY to turn off the SCLK to the link. This, in turn, causes the link chip to go into a low power mode in which only the RDI register is accessible. The function of this bit is identical to that of the hardware pin "PD". When PD is set (1), SWPD will be set automatically by the pin state and will cause entry into the power down mode as stated above. DO NOT USE BOTH (HARDWARE AND SOFTWARE) MODES OF OPERATION TO CAUSE THE POWER DOWN FUNCTION. Use either hardware mode (the PD pin) OR the software method (setting / resetting the SWPD bit), not both. The PD pin will take precedence over the software method... the link will not come out of PD mode unless the PD pin is de–asserted (0). An unused PD pin should be connected to the link chip ground. The SWPD bit *does not* indicate the status of the PD pin. See Section 12.5.3 for more information.

Bit 30: R LPSTAT: Link – PHY interface status. This bit reflects the status of the LPS signal. When the LPS signal is active (pulsing) the PHY interprets it as indicating that the link power is on and the link is requesting to be activated. The PHY, in turn, supplies the SCLK to the link, thus giving it the means to become active. The SCLK is used by the link to operate most of its internal circuitry. If LPS was active and then de–activated, it is a signal to the PHY chip that the link desires entry into the power down mode. The LPSTAT bit continually indicates the status of the LPS pin and thus the overall status of the link – PHY interface. It should also be noted here that a momentary de–activation of the LPS signal by the setting of the RPL bit (bit 18 of register 0x004, LNKCTL) to cause a link – PHY interface reset will also be indicated by the LPSTAT bit. It is suggested that this momentary status change be ignored when the host controller causes a link – PHY reset through the use of the RPL bit.

Bit 19: R/W EPLI: Enable the PHY – link initialized interrupt. Leaving this bit in the reset (0) state allows the PLI bit to be read as a status bit.

Bit 18: R/W ELOA: Enable link–on active interrupt. Leaving this bit in the reset (0) state allows the LOA bit to be read as a status bit.

Bit 17: R/W ESCA: Enable SCLK active interrupt. Leaving this bit in the reset (0) state allows the SCA bit to be read as a status bit.

Bit 16: R/W ESCI: Enable SCLK inactive interrupt. Leaving this bit in the reset (0) state allows the SCI bit to be read as a status bit.

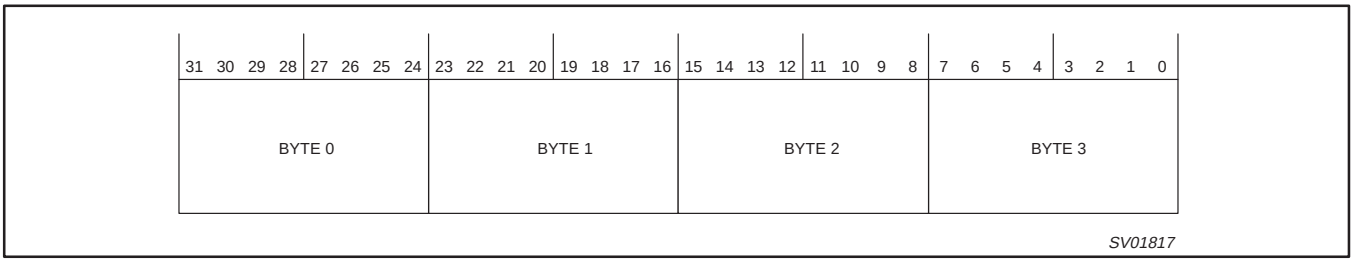
Bit 3: R/W PLI: PHY – link interface initialized interrupt. This interrupt indicates when the PHY – link initialization routine has been accomplished. This bit will be set upon completion of the initialization; if enabled, it will cause a host interface interrupt in order to inform the host controller of the completed action. Reset of this interrupt requires the writing of a (1) to this bit position. When used as a status bit, it will be necessary to first write a “1” to this bit position before reading the status of this bit. See Section 12.5.3 for a full explanation.

Bit 2: R/W LOA: Link–on active interrupt. This interrupt will become active when a link–on signal is received by the link from the PHY. This bit will remain active as long as the link–on signal is active. When enabled, this bit will set and cause a host interface interrupt when the link detects the presence of a link–on signal from the PHY. In practice, the link will be in the power down state when this interrupt occurs (a link–on packet was sent by another node on the bus which desires to communicate with this powered down node). Proper servicing of this interrupt will contain a scenario similar to: this node is in power down mode and the host controller has set the ELOA bit to enable the interrupt and the PHY of this node received a link–on packet from another node requesting this node to power up; (1) the host controller gets the interrupt and makes a decision to power up, (2) the host de–asserts SWPD (by hardware or software means... see SWPD above), (3) the host monitors SCA for a ”1” state, (4) when SCA is true, the host writes a 0 to the ELOA bit and then writes a 1 to the LOA interrupt bit to cancel the interrupt. The link is now powered up. When used as a status bit, it will be necessary to first write a “1” to this bit position before reading the status of this bit. See Section 12.5.3 for a full explanation.

Bit 1: R/W SCA: SCLK active interrupt. When the SCLK signal from the PHY to the link is present, this bit is set. If this interrupt has been enabled, the host will receive an interrupt when the SCLK becomes active (an example of such use might be during the recovery from a link power down situation). When used as a status bit, it will be necessary to first write a “1” to this bit position before reading the status of this bit. See Section 12.5.3 for a full explanation.

Bit 0: R/W SCI: SCLK inactive interrupt. When the SCLK signal is NOT active, this bit sets. If this interrupt is enabled, when the SCLK ceases to be active, the interrupt will occur. SCLK could become inactive due to the PHY connected to this link going into power down mode. SCI operates as a true status bit. See Section 12.5.3.

13.3.12 Shadow Register (SHADOW_REG) – Base Address: 0x0F4



Reset Value 0x0F0A0500

Bit 31..0: R/W The shadow register is a mechanism that allows a byte (8-bit) or word (16-bit) host interface write quadlets (32-bit) into the AV Link. Bytes or words can be written into the shadow register in any order and then written to the AV Link by asserting address line A8 with the desired address. For example, if you want to write to Transmit Request Next register (TX_RQ_NEXT), and you were using an 8-bit host, then you would write the first three bytes to the shadow register and the fourth byte to the address 0x188 (or 0x189, or 0x18A, or 0x18B). In practice, any write or read with address line A8 not asserted will be directed to the shadow register. To verify the settings of LTLEND and DATAINV, this register is initialized to 0x0F0A0500 on power up. Note, unlike the other registers in this device, access to this register should not be addressed with address line A8 = 1.

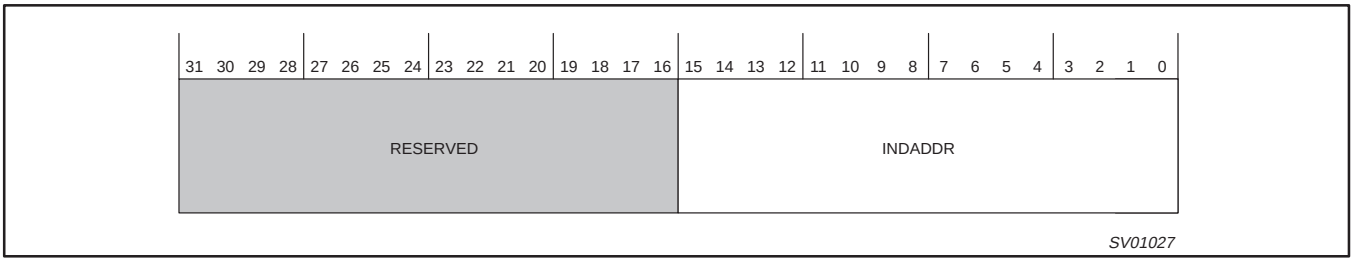
13.4 Indirect Address Registers

13.4.1

The host interface register set has been extended to provide additional control and data registers for FIFO size control and copy protection control registers. These extensions have been implemented via an indirect addressing mechanism. This mechanism allows software written for previous versions of the AV Link (PDI1394L21 and PDI1394L11) to operate on the PDI1394L40 with minimal changes.

To read or write from the indirect memory, you first write the appropriate address into the indirect address register (A8 = 1), then read or write from (or to) the indirect data increment the indirect address by one quadlet. Therefore, if you are writing several quadlets to continuous addresses, you will not need to increment the indirect address register.

13.4.2 Indirect Address Register (INDADDR) – Base Address: 0x0F8

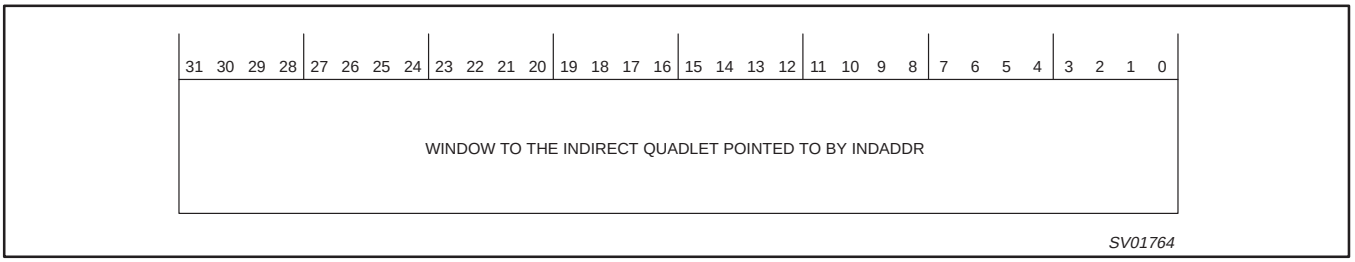


Bit 15..0: R/W Indirect Address: To read or write from the indirect memory, you first write the appropriate address into the indirect address register (A8 = 1), then read or write from (or to) the indirect data register (INDDATA, 0x0FC). Each write or read (A8 = 1) to the indirect data register (INDDATA) will automatically increment the indirect address by one quadlet. The following addresses are defined in the indirect address space:

Table 8. INDADDR address and function

INDADDR	FUNCTION
0–0x0FC	Reserved
0x100–0x1FC	FIFO Size Registers
0x500–0xFFFF	Reserved

13.4.3 Indirect Data Register (INDDATA) – Base Address: 0x0FC



Bit 31..0: R/W Quadlet of data pointed to by the indirect address n the INDADDR register (0x0F8). Note that the Indirect address autoincrements on each read or write of the INDDATA register.

13.5 Indirect Address Registers

The following registers are defined in the indirect address space. Access to these registers must be made through the Indirect Address (INDADDR) and Indirect Data (INDDATA) registers.

13.5.1 Registers for FIFO Size Programming

Each FIFO can be programmed to a certain size with a granularity of 64 quadlets. The size is determined by the values of the base_fifo and end_fifo fields of the FIFO Size registers. The following formula applies:

fifo_size = (end_fifo – base_fifo + 1) × 64 quadlets

The FIFO's have been implemented on a single memory. The base_fifo and end_fifo fields are sued to determine the physical start and end address of each FIFO inside the memory.

The start address of a FIFO is {fifo_addr[11:6] = base_fifo, fifo_addr[5:0] = 000000}.
The end address of a FIFO is {fifo_addr[11:6] = end_fifo, fifo_addr[5:0] = 111111}.
Note: The end_fifo must be larger than base_fifo and the hardware does not check for invalid values.

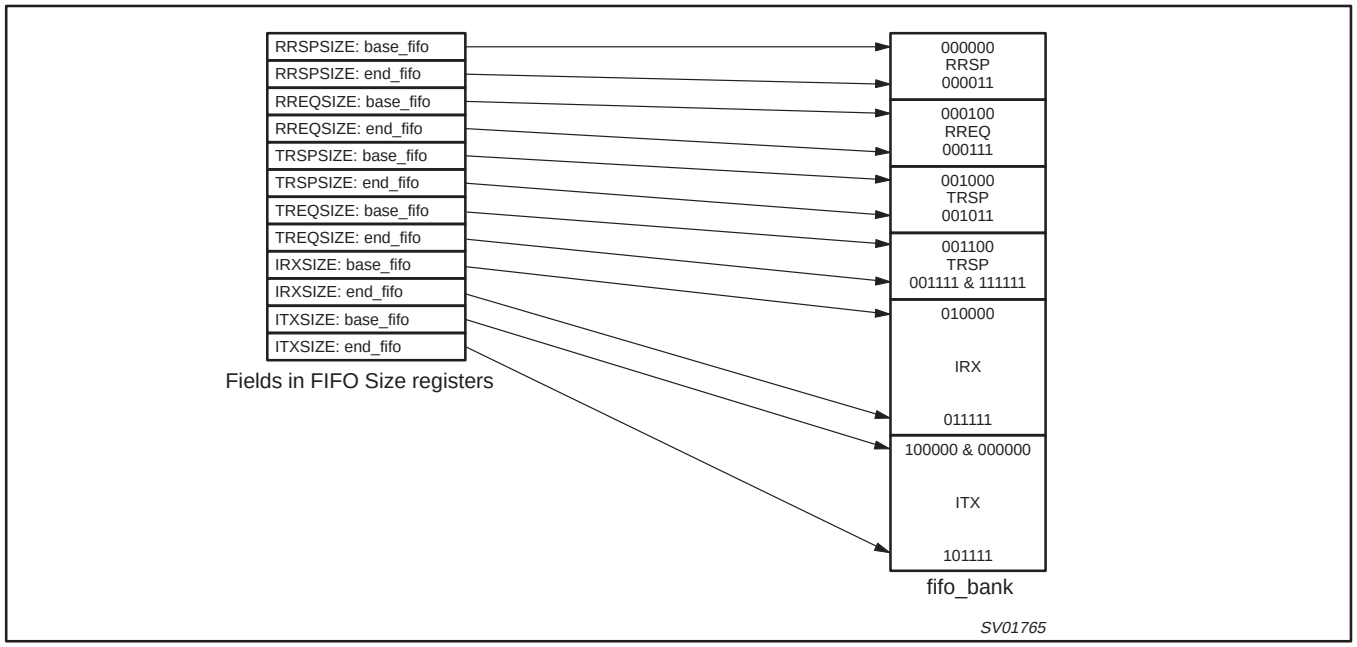
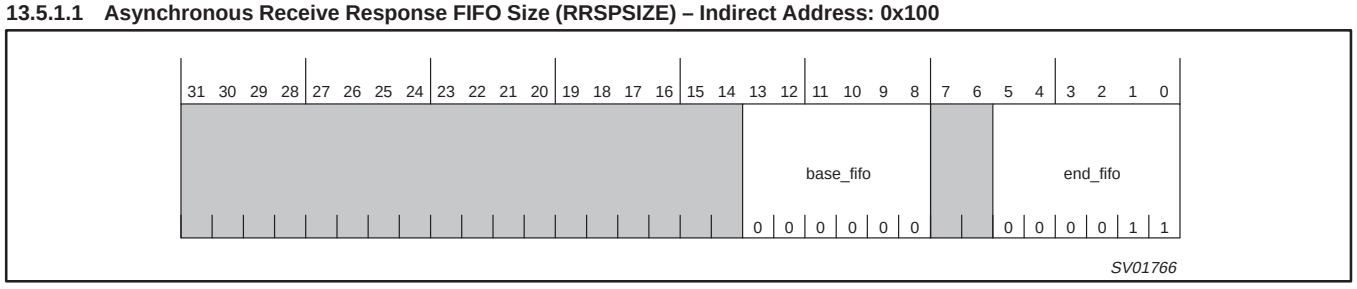


Figure 34. Reset situation of size programmable FIFOs

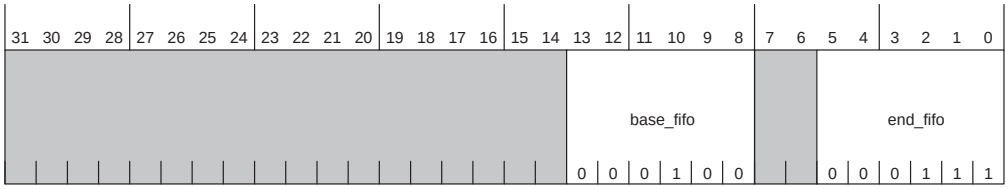
13.5.1.1 Asynchronous Receive Response FIFO Size (RRSPSIZE) – Indirect Address: 0x100



Reset Value 0x00000003

Bit 31..14	R/W	Unused bits read '0'
Bit 13..8	R/W	base_fifo: Base address of the FIFO
Bit 7, 6	R/W	Unused bits read '0'
Bit 5..0	R/W	end_fifo: End address of the FIFO

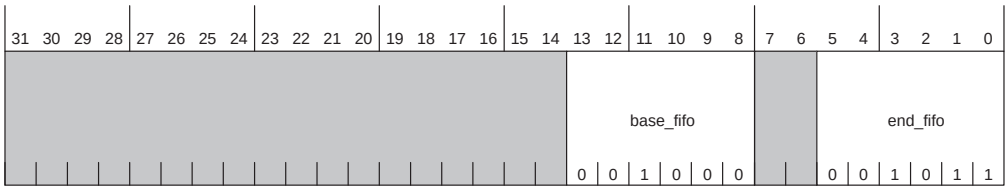
13.5.1.2 Asynchronous Receive Request FIFO Size (RREQSIZE) – Indirect Address: 0x104



Reset Value 0x00000407

Bit 31..14	R/W	Unused bits read ‘0’
Bit 13..8	R/W	base_fifo: Base address of the FIFO
Bit 7, 6	R/W	Unused bits read ‘0’
Bit 5..0	R/W	end_fifo: End address of the FIFO

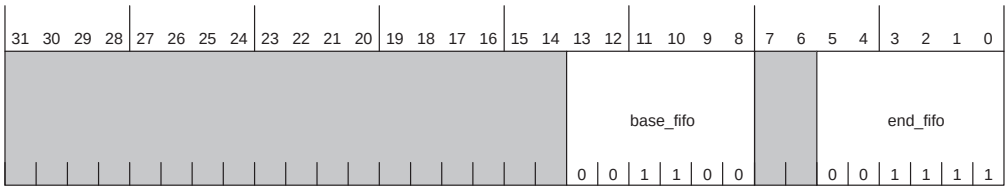
13.5.1.3 Asynchronous Transmit Response FIFO Size (TRSPSIZE) – Indirect Address: 0x110



Reset Value 0x0000080B

Bit 31..14	R/W	Unused bits read ‘0’
Bit 13..8	R/W	base_fifo: Base address of the FIFO
Bit 7, 6	R/W	Unused bits read ‘0’
Bit 5..0	R/W	end_fifo: End address of the FIFO

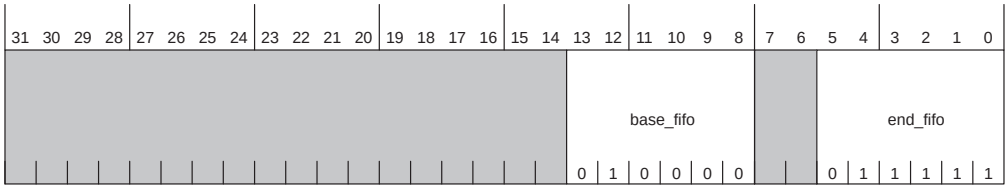
13.5.1.4 Asynchronous Transmit Request FIFO Size (TREQSIZE) – Indirect Address: 0x114



Reset Value 0x00000C0F

Bit 31..14	R/W	Unused bits read ‘0’
Bit 13..8	R/W	base_fifo: Base address of the FIFO
Bit 7, 6	R/W	Unused bits read ‘0’
Bit 5..0	R/W	end_fifo: End address of the FIFO

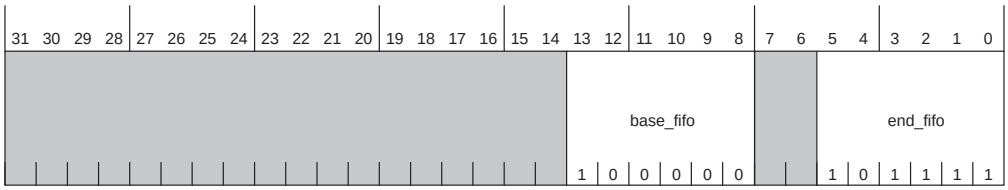
13.5.1.5 Isochronous Receiver FIFO Size (IRXSIZE) – Indirect Address: 0x120



Reset Value 0x0000101F

Bit 31..14	R/W	Unused bits read ‘0’
Bit 13..8	R/W	base_fifo: Base address of the FIFO
Bit 7, 6	R/W	Unused bits read ‘0’
Bit 5..0	R/W	end_fifo: End address of the FIFO

13.5.1.6 Isochronous Transmitter FIFO Size (ITXSIZE) – Indirect Address: 0x130



Reset Value 0x0000202F

Bit 31..14	R/W	Unused bits read ‘0’
Bit 13..8	R/W	base_fifo: Base address of the FIFO
Bit 7, 6	R/W	Unused bits read ‘0’
Bit 5..0	R/W	end_fifo: End address of the FIFO

14.0 DC ELECTRICAL CHARACTERISTICS

Table 9. DC Electrical Characteristics

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTE
V_{IL}	LOW input voltage			0.8	V	Pin categories 1, 2, 3
V_{IH}	HIGH input voltage		2.0		V	Pin categories 1, 2, 3
$V_{IT1}+$	Input threshold, rising edge		$V_{DD}/2 + 0.3$	$V_{DD}/2 + 0.9$	V	Pin categories 6, 8 LOW to HIGH transition
$V_{IT1}–$	Input threshold, falling edge		$V_{DD}/2 – 0.9$	$V_{DD}/2 – 0.3$	V	Pin categories 6, 8 HIGH to LOW transition
$V_{IT2}+$	Input threshold, rising edge			$.42 V_{DD} + 1.0$	V	Pin category 9 LOW to HIGH transition
$V_{IT2}–$	Input threshold, falling edge		$.42 V_{DD} + 0.2$		V	Pin category 9 HIGH to LOW transition
V_{OH1}	HIGH output voltage		2.4		V	Pin category 1 I_{OH} = 4mA I_{OL} = 4mA
V_{OL1}	LOW output voltage			0.4	V	Pin category 1 I_{OH} = 4mA I_{OL} = 4mA
V_{OH2}	HIGH output voltage		2.4		V	Pin categories 4, 6, 7 I_{OH} = 4mA
V_{OL2}	LOW output voltage			0.4	V	Pin categories 4, 5, 6, 7 I_{OL} = 4mA
I_L	Input leakage current	V_{dd} = 3.6 V		±1	µA	Pin categories 2, 3, 9 V_I = 5.5 V or 0 V
I_L	Input leakage current	ISON = high		1000	µA	Pin categories 6, 8 V_{DD} = 3.6 V, $V_{IN} = V_{DD}/2$
		ISON = low		5	µA	Pin categories 6, 8 V_{DD} = 3.6 V, V_{IN} = 0 V, 3.6 V
I_L	Input leakage current	ISON = high		500	µA	Pin categories 6, 8 V_{DD} = 3.0 V, V_{IN} = 5.5 V
		ISON = low		750	µA	Pin categories 6, 8 V_{DD} = 0 V, V_{IN} = 5.5 V
I_{OZ}	3-State output current	V_{DD} = 3.6 V		±5	µA	Pin categories 1, 7 V_I = 5.5 V or 0 V
I_{DD}	Supply current	Operating		200	mA	V_{DD} = 3.6 V
		Powered–down		10	mA	V_{DD} = 3.6 V

14.1 Pin Categories

Table 10. Pin Categories

Category 1: Input/Output	Category 2: Input	Category 3: Input	Category 4: Output	Category 5: Output	Category 6: Input/Output	Category 7: Output	Category 8: Input	Category 9: Input
HIF AD[7:0]	HIF A[8]	RESETN	CYCLEOUT	HIF INTN	PHY D[0:7]	LREQ	SCLK	LNKON
AVxSYNC	HIF CSN	CYCLEIN	CLK50		PHY CTL[0:1]	LPS		
AV2ERR0	HIF WRN	ISON	HIF WAIT					
AV2ERR1		HIF MUX						
AVxVALID	AVxENDPCK	HIF16BIT						
AV xD[7:0]	HIF ALE	1394MODE	AV1ERR0					
AVxCLK	HIF RDN		AV1ERR1					
AVxFSYNC								
HIF D[15:8]								
HIF A[7:0]								
AVxSYSYNC								
AVxSY								
AVxREADY								

15.0 AC CHARACTERISTICS

GND = 0 V, C_L = 50 pF

SYMBOL	PARAMETER	TEST CONDITIONS	WAVEFORMS	LIMITS			UNIT
				T_{amb} = 0 °C to +70 °C			
				MIN	TYP	MAX	
t_{PERIOD} (parallel mode)	AV clock period		Figure 36	41.67			ns
t_{SU}	AV clock setup time		Figure 36	4			ns
t_{IH}	AV clock input hold time		Figure 36	3			ns
t_{OD}	AV clock output delay time		Figure 36	3		24	ns
t_{WHIGH}	AV clock pulse width HIGH		Figure 36	10			
t_{WLOW}	AV clock pulse width LOW		Figure 36	10			
t_{PWFS}	AVxFSYNC pulse width HIGH		Figure 37	200		300	ns
t_{SUP}	PHY-link setup time		Figure 38	6.0			ns
t_{HP}	PHY-link hold time		Figure 38	0			ns
$t_{SCLKPER}$	SCLK period		Figure 38	20.343	20.345	20.347	ns
t_{DP}	PHY-link output delay	Note: C_L = 20 pF	Figure 39	2.0		10.0	ns
t_{AS}	Host address setup time		Figure 40	0			ns
t_{AH}	Host address hold time		Figure 40	2			ns
t_{CL}	Host chip select pulse width LOW		Figure 40	115			ns
t_{CH}	Host chip select pulse width HIGH		Figure 40	42			ns
t_{RP}	Host read pulse width		Figure 40	115			ns
t_{ACC}	Host access time		Figure 40			115	ns
t_{DH}	Host data hold time		Figure 40	2			ns
t_{DS}	Host data setup time		Figure 40	0			ns
t_{DZ}	Host data bus release (Hi-Z)		Figure 40			15	ns
t_{WRP}	Host write pulse width		Figure 40	115			ns
t_{WAIT}	WAIT output delay		Figure 40			12	ns
t_{WWAIT}	WAIT pulse width		Figure 40	62			ns
t_{CWH}	CYCLEIN HIGH pulse width		Figure 41	200			ns
t_{CWL}	CYCLEIN LOW pulse width		Figure 41	200			ns
t_{CP}	CYCLEIN cycle period		Figure 41	125			µs
t_{CD}	CYCLEOUT cycle delay		Figure 42			20	ns
t_{RESET}	RESET_N pulse width LOW		Figure 43	10			µs
t_{PWALE}	ALE pulse width		Figures 8, 9, 10	20			ns
t_{ALES}	ALE setup time		Figures 8, 9, 10	3			ns
t_{ALEH}	ALE hold time		Figures 8, 9, 10	2			ns
f_{LPS}	LPS signal frequency		–	1.0		2.75	MHz
dc_{LPS}	LPS signal duty cycle		–	23		28	%

16.0 TIMING DIAGRAMS

16.1 AV Interface Operation

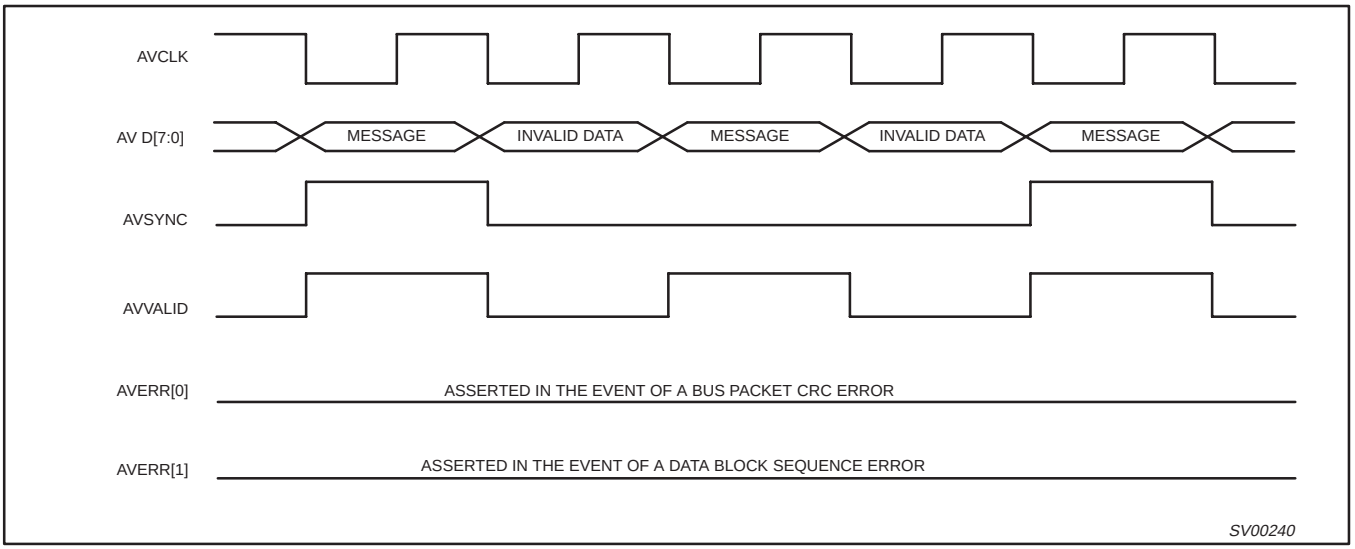


Figure 35. AV Parallel Interface Operation Diagram

16.2 AV Interface Critical Timings

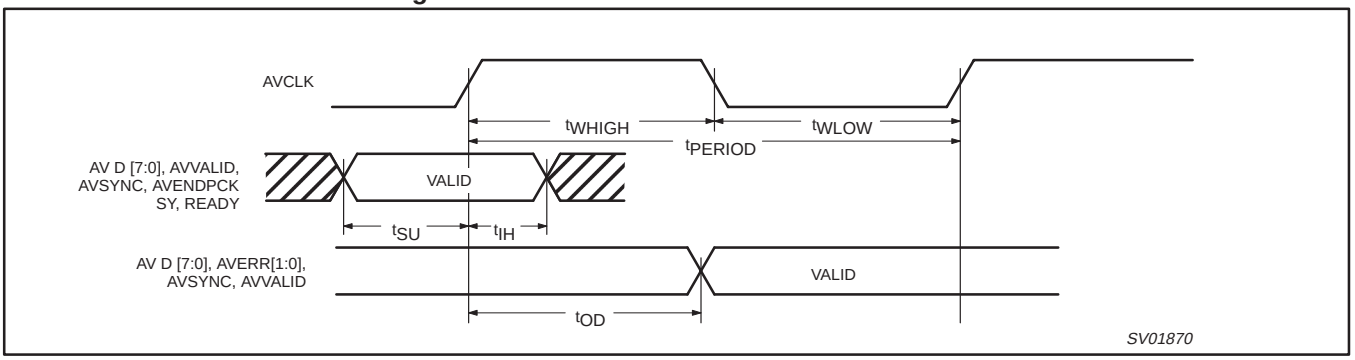
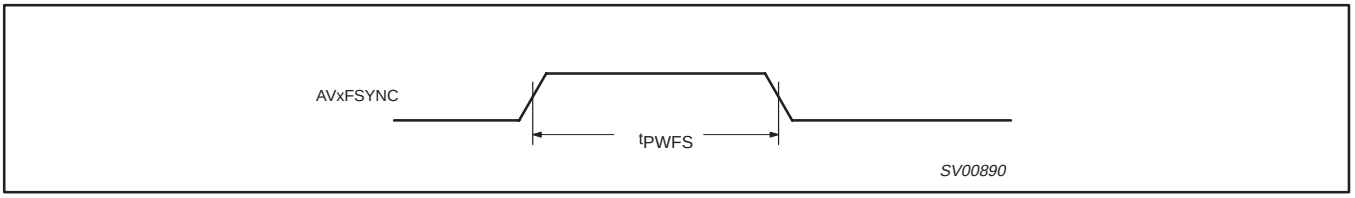


Figure 36. AV Interface Timing Diagram



NOTE:
1. Timing shown is for AVxFSYNC used as an output only. When AVxFSYNC is used as an input, only the rising edge of the signal is considered as long as the input pulse width exceeds 40 nS.

Figure 37. AVxFSYNC Timing Diagram

16.3 PHY-Link Interface Critical Timings

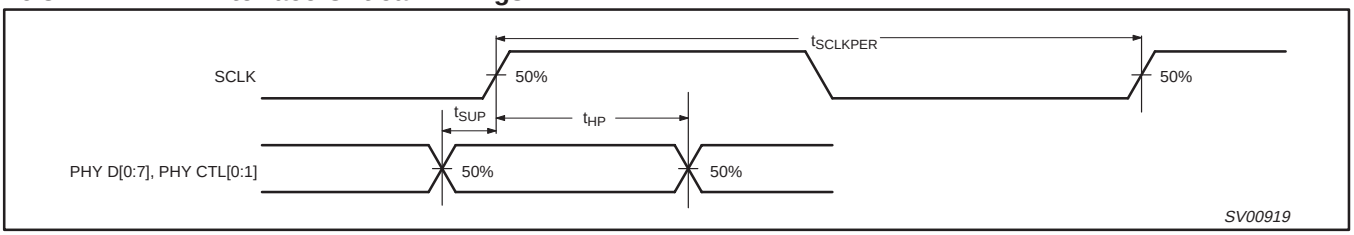


Figure 38. PHY D[0:7], PHY CTL[0:1] Input Setup and Hold Timing Waveforms

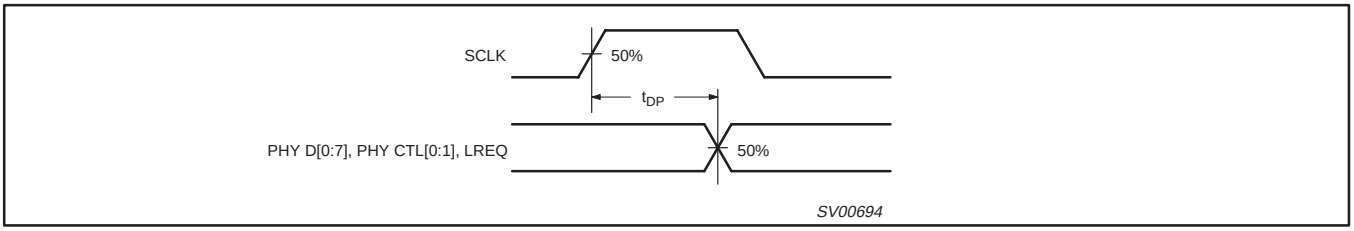
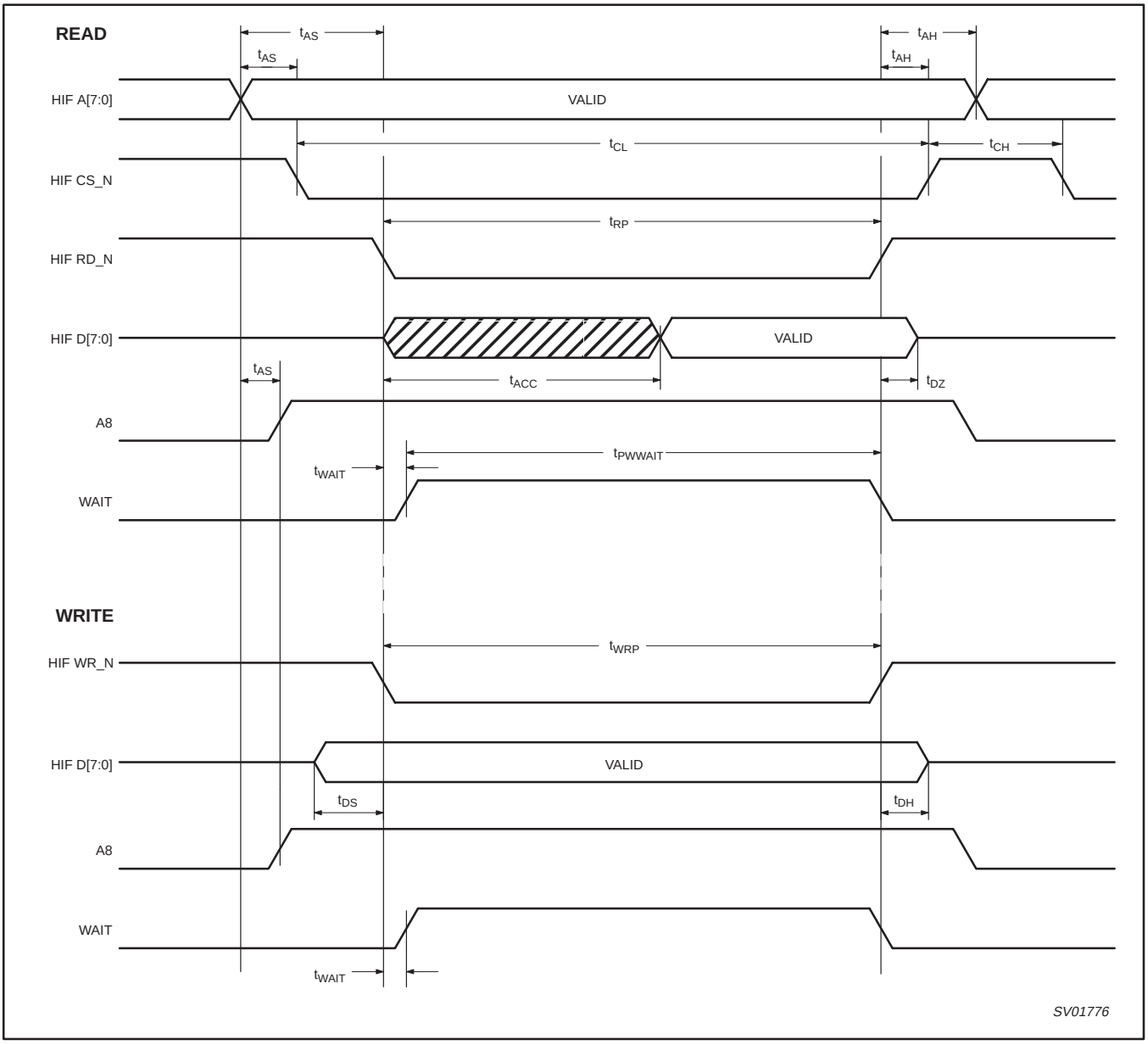


Figure 39. PHY D[0:7], PHY CTL[0:1], and LREQ Output-Delay Timing Waveforms

16.4 Host Interface Critical Timings



NOTE:
1. Wait line asserts only during Read and Write cycles in which A8 is asserted.

Figure 40. Host Interface Timing Waveforms

16.5 CYCLEIN/CYCLEOUT Timings

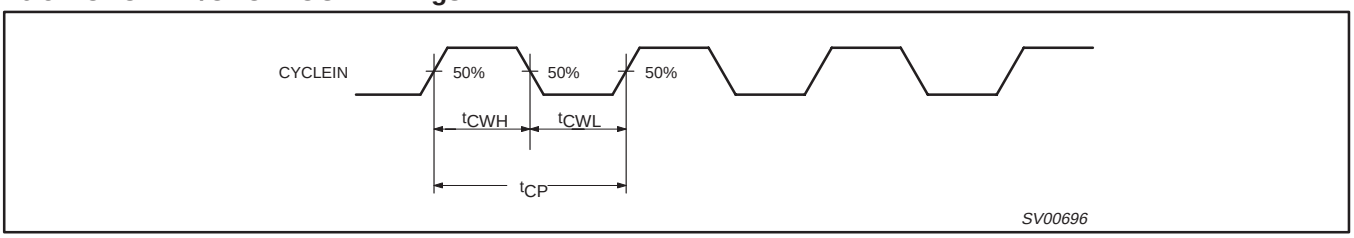


Figure 41. CYCLEIN Waveform

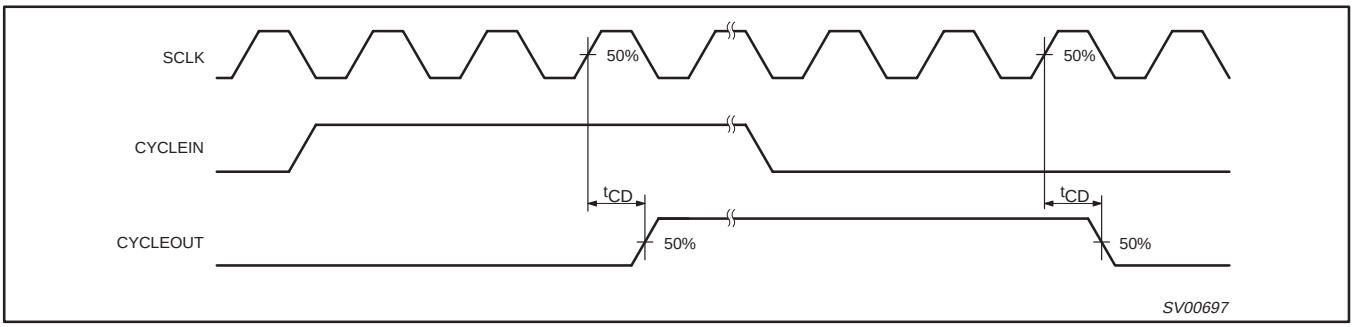


Figure 42. CYCLEOUT Waveforms

16.6 $\overline{\text{RESET}}$ Timings

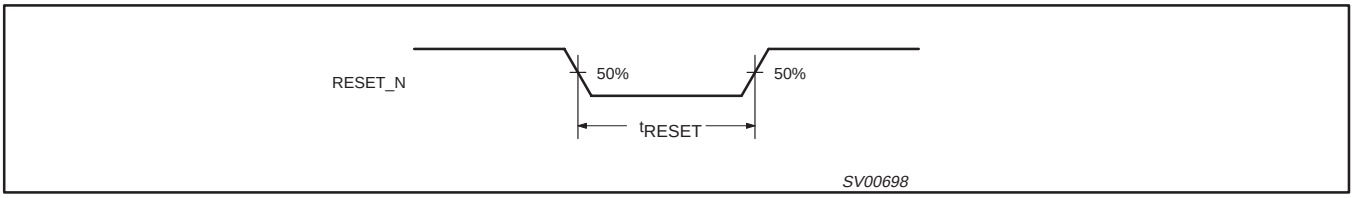
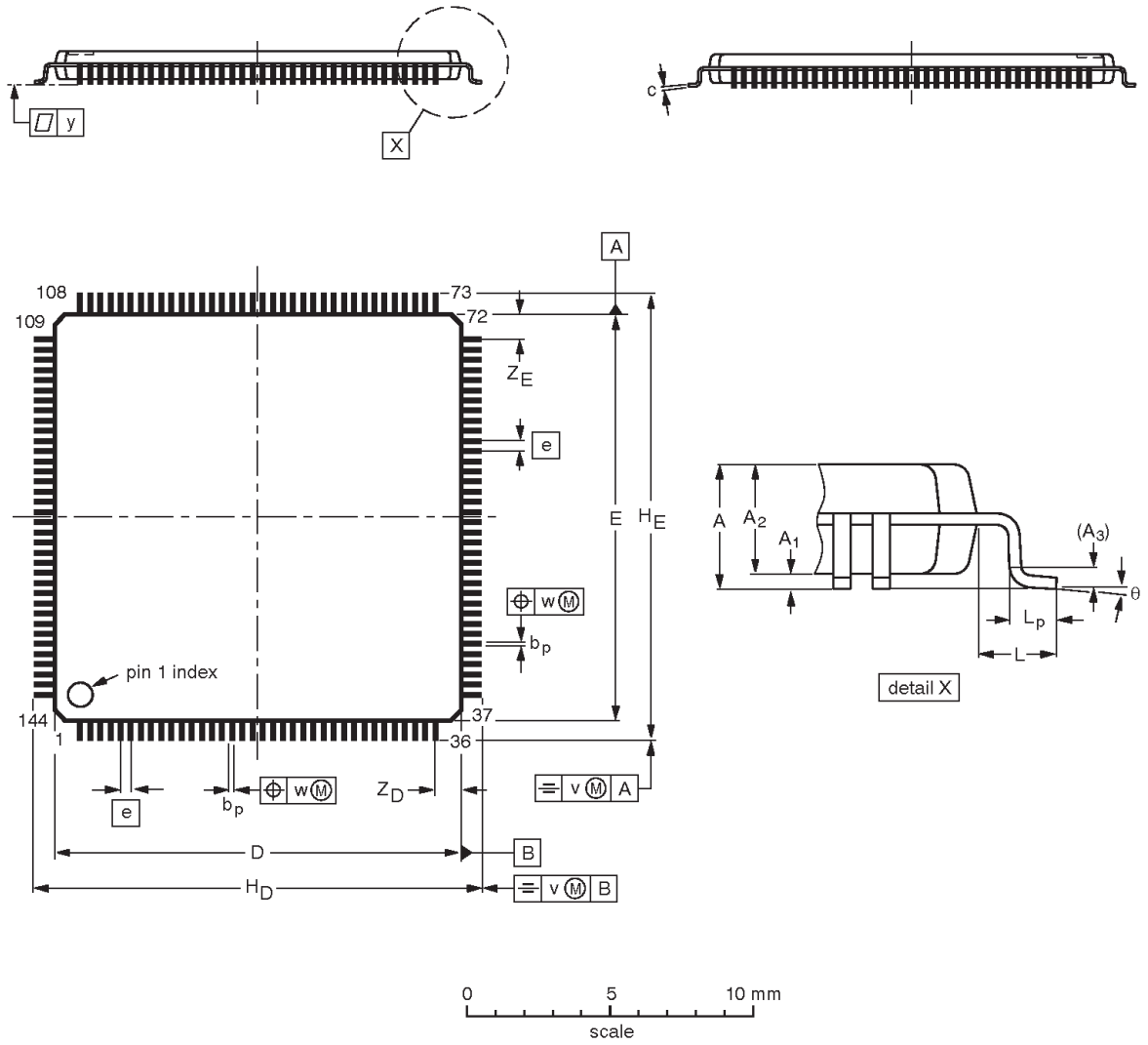


Figure 43. RESET_N Waveform

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm SOT486-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.50	22.15 21.85	22.15 21.85	1.0	0.75 0.45	0.2	0.08	0.08	1.40 1.10	1.40 1.10	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT486-1	136E23	MS-026				~~99-12-03~~ 00-01-19

Data sheet status

Data sheet status	Product status	Definition [1]
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Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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ERRATA FOR THE PHILIPS
PDI1394L40 1394 ENHANCED AV LINK LAYER CONTROLLER

(This errata list refers only to version 0301 of the L40 chip... package date codes after 0030 and the L40 Data Sheet dated 2000 December 15)

Chip Errata:

E–1 **AV1READY pin initialization state (after hardware reset of the chip)**

Description of expected operation: This pin should be in an output state with a LOW level applied immediately after power on reset and after any subsequent hardware reset.

Description of observed behavior: The AV1READY pin is in an undefined output state (with level being HIGH or LOW) after power–up and after subsequent hardware resets of the L40.

Solution or work around: The host controller software power–up routine should be modified to place the pin state in the proper condition (as it will be used later) immediately after power–up and after any subsequent hardware reset. The proper state of the pin can be set by means of the GLOBCSR register (0x018), by placing the proper states on bits 16 and 17, DIRAV1 and ENOUTAV1.

E–2 **Register 0x008, LNKPHYINTACK, bit 11 is set at all times.**

Description of expected operation: This bit position is not used and therefore should indicate a ”0” or reset condition at all times.

Description of observed behavior: This bit always indicates a ”1” state.

Solution or work around: Ignore the state of this bit in this register. The reset state of this register is ”00000800” instead of the data sheet indicated ”00000000”. The state of this bit will be changed to ”0” in subsequent versions of this part.

E–3 **RDI register bits do not function properly when the L40 part is used with PDI1394P11A PHY.**

Description of expected operation: When the L40 is placed in power–down mode (either by setting the SWPD bit in the RDI register or placing the PD pin in the HIGH state), the L40 stops producing the LPS signal and the PHY interprets this lack of LPS signal as the impetus to remove the SYSCLK (system clock) from the link – PHY interface. This action causes the L40 to enter power–down mode and should place the SCA bit LOW, the PLI bit LOW, and the SCI bit HIGH.

Description of observed behavior: The SCA, PLI and SCI bits of the RDI register do not reset / set when SWPD or the PD pin is asserted. This is due to the fact that the SYSCLK output of the P11A PHY remains HIGH when the clock is stopped. The SCA and PLI bits will erroneously read as if the L40 is powered up, they will both remain HIGH. The SCI bit, which is normally set (1) when the L40 is powered–down, will remain reset (0) in this case. Reading the status of these bits in the RDI register will give a false indication that the L40 is operating when it is not.

Solution or work around: A hardware work–around for this problem exists. It consists of adding a pull down resistor to set a low dc bias level on the SCLK input of the L40 so as to make the pin go to the LOW state when the clock is not present. The value of the resistor is R= 3.3 KOhms; a 1/10th watt type is sufficient.

E–4 **When L40 is used with IEEE 1394–1995 compatible PHYs, RDI register bit ”PLI” does not function.**

Description of expected operation: When the L40 is placed in power–down mode (either by setting the SWPD bit in the RDI register or placing the PD pin in the HIGH state), the L40 stops producing the LPS signal and the PHY interprets this lack of LPS signal as a request to remove the SYSCLK (system clock) from the link – PHY interface. This action causes the L40 to enter power–down mode and should place the SCA bit LOW, the PLI bit LOW, and the SCI bit HIGH.

Description of observed behavior: The PLI bit (bit 3) always indicates a set (1) condition regardless of whether the L40 is powered up or powered down. This is normal bit PLI operation when the L40 is used with a NON 1394A type of PHY.

Solution or work around: Non–1394A PHYs do not initialize the link–PHY interface... this is normal functioning. When the L40 is operated with its 1394 MODE pin held high (as is the case when operating with a 1394–1995 PHY) the PLI bit in the RDI register will always be seen as set (1). In order to determine the status of operation of the L40, the SCA and SCI bits may be used (SCI bit recommended) to determine the power status of the link chip. The PLI bit should be ignored by the node operating software when the L40 is operated with a NON–1394A PHY with the L40 1394 MODE pin at 3.3v (high).