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QUAD E1 SHORT HAUL LINE INTERFACE UNIT

IDT82V2054

FEATURES

- Fully integrated quad E1 short haul line interface which supports 120 Ω twisted pair and 75 Ω coaxial applications
- Selectable Single Rail mode or Dual Rail mode and AMI or HDB3 encoder/decoder
- Built-in transmit pre-equalization meets G.703
- Selectable transmit/receive jitter attenuator meets ETSI CTR12/13, ITU G.736, G.742 and G.823 specifications
- SONET/SDH optimized jitter attenuator meets ITU G.783 mapping jitter specification
- Digital/Analog LOS detector meets ITU G.775 and ETS 300 233
- ITU G.772 non-intrusive monitoring for in-service testing for any one of channel 1 to channel 3
- Low impedance transmit drivers with high-Z
- Selectable hardware and parallel/serial host interface
- Local and Remote Loopback test functions
- Hitless Protection Switching (HPS) for 1 + 1 protection without relays
- JTAG boundary scan for board test
- 3.3 V supply with 5 V tolerant I/O
- Low power consumption
- Operating temperature range: -40°C to +85°C
- Available in 144-pin Thin Quad Flat Pack (TQFP) and 160-pin Plastic Ball Grid Array (PBGA) packages

  Green package options available

FUNCTIONAL BLOCK DIAGRAM

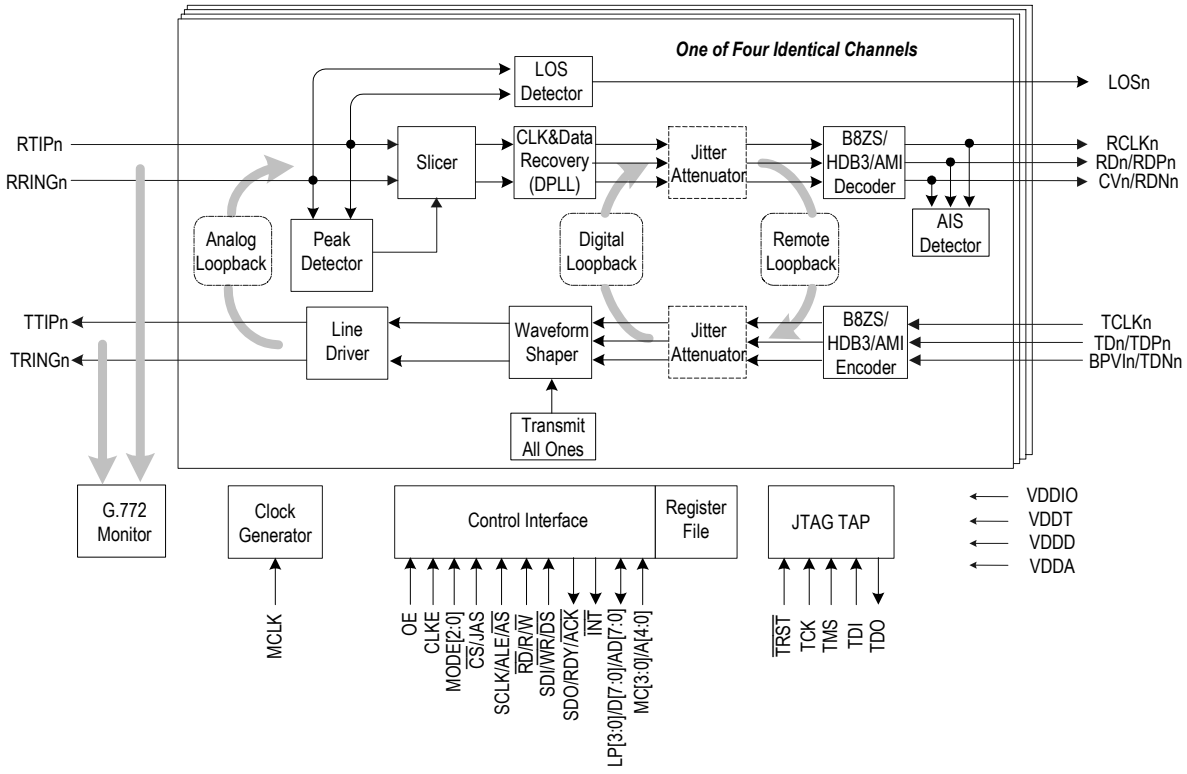


Figure-1 Block Diagram

DESCRIPTION

The IDT82V2054 is a single chip, 4-channel E1 short haul PCM transceiver with a reference clock of 2.048 MHz. The IDT82V2054 contains 4 transmitters and 4 receivers.

All the receivers and transmitters can be programmed to work either in Single Rail mode or Dual Rail mode. HDB3 or AMI encoder/decoder is selectable in Single Rail mode. Pre-encoded transmit data in NRZ format can be accepted when the device is configured in Dual Rail mode. The receivers perform clock and data recovery by using integrated digital phase-locked loop. As an option, the raw sliced data (no retiming) can be output on the receive data pins. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance.

A jitter attenuator is integrated in the IDT82V2054 and can be switched into either the transmit path or the receive path for all channels. The jitter attenuation performance meets ETSI CTR12/13, ITU G.736, G.742 and G.823 specifications.

The IDT82V2054 offers hardware control mode and software control mode. Software control mode works with either serial host interface or parallel host interface. The latter works via an Intel/Motorola compatible 8-bit parallel interface for both multiplexed or non-multiplexed applications. Hardware control mode uses multiplexed pins to select different operation modes when the host interface is not available to the device.

The IDT82V2054 also provides loopback and JTAG boundary scan testing functions. Using the integrated monitoring function, the IDT82V2054 can be configured as a 4-channel transceiver with non-intrusive protected monitoring points.

The IDT82V2054 can be used for SDH/SONET multiplexers, central office or PBX, digital access cross connects, digital radio base stations, remote wireless modules and microwave transmission systems.

PIN CONFIGURATIONS

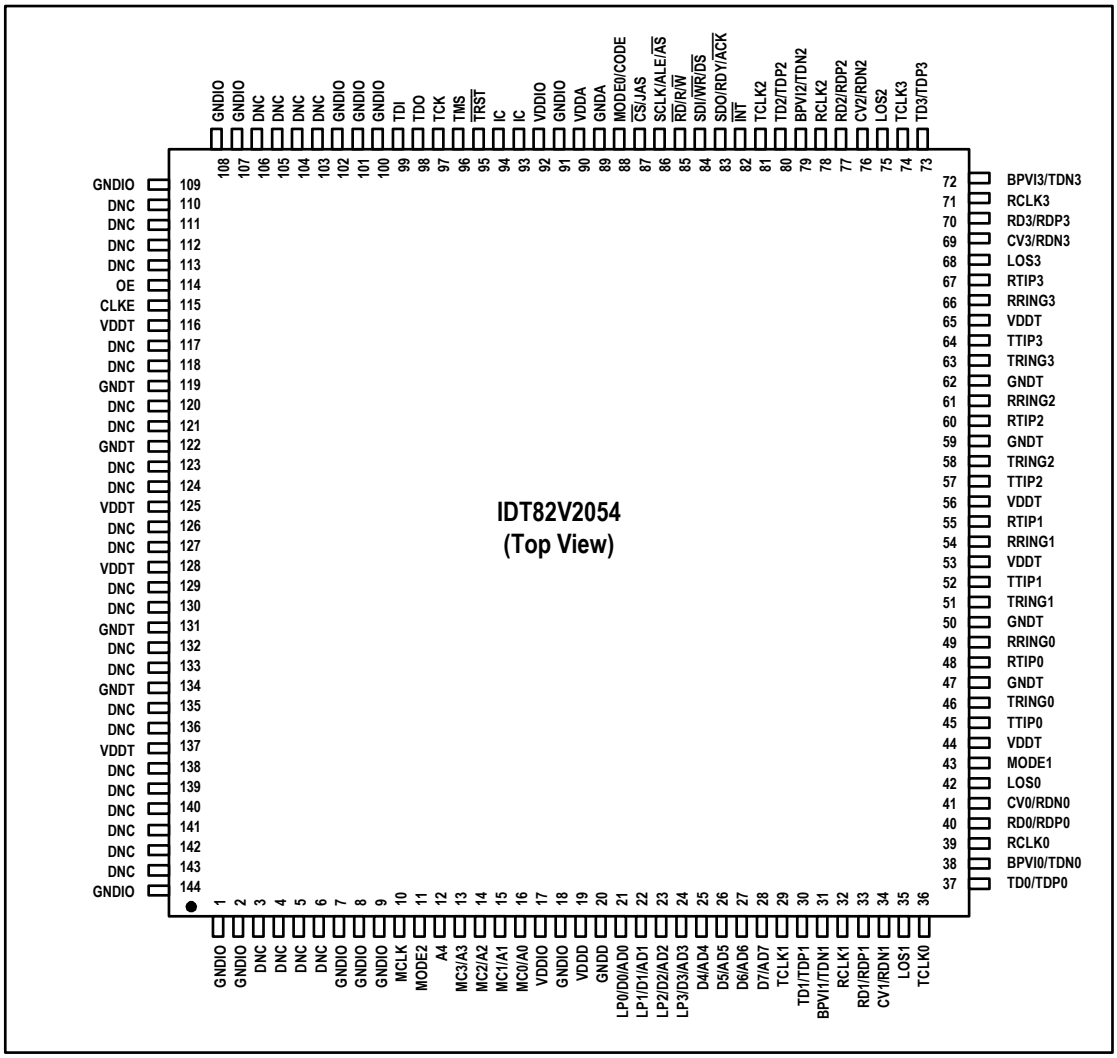


Figure-2 TQFP144 Package Pin Assignment

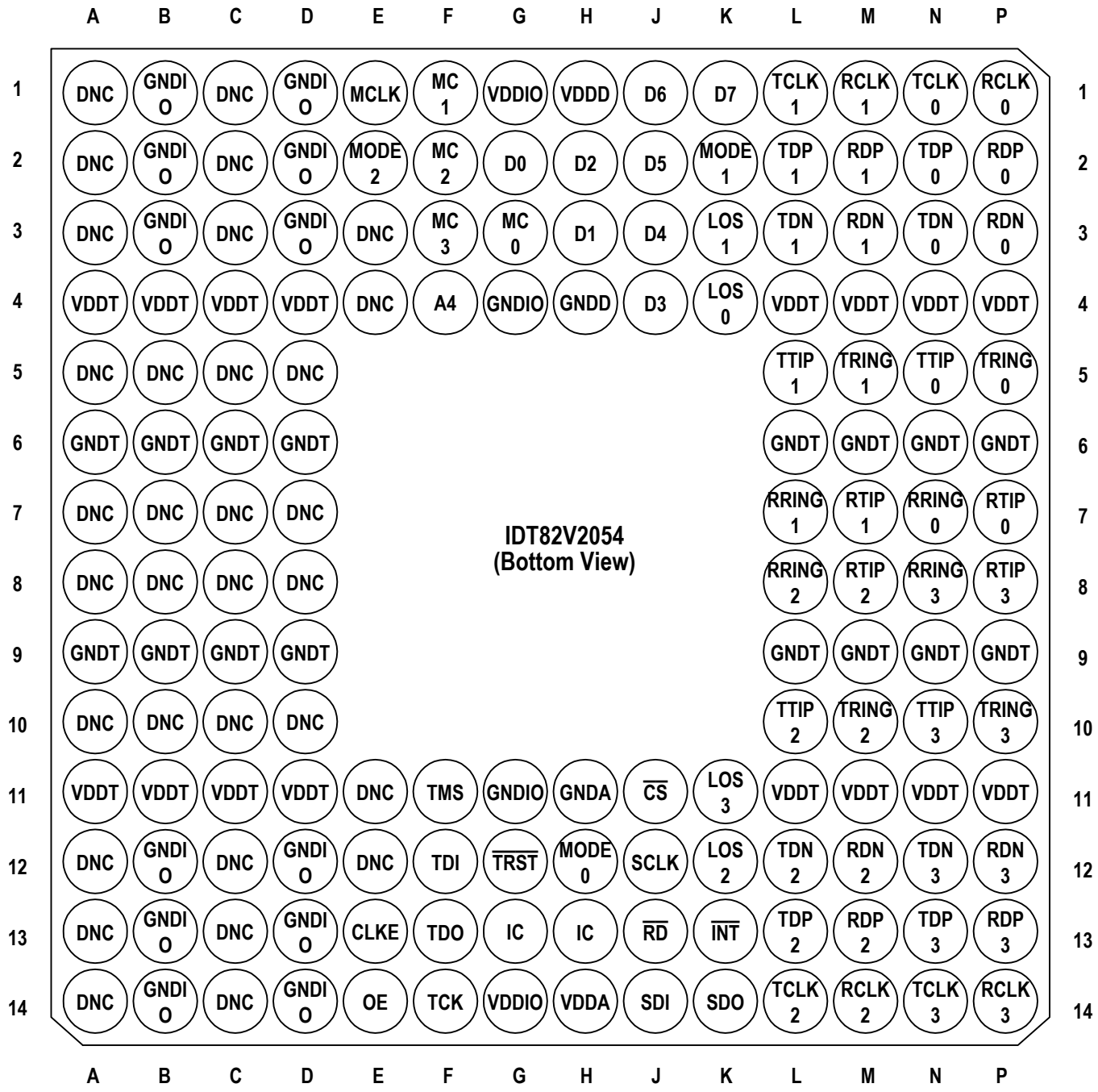


Figure-3 PBGA160 Package Pin Assignment

1 PIN DESCRIPTION

Table-1 Pin Description

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
Transmit and Receive Line Interface				
TTIP0 TTIP1 TTIP2 TTIP3	Analog Output	45 52 57 64	N5 L5 L10 N10	**TTIPn/TRINGn: Transmit Bipolar Tip/Ring for Channel 0~3** These pins are the differential line driver outputs. They will be in high-Z state if pin OE is low or the corresponding pin TCLKn is low (pin OE is global control, while pin TCLKn is per-channel control). In host mode, each pin can be in high-Z by programming a '1' to the corresponding bit in register **OE**(1).
TRING0 TRING1 TRING2 TRING3		46 51 58 63	P5 M5 M10 P10	
RTIP0 RTIP1 RTIP2 RTIP3	Analog Input	48 55 60 67	P7 M7 M8 P8	**RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 0~3** These pins are the differential line receiver inputs.
RRING0 RRING1 RRING2 RRING3		49 54 61 66	N7 L7 L8 N8	
Transmit and Receive Digital Data Interface				
TD0/TDP0 TD1/TDP1 TD2/TDP2 TD3/TDP3	I	37 30 80 73	N2 L2 L13 N13	**TDn: Transmit Data for Channel 0~3** When the device is in Single Rail mode, the NRZ data to be transmitted is input on this pin. Data on TDn is sampled into the device on the falling edges of TCLKn, and encoded by AMI or HDB3 line code rules before being transmitted to the line. **BPVIn: Bipolar Violation Insertion for Channel 0~3** Bipolar violation insertion is available in Single Rail mode 2 (see Table-2 on page 13 and Table-3 on page 14) with AMI enabled. A low-to-high transition on this pin will make the next logic one to be transmitted on TDn the same polarity as the previous pulse, and violate the AMI rule. This is for testing. **TDPn/TDNn: Positive/Negative Transmit Data for Channel 0~3** When the device is in Dual Rail Mode, the NRZ data to be transmitted for positive/negative pulse is input on this pin. Data on TDPn/TDNn are sampled on the falling edges of TCLKn. The line code in dual rail mode is as the follow: TDPn / TDNn / Output Pulse 0 / 0 / Space 0 / 1 / Negative Pulse 1 / 0 / Positive Pulse 1 / 1 / Space Pulling pin TDNn high for more than 16 consecutive TCLK clock cycles will configure the corresponding channel into Single Rail mode 1 (see Table-2 on page 13 and Table-3 on page 14).
BPVI0/TDN0 BPVI1/TDN1 BPVI2/TDN2 BPVI3/TDN3		38 31 79 72	N3 L3 L12 N12	

1. Register name is indicated by bold capital letter. For example, **OE** indicates Output Enable Register.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>TCLK0
TCLK1
TCLK2
TCLK3</td><td>I</td><td>36
29
81
74</td><td>N1
L1
L14
N14</td><td>TCLKn: Transmit Clock for Channel 0~3
The clock of 2.048 MHz for transmit is input on this pin. The transmit data at TDn/TDPn or TDNn is sampled into the device on the falling edges of TCLKn.
Pulling TCLKn high for more than 16 MCLK cycles, the corresponding transmitter is set in Transmit All Ones (TAOS) state (when MCLK is clocked). In TAOS state, the TAOS generator adopts MCLK as the clock reference.
If TCLKn is low, the corresponding transmit channel is set into power down state, while driver output ports become high-Z.
Different combinations of TCLKn and MCLK result in different transmit mode. It is summarized as the follows:
<table>
<tr><th>MCLK</th><th>TCLKn</th><th colspan="2">Transmit Mode</th></tr>
<tr><td>Clocked</td><td>Clocked</td><td colspan="2">Normal operation</td></tr>
<tr><td>Clocked</td><td>High (≥ 16 MCLK)</td><td colspan="2">Transmit All Ones (TAOS) signals to the line side in the corresponding transmit channel.</td></tr>
<tr><td>Clocked</td><td>Low (≥ 64 MCLK)</td><td colspan="2">The corresponding transmit channel is set into power down state.</td></tr>
<tr><td rowspan="4">High/Low</td><td rowspan="4">TCLK1 is clocked</td><td>TCLKn is clocked</td><td>Normal operation</td></tr>
<tr><td>TCLKn is high (≥ 16 TCLK1)</td><td>Transmit All Ones (TAOS) signals to the line side in the corresponding transmit channel.</td></tr>
<tr><td>TCLKn is low (≥ 64 TCLK1)</td><td>Corresponding transmit channel is set into power down state.</td></tr>
<tr><td colspan="2">The receive path is not affected by the status of TCLK1. When MCLK is high, all receive paths just slice the incoming data stream. When MCLK is low, all the receive paths are powered down.</td></tr>
<tr><td>High/Low</td><td>TCLK1 is unavailable.</td><td colspan="2">All four transmitters (TTIPn & TRINGn) will be in high-Z.</td></tr>
</table>
</td></tr>
<tr><td>RD0/RDP0
RD1/RDP1
RD2/RDP2
RD3/RDP3

CV0/RDN0
CV1/RDN1
CV2/RDN2
CV3/RDN3</td><td>O

High-Z</td><td>40
33
77
70

41
34
76
69</td><td>P2
M2
M13
P13

P3
M3
M12
P12</td><td>RDn: Receive Data for Channel 0~3
In Single Rail mode, the received NRZ data is output on this pin. The data is decoded by AMI or HDB3 line code rule.

CVn: Code Violation for Channel 0~3
In Single Rail mode, the bipolar violation, code violation and excessive zeros will be reported by driving pin CVn high for a full clock cycle. However, only bipolar violation is indicated when AMI decoder is selected.

RDPn/RDNn: Positive/Negative Receive Data for Channel 0~3
In Dual Rail Mode with clock recovery, these pins output the NRZ data. A high signal on RDPn indicates the receipt of a positive pulse on RTIPn/RRINGn while a high signal on RDNn indicates the receipt of a negative pulse on RTIPn/RRINGn.
The output data at RDn or RDPn/RDNn are clocked out on the falling edges of RCLK when the CLKE input is low, or are clocked out on the rising edges of RCLK when CLKE is high.
In Dual Rail Mode without clock recovery, these pins output the raw RZ sliced data. In this data recovery mode, the active polarity of RDPn/RDNn is determined by pin CLKE. When pin CLKE is low, RDPn/RDNn is active low. When pin CLKE is high, RDPn/RDNn is active high.
In hardware mode, RDn or RDPn/RDNn will remain active during LOS. In host mode, these pins will either remain active or insert alarm indication signal (AIS) into the receive path, determined by bit AISE in register GCF.
RDn or RDPn/RDNn is set into high-Z when the corresponding receiver is powered down.</td></tr>
</table>

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>RCLK0
RCLK1
RCLK2
RCLK3</td><td>O

High-Z</td><td>39
32
78
71</td><td>P1
M1
M14
P14</td><td>RCLKn: Receive Clock for Channel 0~3
In clock recovery mode, this pin outputs the recovered clock from signal received on RTIPn/RRINGn. The received data are clocked out of the device on the rising edges of RCLKn if pin CLKE is high, or on falling edges of RCLKn if pin CLKE is low.
In data recovery mode, RCLKn is the output of an internal exclusive OR (XOR) which is connected with RDPn and RDNn. The clock is recovered from the signal on RCLKn.
If Receiver n is powered down, the corresponding RCLKn is in high-Z.</td></tr>
<tr><td>MCLK</td><td>I</td><td>10</td><td>E1</td><td>MCLK: Master Clock
This is an independent, free running reference clock. A clock of 2.048 MHz is supplied to this pin as the clock reference of the device for normal operation.
In receive path, when MCLK is high, the device slices the incoming bipolar line signal into RZ pulse (Data Recovery mode). When MCLK is low, all the receivers are powered down, and the output pins RCLKn, RDPn and RDNn are switched to high-Z.
In transmit path, the operation mode is decided by the combination of MCLK and TCLKn (see TCLKn pin description for details).
NOTE: Wait state generation via RDY/$\overline{ACK}$ is not available if MCLK is not provided.</td></tr>
<tr><td>LOS0
LOS1
LOS2
LOS3</td><td>O</td><td>42
35
75
68</td><td>K4
K3
K12
K11</td><td>LOSn: Loss of Signal Output for Channel 0~3
A high level on this pin indicates the loss of signal when there is no transition over a specified period of time or no enough ones density in the received signal. The transition will return to low automatically when there is enough transitions over a specified period of time with a certain ones density in the received signal. The LOS assertion and desertion criteria are described in 2.3.4 Loss of Signal (LOS) Detection.</td></tr>
<tr><td colspan="5">Hardware/Host Control Interface</td></tr>
<tr><td>MODE2</td><td>I

(Pulled to VDDIO/2)</td><td>11</td><td>E2</td><td>MODE2: Control Mode Select 2
The signal on this pin determines which control mode is selected to control the device:
<table>
<tr><th>MODE2</th><th>Control Interface</th></tr>
<tr><td>Low</td><td>Hardware Mode</td></tr>
<tr><td>VDDIO/2</td><td>Serial Host Interface</td></tr>
<tr><td>High</td><td>Parallel Host Interface</td></tr>
</table>
Hardware control pins include MODE[2:0], LP[3:0], CODE, CLKE, JAS and OE.
Serial host Interface pins include $\overline{CS}$, SCLK, SDI, SDO and $\overline{INT}$.
Parallel host Interface pins include $\overline{CS}$, A[4:0], D[7:0], $\overline{WR}$/$\overline{DS}$, $\overline{RD}$/R/$\overline{W}$, ALE/$\overline{AS}$, $\overline{INT}$ and RDY/$\overline{ACK}$. The device supports multiple parallel host interface as follows (refer to MODE1 and MODE0 pin descriptions below for details):
<table>
<tr><th>MODE[2:0]</th><th>Host Interface</th></tr>
<tr><td>100</td><td>Non-multiplexed Motorola Interface</td></tr>
<tr><td>101</td><td>Non-multiplexed Intel Interface</td></tr>
<tr><td>110</td><td>Multiplexed Motorola Interface</td></tr>
<tr><td>111</td><td>Multiplexed Intel Interface</td></tr>
</table></td></tr>
<tr><td>MODE1</td><td>I</td><td>43</td><td>K2</td><td>MODE1: Control Mode Select 1
In parallel host mode, the parallel interface operates with separate address bus and data bus when this pin is low, and operates with multiplexed address and data bus when this pin is high.
In serial host mode or hardware mode, this pin should be grounded.</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
MODE0/CODE	I	88	H12	**MODE0: Control Mode Select 0** In parallel host mode, the parallel host interface is configured for Motorola compatible hosts when this pin is low, or for Intel compatible hosts when this pin is high. **CODE: Line Code Rule Select** In hardware control mode, the HDB3 encoder/decoder is enabled when this pin is low, and AMI encoder/decoder is enabled when this pin is high. The selections affect all the channels. In serial host mode, this pin should be grounded.
$\overline{CS}$/JAS	I (Pulled to VDDIO/2)	87	J11	**$\overline{CS}$: Chip Select (Active Low)** In host mode, this pin is asserted low by the host to enable host interface. A high to low transition must occur on this pin for each read/write operation and the level must not return to high until the operation is over. **JAS: Jitter Attenuator Select** In hardware control mode, this pin globally determines the Jitter Attenuator position: JAS: Low — JA in transmit path; VDDIO/2 — JA not used; High — JA in receive path
SCLK/ALE/$\overline{AS}$	I	86	J12	**SCLK: Shift Clock** In serial host mode, the signal on this pin is the shift clock for the serial interface. Data on pin SDO is clocked out on falling edges of SCLK if pin CLKE is high, or on rising edges of SCLK if pin CLKE is low. Data on pin SDI is always sampled on rising edges of SCLK. **ALE: Address Latch Enable** In parallel Intel multiplexed host mode, the address on AD[4:0] is sampled into the device on the falling edges of ALE (signals on AD[7:5] are ignored). In non-multiplexed host mode, ALE should be pulled high. **$\overline{AS}$: Address Strobe (Active Low)** In parallel Motorola multiplexed host mode, the address on AD[4:0] is latched into the device on the falling edges of $\overline{AS}$ (signals on AD[7:5] are ignored). In non-multiplexed host mode, $\overline{AS}$ should be pulled high. **NOTE**: This pin is ignored in hardware control mode.
$\overline{RD}$/R/$\overline{W}$	I	85	J13	**$\overline{RD}$: Read Strobe (Active Low)** In parallel Intel multiplexed or non-multiplexed host mode, this pin is active low for read operation. **R/$\overline{W}$: Read/Write Select** In parallel Motorola multiplexed or non-multiplexed host mode, the pin is active low for write operation and high for read operation. **NOTE**: This pin is ignored in hardware control mode.

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
SDI/$\overline{WR}$/$\overline{DS}$	I	84	J14	**SDI: Serial Data Input** In serial host mode, this pin input the data to the serial interface. Data on this pin is sampled on the rising edges of SCLK. **$\overline{WR}$: Write Strobe (Active Low)** In parallel Intel host mode, this pin is active low during write operation. The data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on the rising edges of $\overline{WR}$. **$\overline{DS}$: Data Strobe (Active Low)** In parallel Motorola host mode, this pin is active low. During a write operation (R/$\overline{W}$ = 0), the data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on the rising edges of $\overline{DS}$. During a read operation (R/$\overline{W}$ = 1), the data is driven to D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) by the device on the rising edges of $\overline{DS}$. In parallel Motorola non-multiplexed host mode, the address information on the 5 bits of address bus A[4:0] are latched into the device on the falling edges of $\overline{DS}$. **NOTE**: This pin is ignored in hardware control mode.
SDO/RDY/$\overline{ACK}$	O	83	K14	**SDO: Serial Data Output** In serial host mode, the data is output on this pin. In serial write operation, SDO is always in high-Z. In serial read operation, SDO is in high-Z only when SDI is in address/command byte. Data on pin SDO is clocked out of the device on the falling edges of SCLK if pin CLKE is high, or on the rising edges of SCLK if pin CLKE is low. **RDY: Ready Output** In parallel Intel host mode, the high level of this pin reports to the host that bus cycle can be completed, while low reports the host must insert wait states. **$\overline{ACK}$: Acknowledge Output (Active Low)** In parallel Motorola host mode, the low level of this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation.
$\overline{INT}$	O Open Drain	82	K13	**$\overline{INT}$: Interrupt (Active Low)** This is the open drain, active low interrupt output. Three sources may cause the interrupt. Refer to 2.19 Interrupt Handling for details.
D7/AD7 D6/AD6 D5/AD5 D4/AD4 LP3/D3/AD3 LP2/D2/AD2 LP1/D1/AD1 LP0/D0/AD0	I/O High-Z	28 27 26 25 24 23 22 21	K1 J1 J2 J3 J4 H2 H3 G2	**LPn: Loopback Select 3~0** In hardware control mode, pin LPn configures the corresponding channel in different loopback mode, as follows: LPn: Low → Remote Loopback LPn: VDDIO/2 → No loopback LPn: High → Analog Loopback Refer to 2.12 Loopback Mode for details. In hardware control mode, D4 to D7 should be tied to VDDIO/2. **Dn: Data Bus 7~0** In non-multiplexed host mode, these pins are the bi-directional data bus. **ADn: Address/Data Bus 7~0** In multiplexed host mode, these pins are the multiplexed bi-directional address/data bus. In serial host mode, these pins should be grounded.

Table-1 Pin Description (Continued)

<table>
<tr><th rowspan="2">Name</th><th rowspan="2">Type</th><th colspan="2">Pin No.</th><th rowspan="2">Description</th></tr>
<tr><th>TQFP144</th><th>PBGA160</th></tr>
<tr><td>A4
MC3/A3
MC2/A2
MC1/A1
MC0/A0</td><td>I</td><td>12
13
14
15
16</td><td>F4
F3
F2
F1
G3</td><td>MCn: Performance Monitor Configuration 3~0
In hardware control mode, A4 must be connected to GND. MC[3:0] are used to select one transmitter or receiver of channel 1 to 4 for non-intrusive monitoring. Channel 0 is used as the monitoring channel. If a transmitter is monitored, signals on the corresponding pins TTIPn and TRINGn are internally transmitted to RTIP0 and RRING0. If a receiver is monitored, signals on the corresponding pins RTIPn and RRINGn are internally transmitted to RTIP0 and RRING0. The clock and data recovery circuit in Receiver 0 can then output the monitored clock to pin RCLK0 as well as the monitored data to RDP0 and RDN0 pins. The signals monitored by channel 0 can be routed to TTIP0/TRING0 by activating Remote Loopback in this channel.
Performance Monitor Configuration determined by MC[3:0] is shown below. Note that if MC[2:0] = 000, the device is in normal operation of all the channels.
<table>
<tr><th>MC[3:0]</th><th>Monitoring Configuration</th></tr>
<tr><td>0000</td><td>Normal operation without monitoring</td></tr>
<tr><td>0001</td><td>Monitor Receiver 1</td></tr>
<tr><td>0010</td><td>Monitor Receiver 2</td></tr>
<tr><td>0011</td><td>Monitor Receiver 3</td></tr>
<tr><td>0100</td><td rowspan="4">Reserved</td></tr>
<tr><td>0101</td></tr>
<tr><td>0110</td></tr>
<tr><td>0111</td></tr>
<tr><td>1000</td><td>Normal operation without monitoring</td></tr>
<tr><td>1001</td><td>Monitor Transmitter 1</td></tr>
<tr><td>1010</td><td>Monitor Transmitter 2</td></tr>
<tr><td>1011</td><td>Monitor Transmitter 3</td></tr>
<tr><td>1100</td><td rowspan="4">Reserved</td></tr>
<tr><td>1101</td></tr>
<tr><td>1110</td></tr>
<tr><td>1111</td></tr>
</table>
An: Address Bus 4~0
When pin MODE1 is low, the parallel host interface operates with separate address and data bus. In this mode, the signal on this pin is the address bus of the host interface.</td></tr>
<tr><td>OE</td><td>I</td><td>114</td><td>E14</td><td>OE: Output Driver Enable
Pulling this pin low can drive all driver output into high-Z for redundancy application without external mechanical relays. In this condition, all other internal circuits remain active.</td></tr>
<tr><td>CLKE</td><td>I</td><td>115</td><td>E13</td><td>CLKE: Clock Edge Select
The signal on this pin determines the active edge of RCLKn and SCLK in clock recovery mode, or determines the active level of RDPn and RDNn in the data recovery mode. See 2.2 Clock Edges on page 14 for details.</td></tr>
<tr><td colspan="5">JTAG Signals</td></tr>
<tr><td>$\overline{\text{TRST}}$</td><td>I
Pull-up</td><td>95</td><td>G12</td><td>$\overline{\text{TRST}}$: JTAG Test Port Reset (Active Low)
This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pull-up resistor and can be left disconnected.</td></tr>
<tr><td>TMS</td><td>I
Pull-up</td><td>96</td><td>F11</td><td>TMS: JTAG Test Mode Select
The signal on this pin controls the JTAG test performance and is clocked into the device on the rising edges of TCK. This pin has an internal pull-up resistor and it can be left disconnected.</td></tr>
<tr><td>TCK</td><td>I</td><td>97</td><td>F14</td><td>TCK: JTAG Test Clock
This pin input the clock of the JTAG Test. The data on TDI and TMS are clocked into the device on the rising edges of TCK, while the data on TDO is clocked out of the device on the falling edges of TCK. This pin should be connected to GNDIO or VDDIO pin when unused.</td></tr>
</table>

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
TDO	O High-Z	98	F13	**TDO: JTAG Test Data Output** This pin output the serial data of the JTAG Test. The data on TDO is clocked out of the device on the falling edges of TCK. TDO is a high-Z output signal. It is active only when scanning of data is out. This pin should be left float when unused.
TDI	I Pull-up	99	F12	**TDI: JTAG Test Data Input** This pin input the serial data of the JTAG Test. The data on TDI is clocked into the device on the rising edges of TCK. This pin has an internal pull-up resistor and it can be left disconnected.
Power Supplies and Grounds				
VDDIO	-	17 92	G1 G14	3.3 V I/O Power Supply
GNDIO	-	1 2 7 8 9 18 91 100 101 102 107 108 109 144	B1 B2 B3 B12 B13 B14 D1 D2 D3 D12 D13 D14 G4 G11	I/O GND
VDDT	-	44 53 56 65 116 125 128 137	A4, A11 B4, B11 C4, C11 D4, D11 L4, L11 M4, M11 N4, N11 P4, P11	**3.3 V/5 V Power Supply for Transmitter Driver** All VDDT pins must be connected to 3.3 V or all VDDT must be connected to 5 V. It is not allowed to leave any of the VDDT pins open (not-connected) even if the channel is not used.
GNDT	-	47 50 59 62 119 122 131 134	A6, A9 B6, B9 C6, C9 D6, D9 L6, L9 M6, M9 N6, N9 P6, P9	Analog GND for Transmitter Driver
VDDD	-	19	H1	3.3 V Digital Core Power Supply
VDDA	-	90	H14	3.3 V Analog Core Power Supply
GNDD	-	20	H4	Digital Core GND
GNDA	-	89	H11	Analog Core GND

Table-1 Pin Description (Continued)

Name	Type	Pin No.		Description
		TQFP144	PBGA160	
Others				
IC	-	93 94	G13 H13	**IC: Internal Connection** Internal use. Leave it open for normal operation.
DNC	-	3 4 5 6 103 104 105 106 110 111 112 113 117 118 120 121 123 124 126 127 129 130 132 133 135 136 138 139 140 141 142 143	A1 A2 A3 A5 A7 A8 A10 A12 A13 A14 B5 B7 B8 B10 C1 C2 C3 C5 C7 C8 C10 C12 C13 C14 D5 D7 D8 D10 E3 E4 E11 E12	**DNC: Do Not Connect**

2 FUNCTIONAL DESCRIPTION

2.1 OVERVIEW

The IDT82V2054 is a fully integrated quad short-haul line interface unit, which contains four transmit and receive channels for use in E1 applications. The receiver performs clock and data recovery. As an option, the raw sliced data (no retiming) can be output to the system. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance. A selectable jitter attenuator may be placed in the receive path or the transmit path. Moreover, multiple testing functions, such as error detection, loopback and JTAG boundary scan are also provided. The device is optimized for flexible software control through a serial or parallel host mode interface. Hardware control is also available. Figure-1 on page 1 shows one of the four identical channels operation.

2.1.1 SYSTEM INTERFACE

The system interface of each channel can be configured to operate in different modes:

1. *Single rail interface with clock recovery.*
2. *Dual rail interface with clock recovery.*
3. *Dual rail interface with data recovery (that is, with raw data slicing only and without clock recovery).*

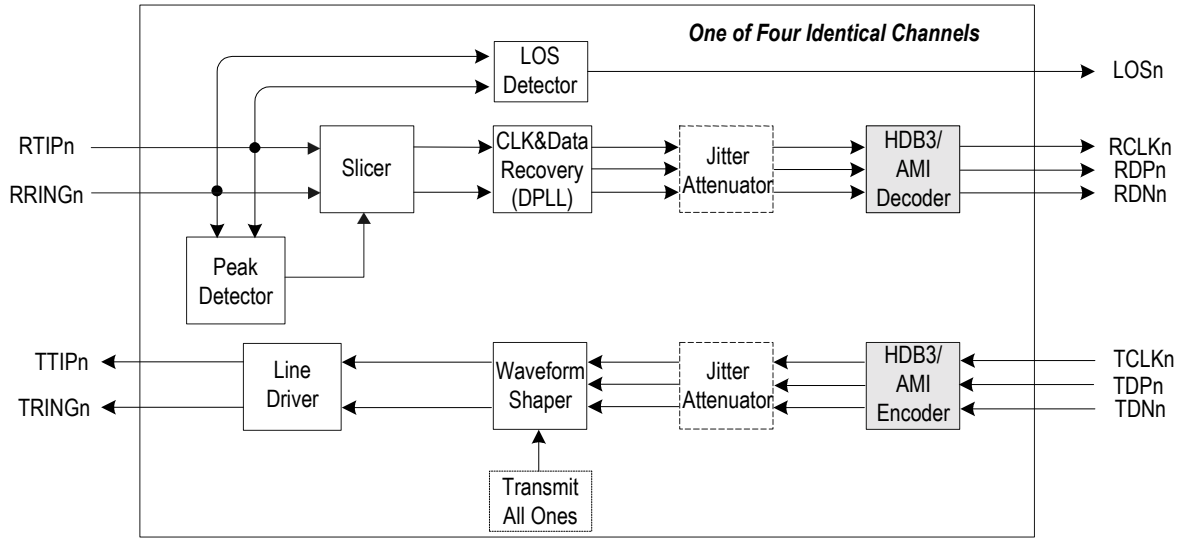
Each signal pin on system side has multiple functions depending on which operation mode the device is in.

The Dual Rail interface consists of TDPn[1], TDNn, TCLKn, RDPn, RDNn and RCLKn. Data transmitted from TDPn and TDNn appears on TTIPn and TRINGn at the line interface; data received from the RTIPn and RRINGn at the line interface are transferred to RDPn and RDNn while the recovered clock extracting from the received data stream outputs on RCLKn. In Dual Rail operation, the clock/data recovery mode is selectable. Dual Rail interface with clock recovery shown in Figure-4 is a default configuration mode. Dual Rail interface with data recovery is shown in Figure-5. Pin RDPn and RDNn, in this condition, are raw RZ slice output and internally connected to an EXOR which is fed to the RCLKn output for external clock recovery applications.

In Single Rail mode, data transmitted from TDn appears on TTIPn and TRINGn at the line interface. Data received from the RTIPn and RRINGn at the line interface appears on RDn while the recovered clock extracting from the received data stream outputs on RCLKn. When the device is in single rail interface, the selectable AMI or HDB3 line encoder/decoder is available and any code violation in the received data will be indicated at the CVn pin. The Single Rail mode has 2 sub-modes: Single Rail Mode 1 and Single Rail Mode 2. Single Rail Mode 1, whose interface is composed of TDn, TCLKn, RDn, CVn and RCLKn, is realized by pulling pin TDNn high for more than 16 consecutive TCLK cycles. Single Rail Mode 2, whose interface is composed of TDn, TCLKn, RDn, CVn, RCLKn and BPVIn, is realized by setting bit CRS in register **e-CRS**[2] and bit SING in register **e-SING**. The difference between them is that, in the latter mode bipolar violation can be inserted via pin BPVIn if AMI line code is selected.

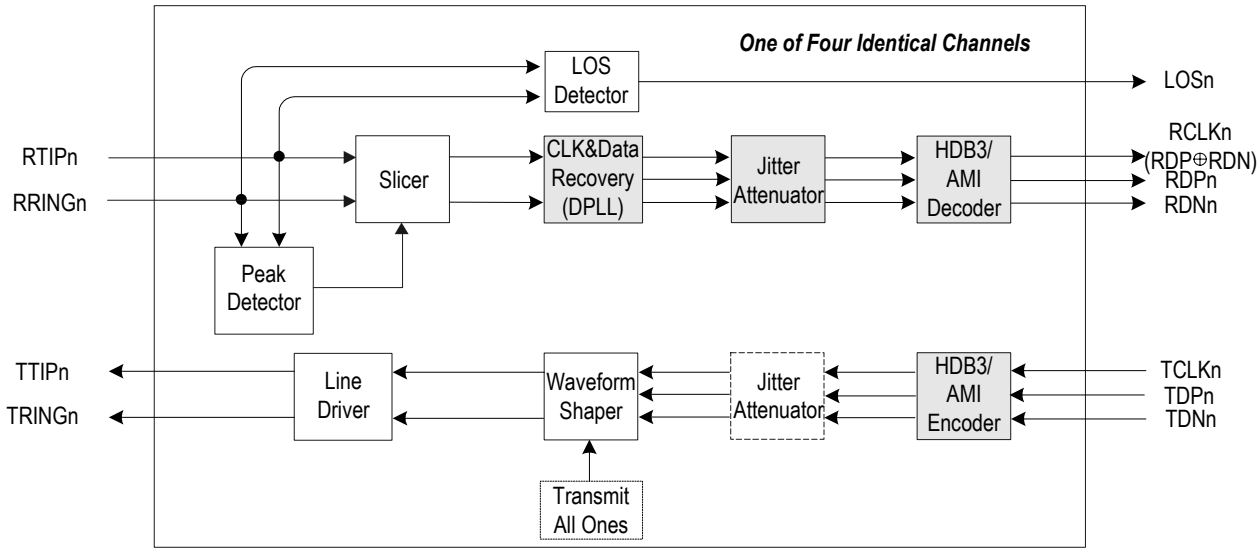
The configuration of the Hardware Mode System Interface is summarized in Table-2. The configuration of the Host (Software) Mode System Interface is summarized Table-3.

1. The footprint 'n' (n = 0 - 3) indicates one of the four channels.
2. The first letter 'e-' indicates expanded register.



Note: The grey blocks are bypassed and the dotted blocks are selectable.

Figure-4 Dual Rail Interface with Clock Recovery



Note: The grey blocks are bypassed and the dotted blocks are selectable

Figure-5 Dual Rail Interface with Data Recovery

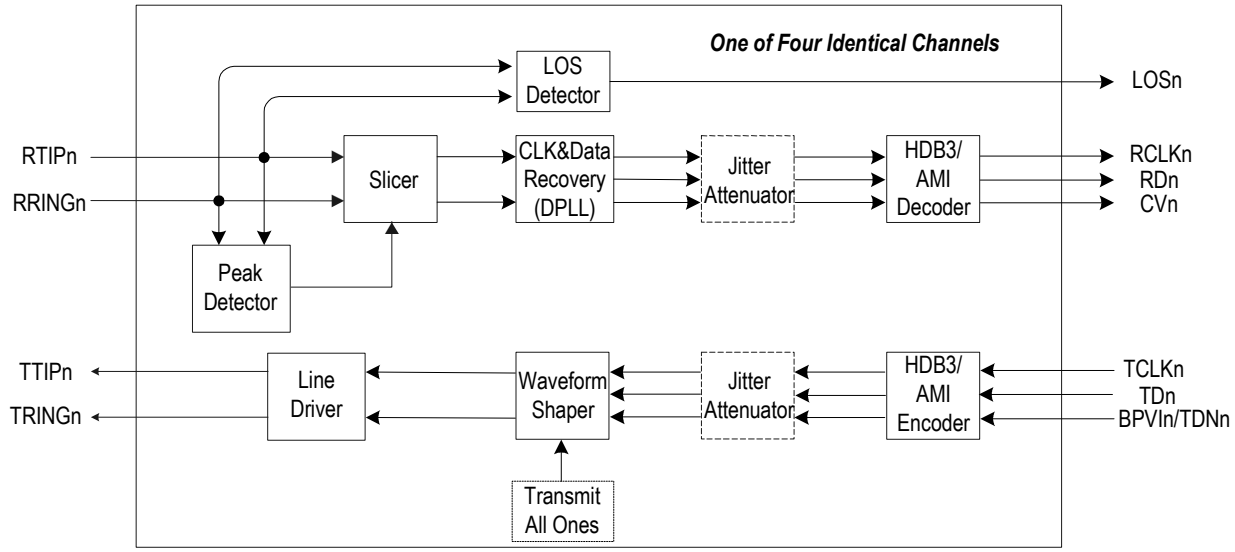


Figure-6 Single Rail Mode

Table-2 System Interface Configuration (In Hardware Mode)

Pin MCLK	Pin TDNn	Interface
Clocked	High (≥ 16 MCLK)	Single Rail Mode 1
Clocked	Pulse	Dual Rail mode with Clock Recovery
High	Pulse	Receive just slices the incoming data. Transmit is determined by the status of TCLKn.
Low	Pulse	Receiver n is powered down. Transmit is determined by the status of TCLKn.

Table-3 System Interface Configuration (In Host Mode)

Pin MCLK	Pin TDNn	CRSn in e-CRS	SINGn in e-SING	Interface
Clocked	High	0	0	Single Rail Mode 1
Clocked	Pulse	0	1	Single Rail Mode 2
Clocked	Pulse	0	0	Dual Rail mode with Clock Recovery
Clocked	Pulse	1	0	Dual Rail mode with Data Recovery
High	Pulse	-	-	Receive just slices the incoming data. Transmit is determined by the status of TCLKn.
Low	Pulse	-	-	Receiver n is powered down. Transmit is determined by the status of TCLKn.

Table-4 Active Clock Edge and Active Level

Pin CLKE	Pin RDn/RDPn and CVn/RDNn			Pin SDO	
	Clock Recovery		Slicer Output		
High	RCLKn 	Active High	Active High	SCLK 	Active High
Low	RCLKn 	Active High	Active Low	SCLK 	Active High

2.2 CLOCK EDGES

The active edge of RCLKn and SCLK are selectable. If pin CLKE is high, the active edge of RCLKn is the rising edge, as for SCLK, that is falling edge. On the contrary, if CLKE is low, the active edge of RCLK is the falling edge and that of SCLK is rising edge. Pins RDn/RDPn, CVn/RDNn and SDO are always active high, and those output signals are clocked out on the active edge of RCLKn and SCLK respectively. See Table-4 Active Clock Edge and Active Level on page 14 for details. However, in dual rail mode without clock recovery, pin CLKE is used to set the active level for RDPn/RDNn raw slicing output: High for active high polarity and low for active low. It should be noted that data on pin SDI are always active high and are sampled on the rising edges of SCLK. The data on pin TDn/TDPn or BPVIn/TDNn are also always active high but is sampled on the falling edges of TCLK, despite the level on CLKE.

2.3 RECEIVER

In receive path, the line signals couple into RRINGn and RTIPn via a transformer and are converted into RZ digital pulses by a data slicer. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. Clock and data are recovered from the received RZ digital pulses by a digital phase-locked loop that provides jitter accommodation. After passing through the selectable jitter attenuator, the recovered data are decoded using HDB3 or AMI line code rules and clocked out of pin RDn in single rail mode, or presented on RDPn/RDNn in an undecoded dual rail NRZ format. Loss of signal, alarm indication signal, line code violation and excessive zeros are detected. These various changes in status may be enabled to generate interrupts.

2.3.1 PEAK DETECTOR AND SLICER

The slicer determines the presence and polarity of the received pulses. In data recovery mode, the raw positive slicer output appears on RDPn while the negative slicer output appears on RDNn. In clock and data recovery mode, the slicer output is sent to Clock and Data Recovery circuit for abstracting retimed data and optional decoding. The slicer circuit has a built-in peak detector from which the slicing threshold is derived. The slicing threshold is default to 50% (typical) of the peak value.

Signals with an attenuation of up to 12 dB (from 2.4 V) can be recovered by the receiver. To provide immunity from impulsive noise, the peak detectors are held above a minimum level of 0.150 V typically, despite the received signal level.

2.3.2 CLOCK AND DATA RECOVERY

The Clock and Data Recovery is accomplished by Digital Phase Locked Loop (DPLL). The DPLL is clocked 16 times of the received clock rate, i.e. 32.768 MHz in E1 mode. The recovered data and clock from DPLL is then sent to the selectable Jitter Attenuator or decoder for further processing.

The clock recovery and data recovery can be selected on a per channel basis by setting bit CRSn in register **e-CRS**. When bit CRSn is defaulted to '0', the corresponding channel operates in data and clock recovery mode. The recovered clock is output on pin RCLKn and retimed NRZ data are output on pin RDPn/RDNn in Dual Rail mode or on RDn in single rail mode. When bit CRSn is set to '1', Dual Rail mode with data recovery is enabled in the corresponding channel and the clock recovery is bypassed. In this condition, the analog line signal are converted to RZ digital bit streams on the RDPn/RDNn pins and internally connected to an EXOR which is fed to the RCLKn output for external clock recovery applications.

If pin MCLK is pulled high, all the receivers will enter the Dual Rail mode with data recovery. In this case, register **e-CRS** is ignored.

2.3.3 HDB3/AMI LINE CODE RULE

Selectable HDB3 and AMI line coding/decoding is provided when the device is configured in Single Rail mode. HDB3 rules is enabled by setting bit CODE in register **GCF** to '0' or pulling pin CODE low. AMI rule is enabled by setting bit CODE in register **GCF** to '1' or pulling pin CODE high. The settings affect all four channels.

Line code rule selection for each channel, if needed, is available by setting bit SINGn in register **e-SING** to '1' (to activate bit CODEn in register **e-CODE**) and programming bit CODEn to select line code rules in the corresponding channel: '0' for B8ZS/HDB3, while '1' for AMI. In this case, the value in bit CODE in register **GCF** or pin CODE for global control is unaffected in the corresponding channel and only affect in other channels.

In dual rail mode, the decoder/encoder are bypassed. Bit CODE in register **GCF**, bit CODEn in register **e-CODE** and pin CODE are ignored.

The configuration of the line code rule is summarized in Table-5.

2.3.4 LOSS OF SIGNAL (LOS) DETECTION

The Loss of Signal Detector monitors the amplitude and density of the received signal on receiver line before the transformer (measured on port A, B shown in Figure-10). The loss condition is reported by pulling pin LOSn high. At the same time, LOS alarm registers track LOS condition. When LOS is detected or cleared, an interrupt will generate if not masked. In host mode, the detection supports ITU G.775 and ETSI 300 233. In hardware mode, it supports the ITU G.775.

Table-6 summarizes the conditions of LOS in clock recovery mode.

During LOS, the RDPn/RDNn output the sliced data when bit AISE in register **GCF** is set to '0' or output all ones as AIS (alarm indication signal) when bit AISE is set to '1'. The RCLKn is replaced by MCLK only if the bit AISE is set.

Table-5 Configuration of the Line Code Rule

Hardware Mode	
CODE	**Line Code Rule**
Low	All channels in HDB3
High	All channels in AMI

Host Mode			
CODE in GCF	**CODEn in e-CODE**	**SINGn in e-SING**	**Line Code Rule**
0	0/1	0	All channels in HDB3
0	0	1	
1	0/1	0	All channels in AMI
1	1	1	
0	1	1	CHn in AMI
1	0	1	CHn in HDB3

Table-6 LOS Condition in Clock Recovery Mode

		Standard		Signal on LOSn
		G.775	**ETSI 300 233**	
LOS Detected	**Continuous Intervals**	32	2048 (1 ms)	High
	Amplitude[1]	below typical 200 mVp	below typical 200 mVp	
LOS Cleared	**Density**	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros	Low
	Amplitude[1]	exceed typical 250 mVp	exceed typical 250 mVp	

1. LOS levels at device (RTIPn, RRINGn) with all ones signal. For more detail regarding the LOS parameters, please refer to Receiver Characteristics on page 45.

2.3.5 ALARM INDICATION SIGNAL (AIS) DETECTION

Alarm Indication Signal is available only in host mode with clock recovery, as shown in Table-7.

Table-7 AIS Condition

	ITU G.775 (Register LAC defaulted to '0')	**ETSI 300 233 (Register LAC set to '1')**
AIS Detected	Less than 3 zeros contained in each of two consecutive 512-bit stream are received	Less than 3 zeros contained in a 512-bit stream are received
AIS Cleared	3 or more zeros contained in each of two consecutive 512-bit stream are received	3 or more zeros contained in a 512-bit stream are received

2.3.6 ERROR DETECTION

The device can detect excessive zeros, bipolar violation and HDB3 code violation, as shown in Figure-7 and Figure-8. All the three kinds of errors are reported in both host mode and hardware mode with HDB3 line code rule used. In host mode, the **e-CZER** and **e-CODV** are used to determine whether excessive zeros and code violation are reported respectively. When the device is configured in AMI decoding mode, only bipolar violation can be reported.

The error detection is available only in single rail mode in which the pin CVn/RDNn is used as error report output (CVn pin).

The configuration and report status of error detection are summarized in Table-8.

Table-8 Error Detection

Hardware Mode	
Line Code	**Pin CVn Reports**
AMI	Bipolar Violation
HDB3	Bipolar Violation + Code Violation + Excessive Zeros

Host Mode			
Line Code	**CODVn in e-CODV**	**CZERn in e-CZER**	**Pin CVn Reports**
AMI	-	-	Bipolar Violation
HDB3	0	0	Bipolar Violation + Code Violation
	0	1	Bipolar Violation + Code Violation + Excessive Zeros
	1	0	Bipolar Violation
	1	1	Bipolar Violation + Excessive Zeros

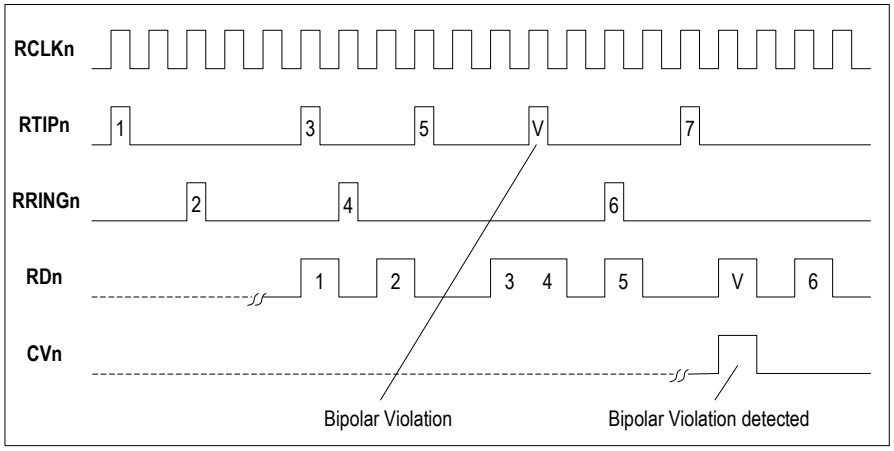


Figure-7 AMI Bipolar Violation

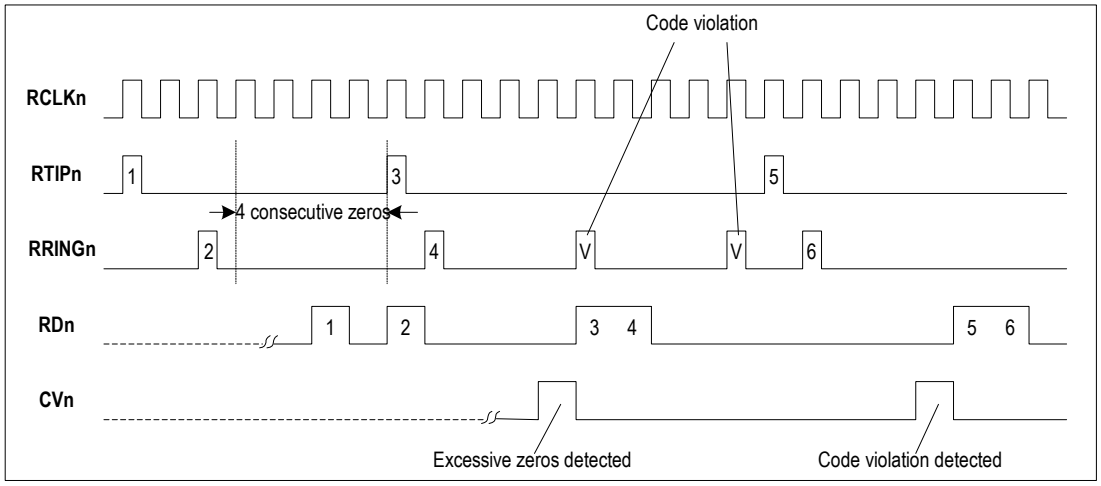


Figure-8 HDB3 Code Violation & Excessive Zeros

2.4 TRANSMITTER

In transmit path, data in NRZ format are clocked into the device on TDn and encoded by AMI or HDB3 line code rules when single rail mode is configured or pre-encoded data in NRZ format are input on TDPn and TDNn when dual rail mode is configured. The data are sampled into the device on falling edges of TCLKn. Jitter attenuator, if enabled, is provided with a FIFO through which the data to be transmitted are passing. A low jitter clock is generated by an integral digital phase-locked loop and is used to read data from the FIFO. The shape of the pulses should meet the E1 pulse template after the signal passes through different cable lengths or types. Bipolar violation, for diagnosis, can be inserted on pin BPVIn if AMI line code rule is enabled.

2.4.1 WAVEFORM SHAPER

E1 pulse template, specified in ITU-T G.703, is shown in Figure-9. The device has built-in transmit waveform templates for cable of 75 Ω or 120 Ω.

The built-in waveform shaper uses an internal high frequency clock which is 16XMCLK as the clock reference. This function will be bypassed when MCLK is unavailable.

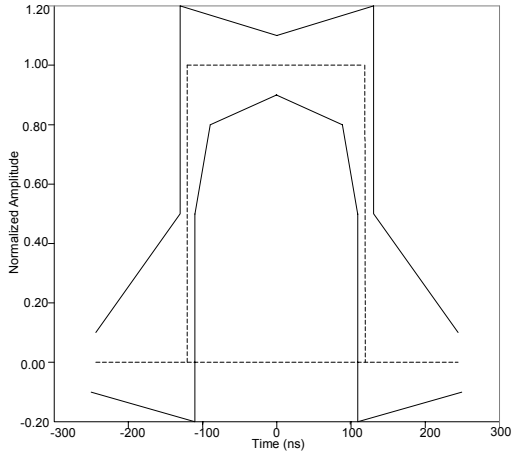


Figure-9 CEPT Waveform Template

2.4.2 BIPOLAR VIOLATION INSERTION

When configured in Single Rail Mode 2 with AMI line code enabled, pin TDNn/BPVIn is used as BPVI input. A low-to-high transition on this pin inserts a bipolar violation on the next available mark in the transmit data stream. Sampling occurs on the falling edges of TCLK. But in TAOS (Transmit All Ones) with Analog Loopback and Remote Loopback, the BPVI is disabled. In TAOS with Digital Loopback, the BPVI is looped back to the system side, so the data to be transmitted on TTINGn and TRINGn are all ones with no bipolar violation.

2.5 JITTER ATTENUATOR

The jitter attenuator can be selected to work either in transmit path or in receive path or not used. The selection is accomplished by setting pin JAS in hardware mode or configuring bits JACF[1:0] in register **GCF** in host mode which affects all four channels.

For applications which require line synchronization, the line clock needed to be extracted for the internal synchronization, the jitter attenuator is set in the receive path. Another use of the jitter attenuator is to provide clock smoothing in the transmit path for applications such as synchronous/asynchronous demultiplexing applications. In these applications, TCLK will have an instantaneous frequency that is higher than the nominal E1 data rate and in order to set the average long-term TCLK frequency within the transmit line rate specifications, periods of TCLK are suppressed (gapped).

The jitter attenuator integrates a FIFO which can accommodate a gapped TCLK. In host mode, the FIFO length can be 32 X 2 or 64 X 2 bits by programming bit JADP in **GCF**. In hardware mode, it is fixed to 64 X 2 bits. The FIFO length determines the maximum permissible gap width (see Table-9 Gap Width Limitation). Exceeding these values will cause FIFO overflow or underflow. The data is 16 or 32 bits' delay through the jitter attenuator in the corresponding transmit or receive path. The constant delay feature is crucial for the applications requiring "hitless" switching.

Table-9 Gap Width Limitation

FIFO Length	Max. Gap Width
64 bit	56 UI
32 bit	28 UI

In host mode, bit JABW in GCF determines the jitter attenuator 3 dB corner frequency (fc). In hardware mode, the fc is fixed to 1.7 Hz. Generally, the lower the fc is, the higher the attenuation. However, lower fc comes at the expense of increased acquisition time. Therefore, the optimum fc is to optimize both the attenuation and the acquisition time. In addition, the longer FIFO length results in an increased throughput delay and also influences the 3 dB corner frequency. Generally, it's recommended to use the lower corner frequency and the shortest FIFO length that can still meet jitter attenuation requirements.

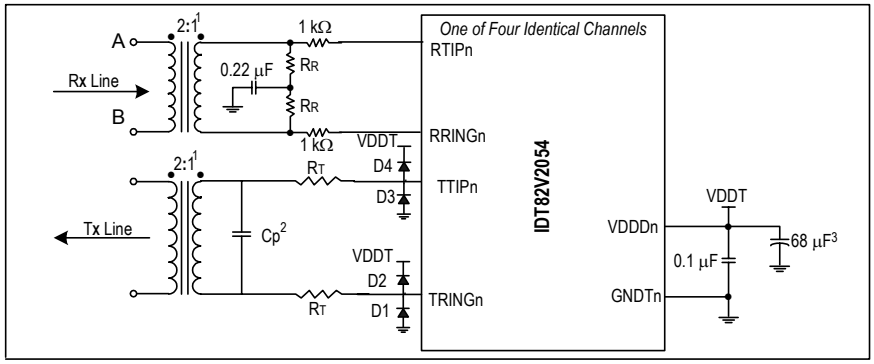
The output jitter meets ITU-T G.736, ITU-T G.742, ITU-T G.783 and ETSI CTR 12/13.

2.6 LINE INTERFACE CIRCUITRY

The transmit and receive interface RTIPn/RRINGn and TTIPn/TRINGn connections provide a matched interface to the cable. Figure-10 shows the appropriate external components to connect with the cable for one transmit/receive channel. Table-10 summarizes the component values based on the specific application.

Table-10 External Components Values

Component	75 Ω Coax	120 Ω Twisted Pair
R_T	9.5 Ω ± 1%	9.5 Ω ± 1%
R_R	9.31 Ω ± 1%	15 Ω ± 1%
Cp	2200 pF	
D1 - D4	Nihon Inter Electronics - EP05Q03L, 11EQS03L, EC10QS04, EC10QS03L;	
	Motorola - MBR0540T1	



NOTE:
1. Pulse T1124 transformer is recommended to be used in Standard (STD) operating temperature range (0°C to 70°C), while Pulse T1114 transformer is recommended to be used in Extended (EXT) operating temperature range is -40°C to +85°C. See Transformer Specifications Table for details.
2. Typical value. Adjust for actual board parasitics to obtain optimum return loss.
3. Common decoupling capacitor for all VDDT and GNDT pins. One per chip.
4. The R_R and R_T values are listed in Table-10.

Figure-10 External Transmit/Receive Line Circuitry

2.7 TRANSMIT DRIVER POWER SUPPLY

All transmit driver power supplies must be 5.0 V or 3.3 V.

Despite the power supply voltage, the 75 Ω/120 Ω lines are driven through a pair of 9.5 Ω series resistors and a 1:2 transformer.

However, in harsh cable environment, series resistors are required to improve the transmit return loss performance and protect the device from surges coupling into the device.

Table-11 Transformer Specifications(1)

Electrical Specification @ 25°C										
Part No.		Turns Ratio (Pri: sec ± 2%)		OCL @ 25°C (mH MIN)		L_L (µH MAX)		$C_{W/W}$ (pF MAX)		Package/Schematic
STD Temp.	EXT Temp.	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	
T1124	T1114	1:2CT	1CT:2	1.2	1.2	.6	.6	35	35	TOU/3

1. Pulse T1124 transformer is recommended to be used in Standard (STD) operating temperature range (0°C to 70°C), while Pulse T1114 transformer is recommended to be used in Extended (EXT) operating temperature range is -40°C to +85°C.

2.8 POWER DRIVER FAILURE MONITOR

An internal power Driver Failure Monitor (DFMON), parallel connected with TTIPn and TRINGn, can detect short circuit failure between TTIPn and TRINGn pins. Bit SCPB in register **GCF** decides whether the output driver short circuit protection is enabled. When the short circuit protection is enabled, the driver output current is limited to a typical value: 180 mAp. Also, register **DF**, **DFI** and **DFM** will be available. When DFMON will detect a short circuit, register **DF** will be set. With a short circuit failure detected, register **DFI** will be set and an interrupt will be generated on pin $\overline{INT}$.

2.9 TRANSMIT LINE SIDE SHORT CIRCUIT FAILURE DETECTION

A pair of 9.5 Ω serial resistors connect with TTIPn and TRINGn pins and limit the output current. In this case, the output current is a limited value which is always lower than the typical line short circuit current 180 mAp, even if the transmit line side is shorted.

Refer to Table-10 External Components Values for details.

2.10 LINE PROTECTION

In transmit side, the Schottky diodes D1~D4 are required to protect the line driver and improve the design robustness. In receive side, the series resistors of 1 kΩ are used to protect the receiver against current surges coupled in the device. The series resistors do not affect the receiver sensitivity, since the receiver impedance is as high as 120 kΩ typically.

2.11 HITLESS PROTECTION SWITCHING (HPS)

The IDT82V2054 transceivers include an output driver with high-Z feature for E1 redundancy applications. This feature reduces the cost of redundancy protection by eliminating external relays. Details of HPS are described in relative Application Note.

2.12 LOOPBACK MODE

The device provides four different diagnostic loopback configurations: Digital Loopback, Analog Loopback, Remote Loopback and Dual Loopback. In host mode, these functions are implemented by programming the registers **DLB**, **ALB** and **RLB** respectively. In hardware mode, only Analog Loopback and Remote Loopback can be selected by pin LPn.

2.12.1 DIGITAL LOOPBACK

By programming the bits of register **DLB**, each channel of the device can be set in Local Digital Loopback. In this configuration, the data and clock to be transmitted, after passing the encoder, are looped back to Jitter Attenuator (if enabled) and decoder in the receive path, then output on RCLKn, RDn/RDPn and CVn/RDNn. The data to be transmitted are still output on TTIPn and TRINGn while the data received on RTIPn and RRINGn are ignored. The Loss Detector is still in use. Figure-11 shows the process.

During Digital Loopback, the received signal on the receive line is still monitored by the LOS Detector (See 2.3.4 Loss of Signal (LOS) Detection for details). In case of a LOS condition and AIS insertion enabled, all ones signal will be output on RDPn/RDNn. With ATAO enabled, all ones signal will be also output on TTIPn/TRINGn. AIS insertion can be enabled by setting AISE bit in register **GCF** and ATAO can be enabled by setting register **ATAO** (default disabled).

2.12.2 ANALOG LOOPBACK

By programming the bits of register **ALB** or pulling pin LPn high, each channel of the device can be configured in Analog Loopback. In this configuration, the data to be transmitted output from the line driver are internally looped back to the slicer and peak detector in the receive path and output on RCLKn, RDn/RDPn and CVn/RDNn. The data to be transmitted are still output on TTIPn and TRINGn while the data received on RTIPn and RRINGn are ignored. The LOS Detector (See 2.3.4 Loss of Signal (LOS) Detection for details) is still in use and monitors the internal looped back data. If a LOS condition on TDPn/TDNn is expected during Analog Loopback, ATAO should be disabled (default). Figure-12 shows the process.

The TTIPn and RTIPn, TRINGn and RRINGn cannot be connected directly to do the external analog loopback test. Line impedance loading is required to conduct the external analog loopback test.

2.12.3 REMOTE LOOPBACK

By programming the bits of register **RLB** or pulling pin LPn low, each channel of the device can be configured in Remote Loopback. In this configuration, the data and clock recovered by the clock and data recovery circuits are looped to waveform shaper and output on TTIPn and TRINGn. The jitter attenuator is also included in loopback when enabled in the transmit or receive path. The received data and clock are still output on RCLKn, RDn/RDPn and CVn/RDNn while the data to be transmitted on TCLKn, TDn/TDPn and BPVIn/TDNn are ignored. The LOs Detector is still in use. Figure-13 shows the process.

2.12.4 DUAL LOOPBACK

Dual Loopback mode is set by setting bit DLBn in register **DLB** and bit RLBn in register **RLB** to '1'. In this configuration, after passing the encoder, the data and clock to be transmitted are looped back to decoder directly and output on RCLKn, RDn/RDPn and CVn/RDNn. The recovered data from RTIPn and RRINGn are looped back to waveform shaper through JA (if selected) and output on TTIPn and TRINGn. The LOS Detector is still in use. Figure-14 shows the process.

2.12.5 TRANSMIT ALL ONES (TAOS)

In hardware mode, the TAOS mode is set by pulling pin TCLKn high for more than 16 MCLK cycles. In host mode, TAOS mode is set by programming register **TAO**. In addition, automatic TAOS signals are inserted by setting register **ATAO** when Loss of Signal occurs. Note that the TAOS generator adopts MCLK as a timing reference. In order to assure that the output frequency is within specified limits, MCLK must have the applicable stability.

The TAOS mode, the TAOS mode with Digital Loopback and the TAOS mode with Analog Loopback are shown in Figure-15, Figure-16 and Figure-17.

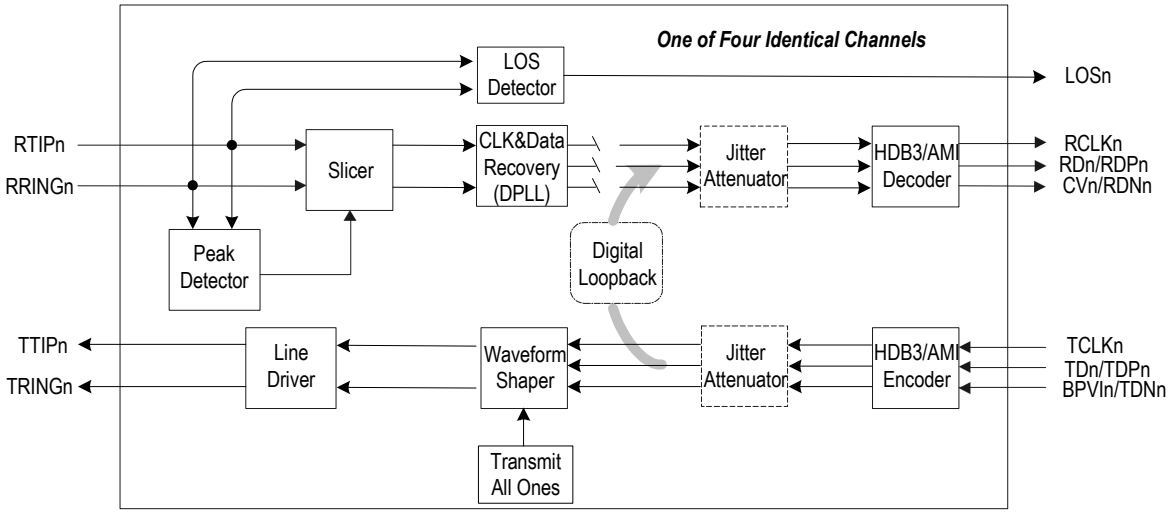


Figure-11 Digital Loopback

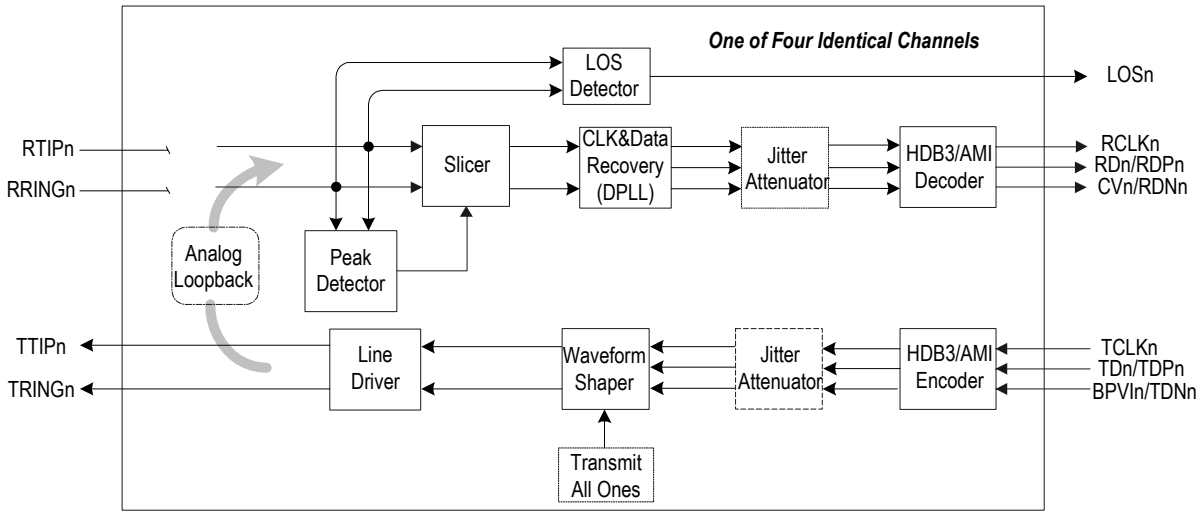


Figure-12 Analog Loopback

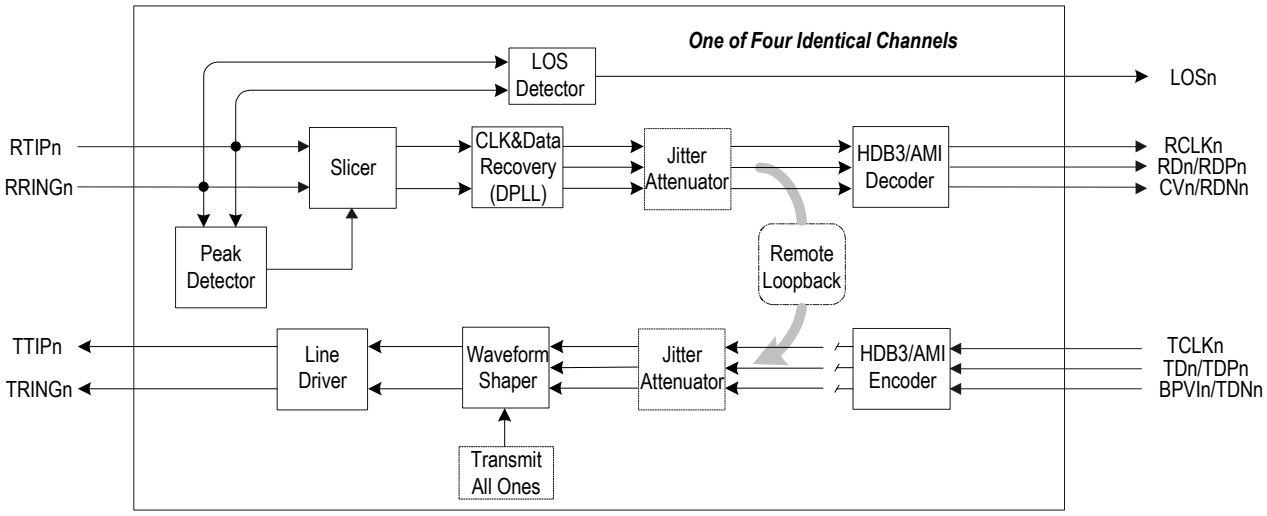


Figure-13 Remote Loopback

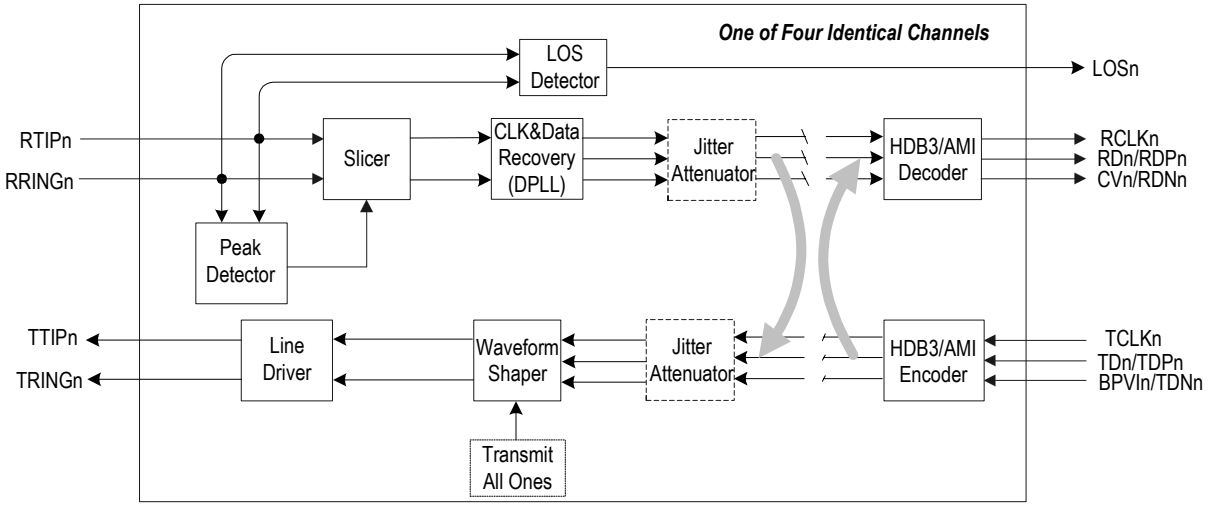


Figure-14 Dual Loopback

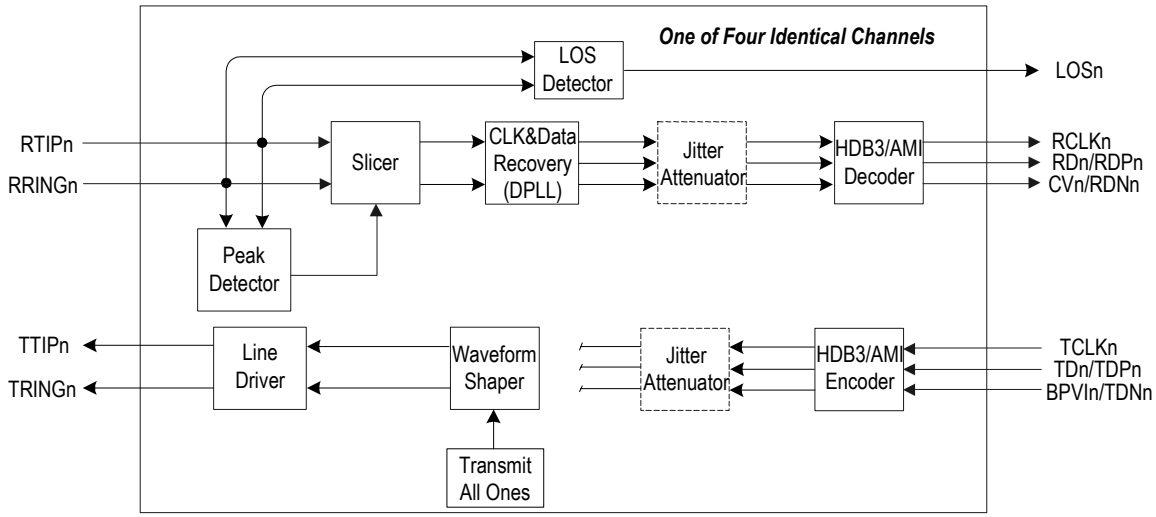


Figure-15 TAOS Data Path

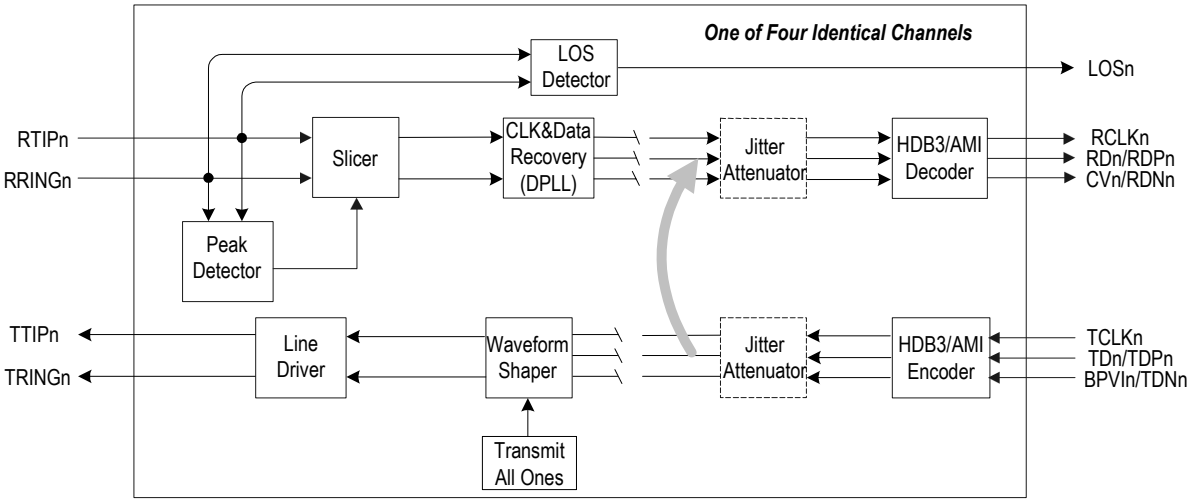


Figure-16 TAOS with Digital Loopback

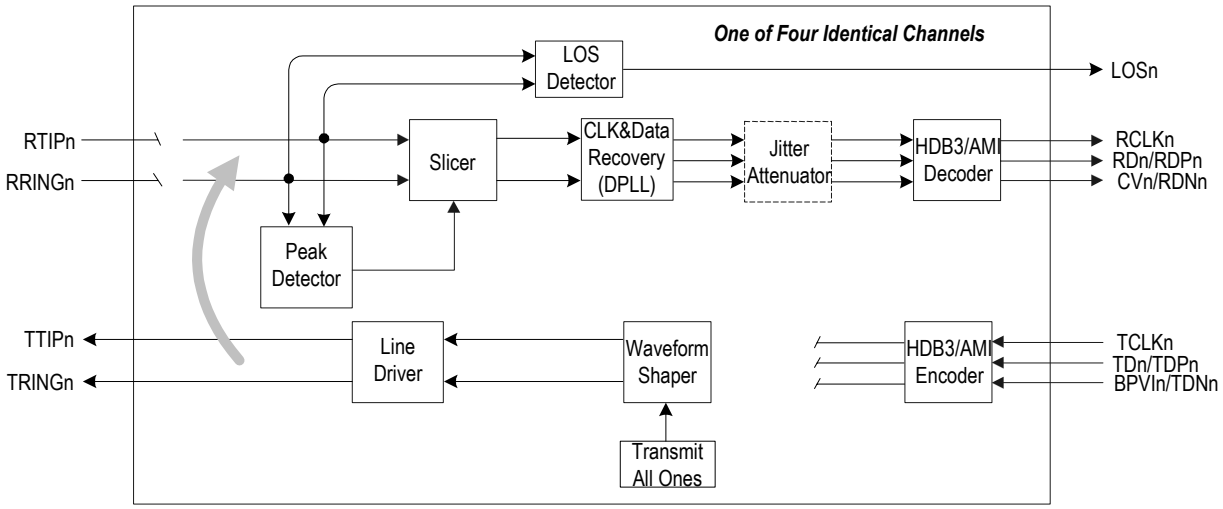


Figure-17 TAOS with Analog Loopback

2.13 G.772 MONITORING

The four channels of IDT82V2054 can all be configured to work as regular transceivers. In applications using only three channels (channels 1 to 3), channel 0 is configured to non-intrusively monitor any of the other channels' inputs or outputs on the line side. The monitoring is non-intrusive per ITU-T G.772. Figure-18 shows the Monitoring Principle. The receive path or transmit path to be monitored is configured by pins MC[3:0] in hardware mode or by register **PMON** in host mode.

The monitored signal goes through the clock and data recovery circuit of channel 0. The monitored clock can output on RCLK0 which can be used as a timing interfaces derived from E1 signal. The monitored data can be observed digitally at the output pins RCLK0, RD0/RDP0 and RDN0. LOS detector is still in use in channel 0 for the monitored signal.

In monitoring mode, channel 0 can be configured in Remote Loopback. The signal which is being monitored will output on TTIP0 and TRING0. The output signal can then be connected to a standard test equipment with an E1 electrical interface for non-intrusive monitoring.

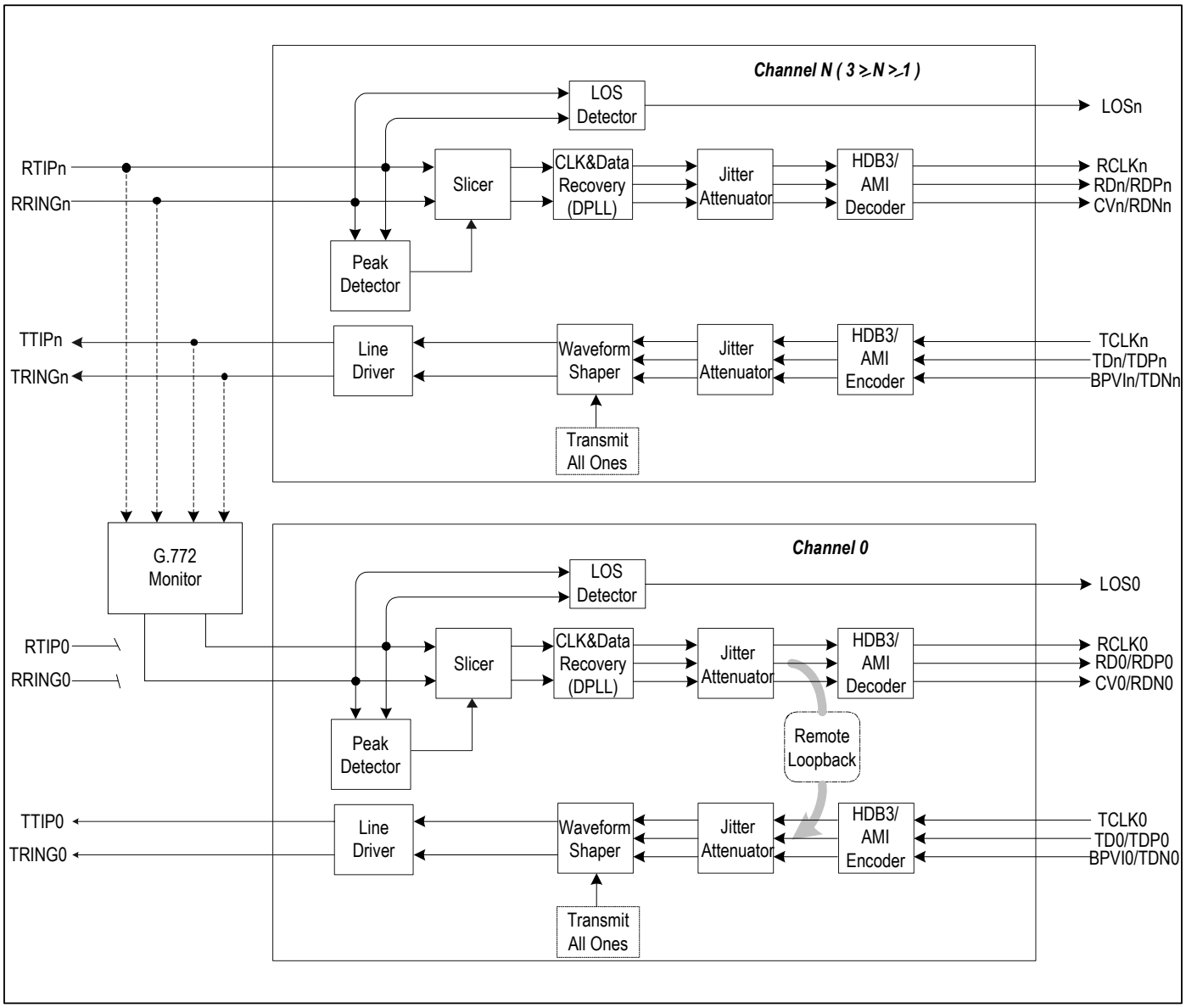


Figure-18 Monitoring Principle

2.14 SOFTWARE RESET

Writing register **RS** will cause software reset by initiating about 1 μs reset cycle. This operation set all the registers to their default value.

2.15 POWER ON RESET

During power up, an internal reset signal sets all the registers to default values. The power-on reset takes at least 10 μs, starting from when the power supply exceeds 2/3 VDDA.

2.16 POWER DOWN

Each transmit channel will be powered down by pulling pin TCLKn low for more than 64 MCLK cycles (if MCLK is available) or about 30 μs (if MCLK is not available). In host mode, each transmit channel will also be powered down by setting bit TPDNn in register **e-TPDN** to '1'.

All the receivers will be powered down when MCLK is low. When MCLK is clocked or high, setting bit RPDNn in register **e-RPDN** to '1' will configure the corresponding receiver to be powered down.

2.17 INTERFACE WITH 5 V LOGIC

The IDT82V2054 can interface directly with 5 V TTL family devices. The internal input pads are tolerant to 5 V output from TTL and CMOS family devices.

2.18 HOST INTERFACE

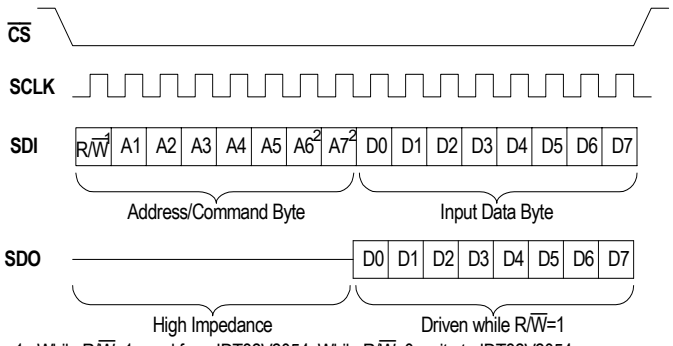
The host interface provides access to read and write the registers in the device. The interface consists of serial host interface and parallel host interface. By pulling pin MODE2 to VDDIO/2 or high, the device can be set to work in serial mode and in parallel mode respectively.

2.18.1 PARALLEL HOST INTERFACE

The interface is compatible with Motorola and Intel host. Pins MODE1 and MODE0 are used to select the operating mode of the parallel host interface. When pin MODE1 is pulled low, the host uses separate address bus and data bus. When high, multiplexed address/data bus is used. When pin MODE0 is pulled low, the parallel host interface is configured for Motorola compatible hosts. When pin MODE0 is pulled high, the parallel host interface is configured for Intel compatible hosts. See Table-1 Pin Description for more details. The host interface pins in each operation mode is tabulated in Table-12:

Table-12 Parallel Host Interface Pins

MODE[2:0]	Host Interface	Generic Control, Data and Output Pin
100	Non-multiplexed Motorola interface	$\overline{CS}$, $\overline{ACK}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$, A[4:0], D[7:0], $\overline{INT}$
101	Non-multiplexed Intel interface	$\overline{CS}$, RDY, $\overline{WR}$, $\overline{RD}$, ALE, A[4:0], D[7:0], $\overline{INT}$
110	Multiplexed Motorola interface	$\overline{CS}$, $\overline{ACK}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$, AD[7:0], $\overline{INT}$
111	Multiplexed Intel interface	$\overline{CS}$, RDY, $\overline{WR}$, $\overline{RD}$, ALE, AD[7:0], $\overline{INT}$



1. While R/$\overline{W}$=1, read from IDT82V2054; While R/$\overline{W}$=0, write to IDT82V2054.
2. Ignored.

Figure-19 Serial Host Mode Timing

2.18.2 SERIAL HOST INTERFACE

By pulling pin MODE2 to VDDIO/2, the device operates in the serial host Mode. In this mode, the registers are accessible through a 16-bit word which contains an 8-bit command/address byte (bit R/$\overline{W}$ and 5-address-bit A1~A5, A6 and A7 bits are ignored) and a subsequent 8-bit data byte (D7~D0), as shown in Figure-19. When bit R/$\overline{W}$ is set to '1', data is read out from pin SDO. When bit R/$\overline{W}$ is set to '0', data on pin SDI is written into the register whose address is indicated by address bits A5~A1.

2.19 INTERRUPT HANDLING

2.19.1 INTERRUPT SOURCES

There are three kinds of interrupt sources:

1. *Status change in register **LOS**. The analog/digital loss of signal detector continuously monitors the received signal to update the specific bit in register **LOS** which indicates presence or absence of a LOS condition.*
2. *Status change in register **DF**. The automatic power driver circuit continuously monitors the output drivers signal to update the specific bit in register **DFM** which indicates presence or absence of an output driver short circuit condition.*
3. *Status change in register **AIS**. The AIS detector monitors the received signal to update the specific bit in register **AIS** which indicates presence or absence of a AIS condition.*

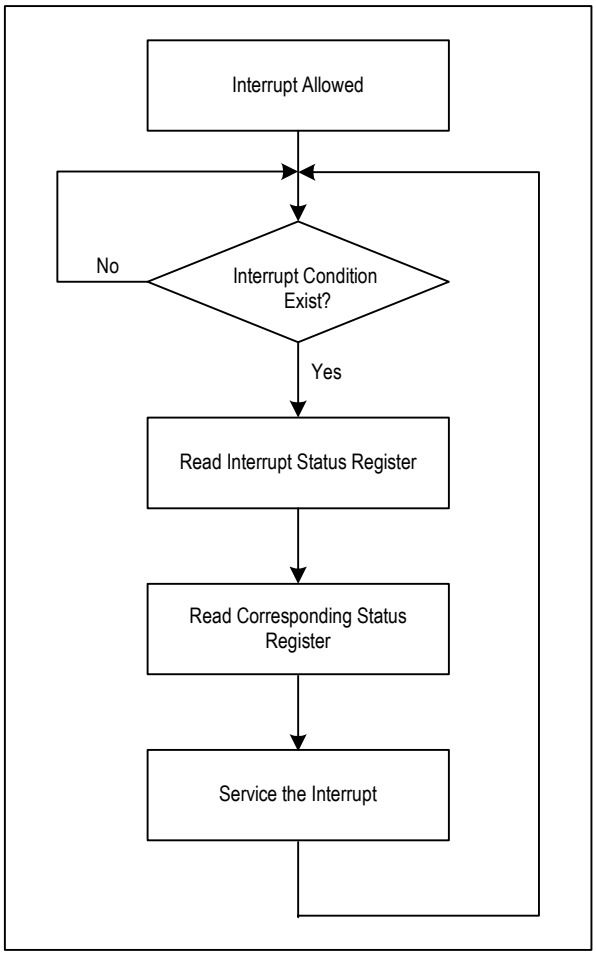


Figure-20 Interrupt Service Routine

2.19.2 INTERRUPT ENABLE

The IDT82V2054 provides a latched interrupt output ($\overline{INT}$) and the four kinds of interrupts are all reported by this pin. When the Interrupt Mask register (**LOSM**, **DFM** and **AISM**) is set to '1', the Interrupt Status register (**LOSI**, **DFI** and **AISI**) is enabled respectively. Whenever there is a transition ('0' to '1' or '1' to '0') in the corresponding status register, the Interrupt Status register will change into '1', which means an interrupt occurs, and there will be a high to low transition on $\overline{INT}$ pin. An external pull-up resistor of approximately 10 kΩ is required to support the wire-OR operation of $\overline{INT}$. When any of the three Interrupt Mask registers is set to '0' (the power-on default value is '0'), the corresponding Interrupt Status register is disabled and the transition on status register is ignored.

2.19.3 INTERRUPT CLEARING

When an interrupt occurs, the Interrupt Status registers: **LOSI**, **DFI** and **AISI**, are read to identify the interrupt source. These registers will be cleared to '0' after the corresponding status registers: **LOS**, **DF** and **AIS** are read. The Status registers will be cleared once the corresponding conditions are met.

Pin $\overline{INT}$ is pulled high when there is no pending interrupt left. The interrupt handling in the interrupt service routine is showed in Figure-20.

3 PROGRAMMING INFORMATION

3.1 REGISTER LIST AND MAP

There are 21 primary registers (including an Address Pointer Control Register and 8 expanded registers in the device).

Whatever the control interface is, 5 address bits are used to set the registers. In non-multiplexed parallel interface mode, the five dedicated address bits are A[4:0]. In multiplexed parallel interface mode, AD[4:0] carries the address information. In serial interface mode, A[5:1] are used to address the register.

The Register **ADDP**, addressed as 11111 or 1F Hex, switches between primary registers bank and expanded registers bank.

By setting the register **ADDP** to 'AAH', the 5 address bits point to the expanded register bank, that is, the expanded registers are available. By clearing the register **ADDP**, the primary registers are available.

3.2 RESERVED AND TEST REGISTERS

Primary Registers, whose address are 10H, 11H, 16H to 1EH, are reserved. Expanded Registers, whose address are 08H to 0FH, are reserved. Expanded registers, whose address are 10H to 1EH, are used for test and must be set to '0'.

When writing to registers with reserved bit locations, the default state must be written to the reserved bits to ensure proper device operation.

Table-13 Primary Register List

Address			Register	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface A7-A0			
00	XX00000	XXX00000	ID	R	Device ID Register
01	XX00001	XXX00001	ALB	R/W	Analog Loopback Configuration Register
02	XX00010	XXX00010	RLB	R/W	Remote Loopback Configuration Register
03	XX00011	XXX00011	TAO	R/W	Transmit All Ones Configuration Register
04	XX00100	XXX00100	LOS	R	Loss of Signal Status Register
05	XX00101	XXX00101	DF	R	Driver Fault Status Register
06	XX00110	XXX00110	LOSM	R/W	LOS Interrupt Mask Register
07	XX00111	XXX00111	DFM	R/W	Driver Fault Interrupt Mask Register
08	XX01000	XXX01000	LOSI	R	LOS Interrupt Status Register
09	XX01001	XXX01001	DFI	R	Driver Fault Interrupt Status Register
0A	XX01010	XXX01010	RS	W	Software Reset Register
0B	XX01011	XXX01011	PMON	R/W	Performance Monitor Configuration Register
0C	XX01100	XXX01100	DLB	R/W	Digital Loopback Configuration Register
0D	XX01101	XXX01101	LAC	R/W	LOS/AIS Criteria Configuration Register
0E	XX01110	XXX01110	ATAO	R/W	Automatic TAOS Configuration Register
0F	XX01111	XXX01111	GCF	R/W	Global Configuration Register
10	XX10000	XXX10000	Reserved		
11	XX10001	XXX10001			
12	XX10010	XXX10010	OE	R/W	Output Enable Configuration Register
13	XX10011	XXX10011	AIS	R	AIS Status Register
14	XX10100	XXX10100	AISM	R/W	AIS Interrupt Mask Register
15	XX10101	XXX10101	AISI	R	AIS Interrupt Status Register
16	XX10110	XXX10110	Reserved		
17	XX10111	XXX10111			
18	XX11000	XXX11000			
19	XX11001	XXX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11111	XXX11111	ADDP	R/W	Address pointer control Register for switching between primary register bank and expanded register bank

Table-14 Expanded (Indirect Address Mode) Register List

Address			Register	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface A7-A0			
00	XX00000	XXX00000	e-SING	R/W	Single Rail Mode Setting Register
01	XX00001	XXX00001	e-CODE	R/W	Encoder/Decoder Selection Register
02	XX00010	XXX00010	e-CRS	R/W	Clock Recovery Enable/Disable Register
03	XX00011	XXX00011	e-RPDN	R/W	Receiver n Powerdown Enable/Disable Register
04	XX00100	XXX00100	e-TPDN	R/W	Transmitter n Powerdown Enable/Disable Register
05	XX00101	XXX00101	e-CZER	R/W	Consecutive Zero Detect Enable/Disable Register
06	XX00110	XXX00110	e-CODV	R/W	Code Violation Detect Enable/Disable Register
07	XX00111	XXX00111	e-EQUA	R/W	Enable Equalizer Enable/Disable Register
08	XX01000	XXX01000	Reserved		
09	XX01001	XXX01001			
0A	XX01010	XXX01010			
0B	XX01011	XXX01011			
0C	XX01100	XXX01100			
0D	XX01101	XXX01101			
0E	XX01110	XXX01110			
0F	XX01111	XXX01111			
10	XX10000	XXX10000	Test		
11	XX10001	XXX10001			
12	XX10010	XXX10010			
13	XX10011	XXX10011			
14	XX10100	XXX10100			
15	XX10101	XXX10101			
16	XX10110	XXX10110			
17	XX10111	XXX10111			
18	XX11000	XXX11000			
19	XX11001	XXX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11111	XXX11111	ADDP	R/W	Address pointer control register for switching between primary register bank and expanded register bank

Table-15 Primary Register Map

Register	Address R/W Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID	00H R Default	ID 7 R 0	ID 6 R 0	ID 5 R 0	ID 4 R 1	ID 3 R 0	ID 2 R 0	ID 1 R 0	ID 0 R 0
ALB	01H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	ALB 3 R/W 0	ALB 2 R/W 0	ALB 1 R/W 0	ALB 0 R/W 0
RLB	02H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	RLB 3 R/W 0	RLB 2 R/W 0	RLB 1 R/W 0	RLB 0 R/W 0
TAO	03H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	TAO 3 R/W 0	TAO 2 R/W 0	TAO 1 R/W 0	TAO 0 R/W 0
LOS	04H R Default	- R 0	- R 0	- R 0	- R 0	LOS 3 R 0	LOS 2 R 0	LOS 1 R 0	LOS 0 R 0
DF	05H R Default	- R 0	- R 0	- R 0	- R 0	DF 3 R 0	DF 2 R 0	DF 1 R 0	DF 0 R 0
LOSM	06H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	LOSM 3 R/W 0	LOSM 2 R/W 0	LOSM 1 R/W 0	LOSM 0 R/W 0
DFM	07H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	DFM 3 R/W 0	DFM 2 R/W 0	DFM 1 R/W 0	DFM 0 R/W 0
LOSI	08H R Default	- R 0	- R 0	- R 0	- R 0	LOSI 3 R 0	LOSI 2 R 0	LOSI 1 R 0	LOSI 0 R 0
DFI	09H R Default	- R 0	- R 0	- R 0	- R 0	DFI 3 R 0	DFI 2 R 0	DFI 1 R 0	DFI 0 R 0
RS	0AH W Default	RS 7 W 1	RS 6 W 1	RS 5 W 1	RS 4 W 1	RS 3 W 1	RS 2 W 1	RS 1 W 1	RS 0 W 1
PMON	0BH R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	MC 3 R/W 0	MC 2 R/W 0	MC 1 R/W 0	MC 0 R/W 0
DLB	0CH R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	DLB 3 R/W 0	DLB 2 R/W 0	DLB 1 R/W 0	DLB 0 R/W 0
LAC	0DH R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	LAC 3 R/W 0	LAC 2 R/W 0	LAC 1 R/W 0	LAC 0 R/W 0
ATAO	0EH R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	ATAO 3 R/W 0	ATAO 2 R/W 0	ATAO 1 R/W 0	ATAO 0 R/W 0
GCF	0FH R/W Default	- R/W 0	AISE R/W 0	SCPB R/W 0	CODE R/W 0	JADP R/W 0	JABW R/W 0	JACF 1 R/W 0	JACF 0 R/W 0

Table-15 Primary Register Map (Continued)

Register	Address R/W Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OE	12 Hex R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	OE 3 R/W 0	OE 2 R/W 0	OE 1 R/W 0	OE 0 R/W 0
AIS	13 Hex R Default	- R 0	- R 0	- R 0	- R 0	AIS 3 R 0	AIS 2 R 0	AIS 1 R 0	AIS 0 R 0
AISM	14 Hex R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	AISM 3 R/W 0	AISM 2 R/W 0	AISM 1 R/W 0	AISM 0 R/W 0
AISI	15 Hex R Default	- R 0	- R 0	- R 0	- R 0	AISI 3 R 0	AISI 2 R 0	AISI 1 R 0	AISI 0 R 0
ADDP	1F Hex R/W Default	ADDP 7 R/W 0	ADDP 6 R/W 0	ADDP 5 R/W 0	ADDP 4 R/W 0	ADDP 3 R/W 0	ADDP 2 R/W 0	ADDP 1 R/W 0	ADDP 0 R/W 0

Table-16 Expanded (Indirect Address Mode) Register Map

Register	Address R/W Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
e-SING	00H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	SING 3 R/W 0	SING 2 R/W 0	SING 1 R/W 0	SING 0 R/W 0
e-CODE	01H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	CODE 3 R/W 0	CODE 2 R/W 0	CODE 1 R/W 0	CODE 0 R/W 0
e-CRS	02H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	CRS 3 R/W 0	CRS 2 R/W 0	CRS 1 R/W 0	CRS 0 R/W 0
e-RPDN	03H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	RPDN 3 R/W 0	RPDN 2 R/W 0	RPDN 1 R/W 0	RPDN 0 R/W 0
e-TPDN	04H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	TPDN 3 R/W 0	TPDN 2 R/W 0	TPDN 1 R/W 0	TPDN 0 R/W 0
e-CZER	05H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	CZER 3 R/W 0	CZER 2 R/W 0	CZER 1 R/W 0	CZER 0 R/W 0
e-CODV	06H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	CODV 3 R/W 0	CODV 2 R/W 0	CODV 1 R/W 0	CODV 0 R/W 0
e-EQUA	07H R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	EQUA 3 R/W 0	EQUA 2 R/W 0	EQUA 1 R/W 0	EQUA 0 R/W 0
ADDP	1FH R/W Default	ADDP 7 R/W 0	ADDP 6 R/W 0	ADDP 5 R/W 0	ADDP 4 R/W 0	ADDP 3 R/W 0	ADDP 2 R/W 0	ADDP 1 R/W 0	ADDP 0 R/W 0

3.3 REGISTER DESCRIPTION

3.3.1 PRIMARY REGISTERS

ID: Device ID Register (R, Address = 00H)

Symbol	Position	Default	Description
ID[7:0]	ID.7-0	10H	An 8-bit word is pre-set into the device as the identification and revision number. This number is different with the functional changes and is mask programmed.

ALB: Analog Loopback Configuration Register (R/W, Address = 01H)

Symbol	Position	Default	Description
-	ALB.7-4	0000	0 = Normal operation. 1 = Reserved.
ALB[3:0]	ALB.3-0	0000	0 = Normal operation. (Default) 1 = Analog Loopback enabled.

RLB: Remote Loopback Configuration Register (R/W, Address = 02H)

Symbol	Position	Default	Description
-	RLB.7-4	0000	0 = Normal operation. 1 = Reserved.
RLB[3:0]	RLB.3-0	0000	0 = Normal operation. (Default) 1 = Remote Loopback enabled.

TAO: Transmit All Ones Configuration Register (R/W, Address = 03H)

Symbol	Position	Default	Description
-	TAO.7-4	0000	0 = Normal operation. 1 = Reserved.
TAO[3:0]	TAO.3-0	0000	0 = Normal operation. (Default) 1 = Transmit all ones.

LOS: Loss of Signal Status Register (R, Address = 04H)

Symbol	Position	Default	Description
-	LOS.7-4	0000	0 = Normal operation. 1 = Reserved.
LOS[3:0]	LOS.3-0	0000	0 = Normal operation. (Default) 1 = Loss of signal detected.

DF: Driver Fault Status Register (R, Address = 05H)

Symbol	Position	Default	Description
-	DF.7-4	0000	0 = Normal operation. 1 = Reserved.
DF[3:0]	DF.3-0	0000	0 = Normal operation. (Default) 1 = Driver fault detected.

LOSM: Loss of Signal Interrupt Mask Register (R/W, Address = 06H)

Symbol	Position	Default	Description
-	LOSM.7-4	0000	0 = Normal operation. 1 = Reserved.
LOSM[3:0]	LOSM.3-0	0000	0 = LOS interrupt is not allowed. (Default) 1 = LOS interrupt is allowed.

DFM: Driver Fault Interrupt Mask Register (R/W, Address = 07H)

Symbol	Position	Default	Description
-	DFM.7-4	0000	0 = Normal operation. 1 = Reserved.
DFM[3:0]	DFM.3-0	0000	0 = Driver fault interrupt not allowed. (Default) 1 = Driver fault interrupt allowed.

LOSI: Loss of Signal Interrupt Status Register (R, Address = 08H)

Symbol	Position	Default	Description
-	LOSI.7-4	0000	0 = Normal operation. 1 = Reserved.
LOSI[3:0]	LOSI.3-0	0000	0 = (Default). Or after a **LOS** read operation. 1 = Any transition on **LOSn** (Corresponding **LOSMn** is set to '1').

DFI: Driver Fault Interrupt Status Register (R, Address = 09H)

Symbol	Position	Default	Description
-	DFI.7-4	0000	0 = Normal operation. 1 = Reserved.
DFI[3:0]	DFI.3-0	0000	0 = (Default). Or after a **DF** read operation. 1 = Any transition on **DFn** (Corresponding **DFMn** is set to '1').

RS: Software Reset Register (W, Address = 0AH)

Symbol	Position	Default	Description
RS[7:0]	RS.7-0	FFH	Writing to this register will not change the content in this register but initiate a 1 μs reset cycle, which means all the registers in the device are set to their default values.

PMON: Performance Monitor Configuration Register (R/W, Address = 0BH)

Symbol	Position	Default	Description
-	PMON.7-4	0000	0 = Normal operation. (Default) 1 = Reserved.
MC[3:0]	PMON.3-0	0000	0000 = Normal operation without monitoring (Default) 0001 = Monitor Receiver 1 0010 = Monitor Receiver 2 0011 = Monitor Receiver 3 0100-0111 = Reserved 1000 = Normal operation without monitoring 1001 = Monitor Transmitter 1 1010 = Monitor Transmitter 2 1011 = Monitor Transmitter 3 1100-1111 = Reserved

DLB: Digital Loopback Configuration Register (R/W, Address = 0CH)

Symbol	Position	Default	Description
-	DLB.7-4	0000	0 = Normal operation. 1 = Reserved.
DLB[3:0]	DLB.3-0	0000	0 = Normal operation. (Default) 1 = Digital Loopback enabled.

LAC: LOS/AIS Criteria Configuration Register (R/W, Address = 0DH)

Symbol	Position	Default	Description
-	LAC.7-4	0000	0 = Normal operation. 1 = Reserved.
LAC[3:0]	LAC.3-0	0000	0 = G.775 (Default) 1 = ETSI 300 233

ATAO: Automatic TAOS Configuration Register (R/W, Address = 0EH)

Symbol	Position	Default	Description
-	ATAO.7-4	0000	0 = Normal operation. 1 = Reserved.
ATAO[3:0]	ATAO.3-0	0000	0 = No automatic transmit all ones. (Default) 1 = Automatic transmit all ones to the line side during LOS.

GCF: Global Configuration Register (R/W, Address = 0FH)

Symbol	Position	Default	Description
-	GCF.7	0	0 = Normal operation. 1 = Reserved.
AISE	GCF.6	0	0 = AIS insertion to the system side disabled on LOS. 1 = AIS insertion to the system side enabled on LOS.
SCPB	GCF.5	0	0 = Short circuit protection is enabled. 1 = Short circuit protection is disabled.
CODE	GCF.4	0	0 = HDB3 encoder/decoder enabled. 1 = AMI encoder/decoder enabled.
JADP	GCF.3	0	Jitter Attenuator Depth Select 0 = 32-bit FIFO (Default) 1 = 64-bit FIFO
JABW	GCF.2	0	Jitter Transfer Function Bandwidth Select 0 = 1.7 Hz 1 = 6.6 Hz
JACF[1:0]	GCF.1-0	00	Jitter Attenuator Configuration 00 = JA not used. (Default) 01 = JA in transmit path 10 = JA not used. 11 = JA in receive path

OE: Output Enable Configuration Register (R/W, Address = 12H)

Symbol	Position	Default	Description
-	OE.7-4	0000	0 = Normal operation. 1 = Reserved.
OE[3:0]	OE.3-0	0000	0 = Transmit drivers enabled. (Default) 1 = Transmit drivers in high-Z state.

AIS: Alarm Indication Signal Status Register (R, Address = 13H)

Symbol	Position	Default	Description
-	AIS.7-4	0000	0 = Normal operation. 1 = Reserved.
AIS[3:0]	AIS.3-0	0000	0 = Normal operation. (Default) 1 = AIS detected.

AISM: Alarm Indication Signal Interrupt Mask Register (R/W, Address = 14H)

Symbol	Position	Default	Description
-	AISM.7-4	0000	0 = Normal operation. 1 = Reserved.
AISM[3:0]	AISM.3-0	0000	0 = AIS interrupt is not allowed. (Default) 1 = AIS interrupt is allowed.

AISI: Alarm Indication Signal Interrupt Status Register (R, Address = 15H)

Symbol	Position	Default	Description
-	AISI.7-4	0000	0 = Normal operation. 1 = Reserved.
AISI[3:0]	AISI.3-0	0000	0 = (Default), or after an **AIS** read operation 1 = Any transition on **AISn**. (Corresponding **AISMn** is set to '1'.)

ADDP: Address Pointer Control Register (R/W, Address = 1F H)

Symbol	Position	Default	Description
ADDP[7:0]	ADDP.7-0	00H	Two kinds of configuration in this register can be set to switch between primary register bank and expanded register bank. When power up, the address pointer will point to the top address of primary register bank automatically. 00H = The address pointer points to the top address of primary register bank (default). AAH = The address pointer points to the top address of expanded register bank.

3.3.2 EXPANDED REGISTER DESCRIPTION

e-SING: Single Rail Mode Setting Register (R/W, Expanded Address = 00H)

Symbol	Position	Default	Description
-	SING.7-4	0000	0 = Normal operation. 1 = Reserved.
SING[3:0]	SING.3-0	0000	0 = Pin TDNn selects single rail mode or dual rail mode. (Default) 1 = Single rail mode enabled (with CRSn=0)

e-CODE: Encoder/Decoder Selection Register (R/W, Expanded Address = 01H)

Symbol	Position	Default	Description
-	CODE.7-4	0000	0 = Normal operation. 1 = Reserved.
CODE[3:0]	CODE.3-0	0000	CODEn selects AMI or HDB3 encoder/decoder on a per channel basis with SINGn = 1 and CRSn = 0. 0 = HDB3 encoder/decoder enabled. (Default) 1 = AMI encoder/decoder enabled.

e-CRS: Clock Recovery Enable/Disable Selection Register (R/W, Expanded Address = 02H)

Symbol	Position	Default	Description
-	CRS.7-4	0000	0 = Normal operation. 1 = Reserved.
CRS[3:0]	CRS.3-0	0000	0 = Clock recovery enabled. (Default) 1 = Clock recovery disabled.

e-RPDN: Receiver n Powerdown Register (R/W, Expanded Address = 03H)

Symbol	Position	Default	Description
-	RPDN.7-4	0000	0 = Normal operation. 1 = Reserved.
RPDN[3:0]	RPDN.3-0	0000	0 = Normal operation. (Default) 1 = Receiver n is powered down.

e-TPDN: Transmitter n Powerdown Register (R/W, Expanded Address = 04H)

Symbol	Position	Default	Description
-	TPDN.7-4	0000	0 = Normal operation. 1 = Reserved.
TPDN[3:0]	TPDN.3-0	0000	0 = Normal operation. (Default) 1 = Transmitter n is powered down(1) (the corresponding transmit output driver enters a low power high-Z mode).

1. Transmitter n is powered down when either pin TCLKn is pulled low or TPDNn is set to '1'.

e-CZER: Consecutive Zero Detect Enable/Disable Register (R/W, Expanded Address = 05H)

Symbol	Position	Default	Description
-	CZER.7-4	0000	0 = Normal operation. 1 = Reserved.
CZER[3:0]	CZER.3-0	0000	0 = Excessive zeros detect disabled. (Default) 1 = Excessive zeros detect enabled for HDB3 decoder in single rail mode.

e-CODV: Code Violation Detect Enable/Disable Register (R/W, Expanded Address = 06H)

Symbol	Position	Default	Description
-	CODV.7-4	0000	0 = Normal operation. 1 = Reserved.
CODV[3:0]	CODV.3-0	0000	0 = Code Violation Detect enable for HDB3 decoder in single rail mode. (Default) 1 = Code Violation Detect disabled.

e-EQUA: Receive Equalizer Enable/Disable Register (R/W, Expanded Address = 07H)

Symbol	Position	Default	Description
-	EQUA.7-4	0000	0 = Normal operation. 1 = Reserved.
EQUA[3:0]	EQUA.3-0	0000	0 = Normal operation. (Default) 1 = Equalizer in Receiver n is enabled, which can improve the receive performance when transmission length is more than 200 m.

4 IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82V2054 supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is achieved through signals applied to the TMS and TCK pins. Data is shifted into the registers via the TDI pin, and shifted out of the registers via the TDO pin. JTAG test data are clocked at a rate determined by JTAG test clock.

The JTAG boundary scan registers includes BSR (Boundary Scan Register), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. Refer to Figure-21 for architecture.

4.1 JTAG INSTRUCTIONS AND INSTRUCTION REGISTER (IR)

The IR with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. See Table-17 Instruction Register Description on page 37 for details of the codes and the instructions related.

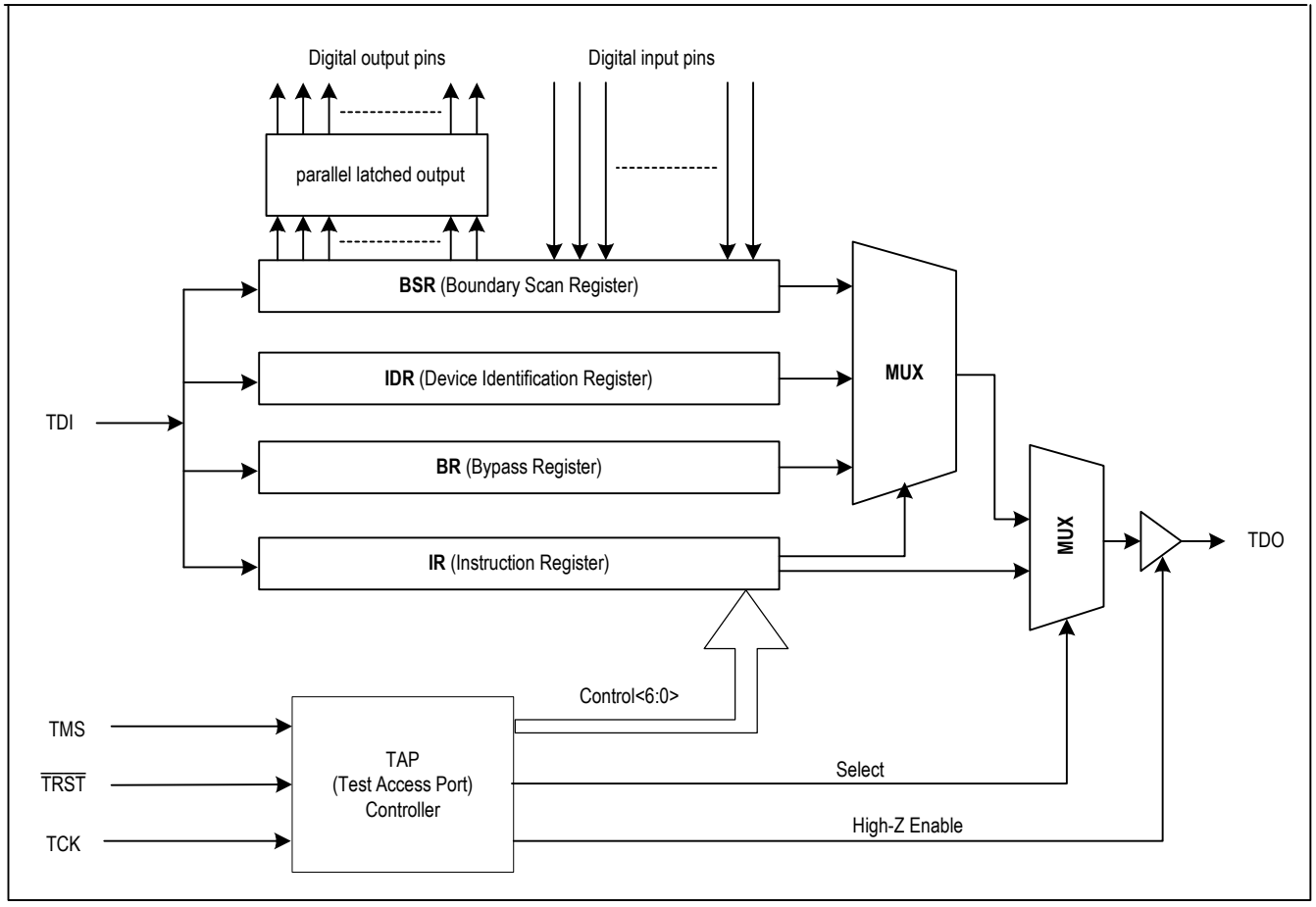


Figure-21 JTAG Architecture

Table-17 Instruction Register Description

IR Code	Instruction	Comments
000	Extest	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between TDI and TDO. The signal on the input pins can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
100	Sample/Preload	The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. The normal path between IDT82V2054 logic and the I/O pins is maintained. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.
110	Idcode	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
111	Bypass	The bypass instruction shifts data from input TDI to output TDO with one TCK clock period delay. The instruction is used to bypass the device.

Table-18 Device Identification Register Description

Bit No.	Comments
0	Set to '1'
1~11	Producer Number
12~27	Part Number
28~31	Device Revision

4.2 JTAG DATA REGISTER

4.2.1 DEVICE IDENTIFICATION REGISTER (IDR)

The IDR can be set to define the producer number, part number and the device revision, which can be used to verify the proper version or revision number that has been used in the system under test. The IDR is 32 bits long and is partitioned as in Table-18. Data from the IDR is shifted out to TDO LSB first.

4.2.2 BYPASS REGISTER (BR)

The BR consists of a single bit. It can provide a serial path between the TDI input and TDO output, bypassing the BSR to reduce test access times.

4.2.3 BOUNDARY SCAN REGISTER (BSR)

The BSR can apply and read test patterns in parallel to or from all the digital I/O pins. The BSR is a 98 bits long shift register and is initialized and read using the instruction EXTEST or SAMPLE/PRELOAD. Each pin is related to one or more bits in the BSR. Please refer to Table-19 for details of BSR bits and their functions.

Table-19 Boundary Scan Register Description

Bit No.	Bit Symbol	Pin Signal	Type	Comments
0	POUT0	AD0	I/O	
1	PIN0	AD0	I/O	
2	POUT1	AD1	I/O	
3	PIN1	AD1	I/O	
4	POUT2	AD2	I/O	
5	PIN2	AD2	I/O	
6	POUT3	AD3	I/O	
7	PIN3	AD3	I/O	
8	POUT4	AD4	I/O	
9	PIN4	AD4	I/O	
10	POUT5	AD5	I/O	
11	PIN5	AD5	I/O	
12	POUT6	AD6	I/O	
13	PIN6	AD6	I/O	
14	POUT7	AD7	I/O	
15	PIN7	AD7	I/O	

Table-19 Boundary Scan Register Description (Continued)

Bit No.	Bit Symbol	Pin Signal	Type	Comments
16	PIOS	N/A	-	Controls pins AD[7:0]. When '0', the pins are configured as outputs. The output values to the pins are set in POUT 7~0. When '1', the pins are high-Z. The input values to the pins are read in PIN 7~0.
17	TCLK1	TCLK1	I	
18	TDP1	TDP1	I	
19	TDN1	TDN1	I	
20	RCLK1	RCLK1	O	
21	RDP1	RDP1	O	
22	RDN1	RDN1	O	
23	HZEN1	N/A	-	Controls pin RDP1, RDN1 and RCLK1. When '0', the outputs are enabled on the pins. When '1', the pins are high-Z.
24	LOS1	LOS1	O	
25	TCLK0	TCLK0	I	
26	TDP0	TDP0	I	
27	TDN0	TDN0	I	
28	RCLK0	RCLK0	O	
29	RDP0	RDP0	O	
30	RDN0	RDN0	O	
31	HZEN0	N/A	-	Controls pin RDP0, RDN0 and RCLK0. When '0', the outputs are enabled on the pins. When '1', the pins are high-Z.
32	LOS0	LOS0	O	
33	MODE1	MODE1	I	
34	LOS3	LOS3	O	
35	RDN3	RDN3	O	
36	RDP3	RDP3	O	
37	HZEN3	N/A	-	Controls pin RDP3, RDN3 and RCLK3. When '0', the outputs are enabled on the pins. When '1', the pins are high-Z.
38	RCLK3	RCLK3	O	
39	TDN3	TDN3	I	
40	TDP3	TDP3	I	
41	TCLK3	TCLK3	I	
42	LOS2	LOS2	O	
43	RDN2	RDN2	O	
44	RDP2	RDP2	O	
45	HZEN2	N/A	-	Controls pin RDP2, RDN2 and RCLK2. When '0', the outputs are enabled on the pins. When '1', the pins are high-Z.
46	RCLK2	RCLK2	O	
47	TDN2	TDN2	I	
48	TDP2	TDP2	I	
49	TCLK2	TCLK2	I	
50	INT	INT	O	
51	ACK	$\overline{ACK}$	O	
52	SDORDYS	N/A	-	Control pin $\overline{ACK}$. When '0', the output is enabled on pin $\overline{ACK}$. When '1', the pin is high-Z.
53	WRB	$\overline{DS}$	I	
54	RDB	R/$\overline{W}$	I	
55	ALE	ALE	I	
56	CSB	$\overline{CS}$	I	

Table-19 Boundary Scan Register Description (Continued)

Bit No.	Bit Symbol	Pin Signal	Type	Comments
57	MODE0	MODE0	I	
58	LOG0	LOG0(1)	I	
59	LOG0	LOG0	I	
60	LOG0	LOG0	I	
61	MASK	MASK(2)	O	
62	MASK	MASK	O	
63	MASK	MASK	O	
64	LOG1	LOG1(3)	-	
65	MASK	MASK	O	
66	LOG0	LOG0	I	
67	LOG0	LOG0	I	
68	LOG0	LOG0	I	
69	MASK	MASK	O	
70	MASK	MASK	O	
71	MASK	MASK	O	
72	LOG1	LOG1	-	
73	MASK	MASK	O	
74	OE	OE	I	
75	CLKE	CLKE	I	
76	MASK	MASK	O	
77	MASK	MASK	O	
78	MASK	MASK	O	
79	LOG1	LOG1	-	
80	MASK	MASK	O	
81	LOG0	LOG0	I	
82	LOG0	LOG0	I	
83	LOG0	LOG0	I	
84	MASK	MASK	O	
85	MASK	MASK	O	
86	MASK	MASK	O	
87	LOG1	LOG1	-	
88	MASK	MASK	O	
89	LOG0	LOG0	I	
90	LOG0	LOG0	I	
91	LOG0	LOG0	I	
92	MCLK	MCLK	I	
93	MODE2	MODE2	I	
94	A4	A4	I	
95	A3	A3	I	
96	A2	A2	I	
97	A1	A1	I	
98	A0	A0	I	

1. Set to Logic 0.

2. Reserved output, do not test.

3. Set to Logic 1.

4.3 TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchronous state machine. Figure-22 shows its state diagram A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. Refer to Table-20 for details of the state description.

Table-20 TAP Controller State Description

State	Description
Test Logic Reset	In this state, the test logic is disabled. The device is set to normal operation. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. The device processor automatically enters this state at power-up.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan state.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other test data registers, which do not have parallel input, are not changed. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output changes only in this state. All shift-register stages in the test data register selected by the current instruction retain their previous value and the instruction does not change during this state.
Select-IR-Scan	This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of '100' on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.

Table-20 TAP Controller State Description (Continued)

State	Description
Exit1-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.

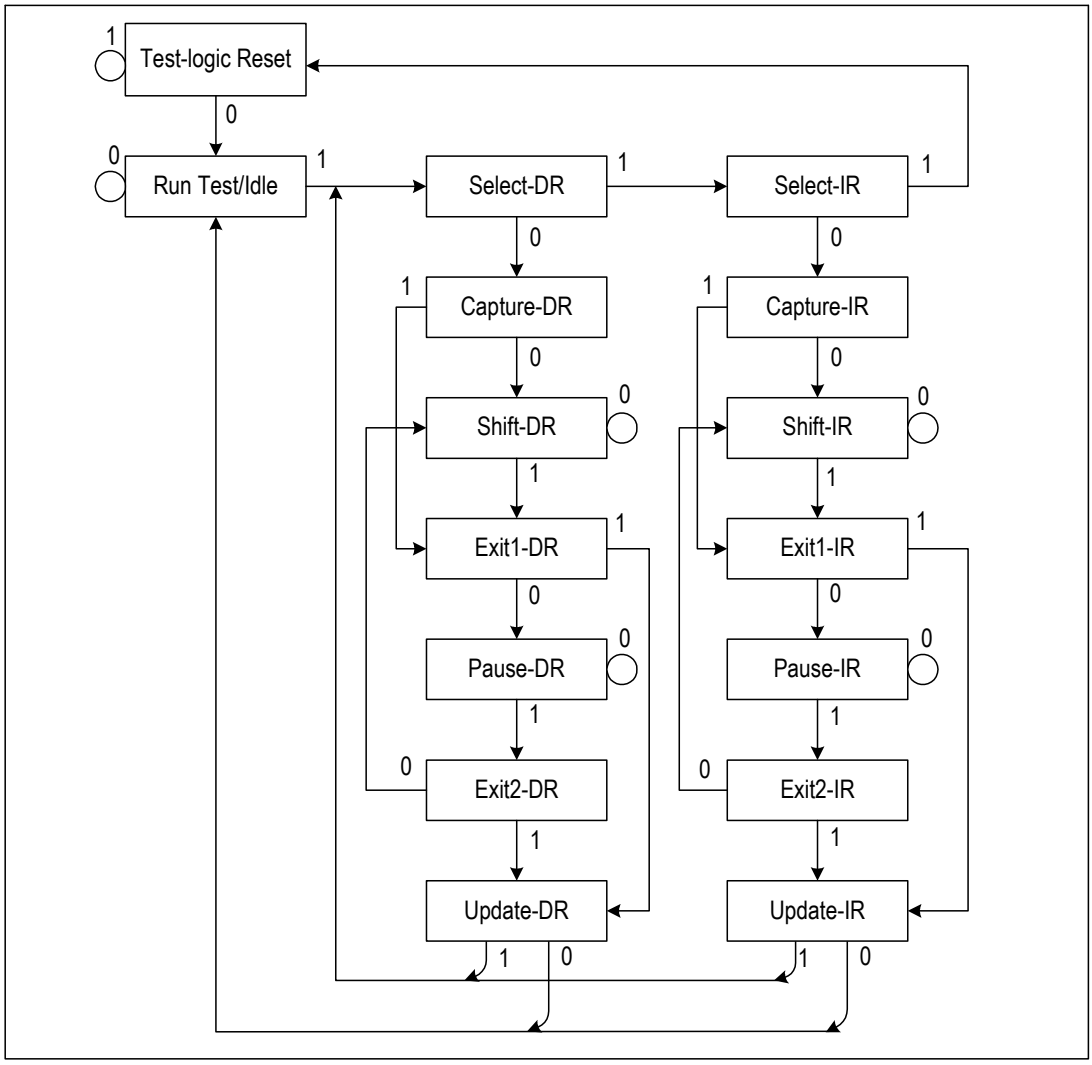


Figure-22 JTAG State Diagram

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min	Max	Unit
VDDA, VDDD	Core Power Supply	-0.5	4.0	V
VDDIO0, VDDIO1	I/O Power Supply	-0.5	4.0	V
VDDT0-3	Transmit Power Supply	-0.5	7.0	V
Vin	Input Voltage, any digital pin	GND-0.5	5.5	V
	Input Voltage(1), RTIPn pins and RRINGn pins	GND-0.5	VDDA+ 0.5 VDDD+ 0.5	V V
	ESD Voltage, any pin(2)	2000		V
Iin	Transient Latch-up Current, any pin		100	mA
	Input Current, any digital pin(3)	-10	10	mA
	DC Input Current, any analog pin(3)		±100	mA
Pd	Maximum Power Dissipation in package		1.6	W
Tc	Case Temperature		120	°C
Ts	Storage Temperature	-65	+150	°C

CAUTION: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Referenced to ground
2. Human body model
3. Constant input current

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDDD	Core Power Supply	3.13	3.3	3.47	V
VDDIO	I/O Power Supply	3.13	3.3	3.47	V
VDDT	Transmitter Supply				
	3.3 V	3.13	3.3	3.47	V
	5 V	4.75	5.0	5.25	V
T_A	Ambient Operating Temperature	-40	25	85	°C
R_L	Output load at TTIPn pins and TRINGn pins	25			Ω
I_{VDD}	Average Core Power Supply Current(1)		40	60	mA
I_{VDDIO}	I/O Power Supply Current(2)		15	25	mA
I_{VDDT}	Average transmitter power supply current, E1 mode(1), (3)				
	75 Ω 50% ones density data:			70	mA
	100% ones density data:			125	mA
	120 Ω 50% ones density data:			65	mA
	100% ones density data:			120	mA

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. Digital output is driving 50 pF load, digital input is within 10% of the supply rails.
3. Power consumption includes power absorbed by line load and external transmitter components.

POWER CONSUMPTION

Symbol	Parameter	LEN	Min	Typ	Max(1)(2)	Unit
	E1, 3.3 V, 75 Ω Load					
	50% ones density data:	000	-	403	-	mW
	100% ones density data:	000	-	613	686	mW
	E1, 3.3 V, 120 Ω Load					
	50% ones density data:	000	-	368	-	mW
	100% ones density data:	000	-	543	607	mW
	E1, 5.0 V, 75 Ω Load					
	50% ones density data:	000	-	511	-	mW
	100% ones density data:	000	-	829	927	mW
	E1, 5.0 V, 120 Ω Load					
	50% ones density data:	000	-	458	-	mW
	100% ones density data:	000	-	723	809	mW

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.

2. Power consumption includes power absorbed by line load and external transmitter components.

DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Level Voltage				
	MODE2, JAS and LPn pins			$\frac{1}{3}$ VDDIO-0.2	V
	All other digital inputs pins			0.8	V
V_{IM}	Input Mid Level Voltage				
	MODE2, JAS and LPn pins	$\frac{1}{3}$ VDDIO+0.2	$\frac{1}{2}$ VDDIO	$\frac{2}{3}$ VDDIO-0.2	V
V_{IH}	Input High Voltage				
	MODE2, JAS and LPn pins	$\frac{2}{3}$ VDDIO+ 0.2			V
	All other digital inputs pins	2.0			V
V_{OL}	Output Low level Voltage(1) (Iout = 1.6 mA)			0.4	V
V_{OH}	Output High level Voltage(1) (Iout = 400 μA)	2.4		VDDIO	V
V_{MA}	Analog Input Quiescent Voltage (RTIPn/RRINGn pin while floating)	1.33	1.4	1.47	V
I_H	Input High Level Current (MODE2, JAS and LPn pin)			50	μA
I_L	Input Low Level Current (MODE2, JAS and LPn pin)			50	μA
I_I	Input Leakage Current				
	TMS, TDI and $\overline{TRST}$ pins			50	μA
	All other digital input pins	-10		10	μA
I_{ZL}	High-Z Leakage Current	-10		10	μA
Z_{OH}	Output High Impedance on TTIPn pins and TRINGn pins	150			kΩ

1. Output drivers will output CMOS logic levels into CMOS loads.

TRANSMITTER CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
V_{o-p}	Output Pulse Amplitudes[1] 75 Ω load 120 Ω load		 2.14 2.7	 2.37 3.0	 2.6 3.3	 V V
V_{o-s}	Zero (space) Level 75 Ω load 120 Ω load		 -0.237 -0.3		 0.237 0.3	 V V
	Transmit Amplitude Variation with supply		-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses				200	mV
T_{PW}	Output Pulse Width at 50% of nominal amplitude		232	244	256	ns
	Ratio of the amplitudes of Positive and Negative Pulses at the center of the pulse interval		0.95		1.05	
RTX	Transmit Return Loss[2]					
	75 Ω	51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	15 15 15			dB dB dB
	120 Ω	51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	15 15 15			dB dB dB
JTX_{P-P}	Intrinsic Transmit Jitter (TCLK is jitter free, JA enabled) 20 Hz – 100 kHz			 0.050		 U.I.
Td	Transmit Path Delay (JA is disabled) Single Rail Dual Rail			 8 3		 U.I. U.I.
I_{SC}	Line Short Circuit Current[3]			180		mAp

1. Measured at the line output ports

2. Test at IDT82V2054 evaluation board

3. Measured on device, between TTIPn and TRINGn

RECEIVER CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
ATT	Permissible Cable Attenuation (@ 1024 kHz)			15	dB
IA	Input Amplitude	0.1		0.9	Vp
SIR	Signal to Interference Ratio Margin(1)	-15			dB
SRE	Data Decision Threshold (refer to peak input voltage)		50		%
	Data Slicer Threshold		150		mV
	Analog Loss Of Signal(2) Declare/Clear:	120/150	200/250	280/350	mVp
	Allowable consecutive zeros before LOS G.775: ETSI 300 233:		32 2048		
	LOS Reset Clock Recovery Mode	12.5			% ones
JRX_{p-p}	Peak to Peak Intrinsic Receive Jitter (JA disabled)			0.0625	U.I.
JTRX	Jitter Tolerance 1 Hz – 20 Hz 20 Hz – 2.4 kHz 18 kHz – 100 kHz	 18.0 1.5 0.2			 U.I. U.I. U.I.
ZDM	Receiver Differential Input Impedance		120		kΩ
ZCM	Receiver Common Mode Input Impedance to GND	10			kΩ
RRX	Receive Return Loss 51 kHz – 102 kHz 102 kHz – 2.048 MHz 2.048 MHz – 3.072 MHz	 20 20 20			 dB dB dB
	Receive Path Delay Dual rail Single rail		 3 8		 U.I. U.I.

1. Per G.703, O.151 @ 6 dB cable attenuation

2. Measured on device, between RTIP and RRING, all ones signal.

JITTER ATTENUATOR CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
f_{-3dB}	Jitter Transfer Function Corner Frequency (–3 dB)				
	Host mode: 32/64 bit FIFO JABW = 0: JABW = 1: Hardware mode		 1.7 6.6 1.7		 Hz Hz Hz
	Jitter Attenuator(1) @ 3 Hz @ 40 Hz @ 400 Hz @ 100 kHz	 -0.5 -0.5 +19.5 +19.5			 dB dB dB dB
td	Jitter Attenuator Latency Delay 32 bit FIFO: 64 bit FIFO:		 16 32		 U.I. U.I.
	Input Jitter Tolerance before FIFO Overflow Or Underflow 32 bit FIFO: 64 bit FIFO:		 28 56		 U.I. U.I.
	Output Jitter in Remote Loopback(2)			0.11	U.I.

1. Per G.736, see Figure-38 on page 55.

2. Per ETSI CTR12/13 output jitter.

TRANSCEIVER TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
	MCLK Frequency		2.048		MHz
	MCLK Tolerance	-100		100	ppm
	MCLK Duty Cycle	40		60	%
Transmit path					
	TCLK Frequency		2.048		MHz
	TCLK Tolerance	-50		+50	ppm
	TCLK Duty Cycle	10		90	%
t1	Transmit Data Setup Time	40			ns
t2	Transmit Data Hold Time	40			ns
	Delay Time of OE Low to Driver High-Z			1	µs
	Delay Time of TCLK Low to Driver High-Z	40	44	48	µs
Receive path					
	Clock Recovery Capture Range(1)		± 80		ppm
	RCLK Duty Cycle(2)	40	50	60	%
t4	RCLK Pulse Width(2)	457	488	519	ns
t5	RCLK Pulse Width Low Time	203	244	285	ns
t6	RCLK Pulse Width High Time	203	244	285	ns
	Rise/Fall Time(3)	5		30	ns
t7	Receive Data Setup Time	200	244		ns
t8	Receive Data Hold Time	200	244		ns
t9	RDPn/RDNn Pulse Width (MCLK = High)(4)	200	244		ns

1. Relative to nominal frequency, MCLK = ± 100 ppm

2. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2 UI displacement for E1 per ITU G.823).

3. For all digital outputs. C load = 15 pF

4. Clock recovery is disabled in this mode.

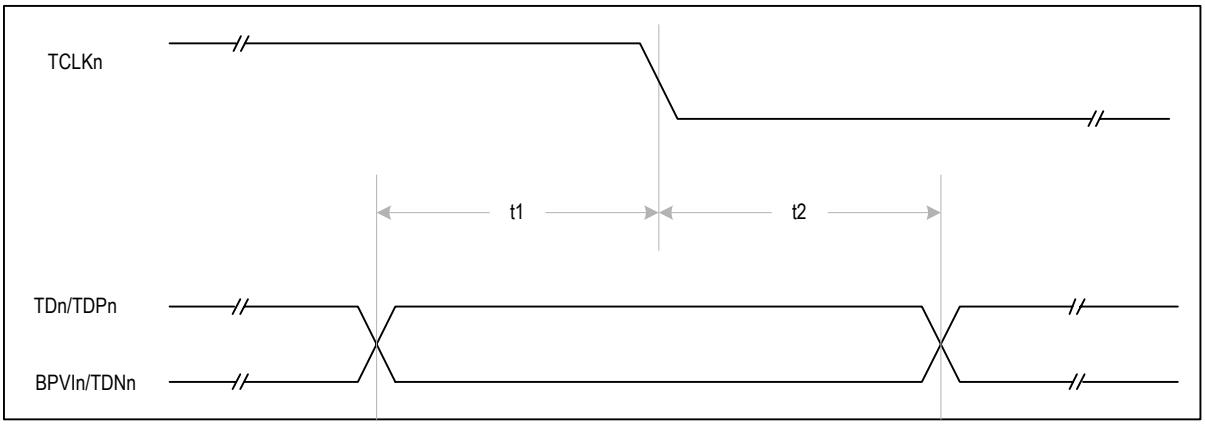


Figure-23 Transmit System Interface Timing

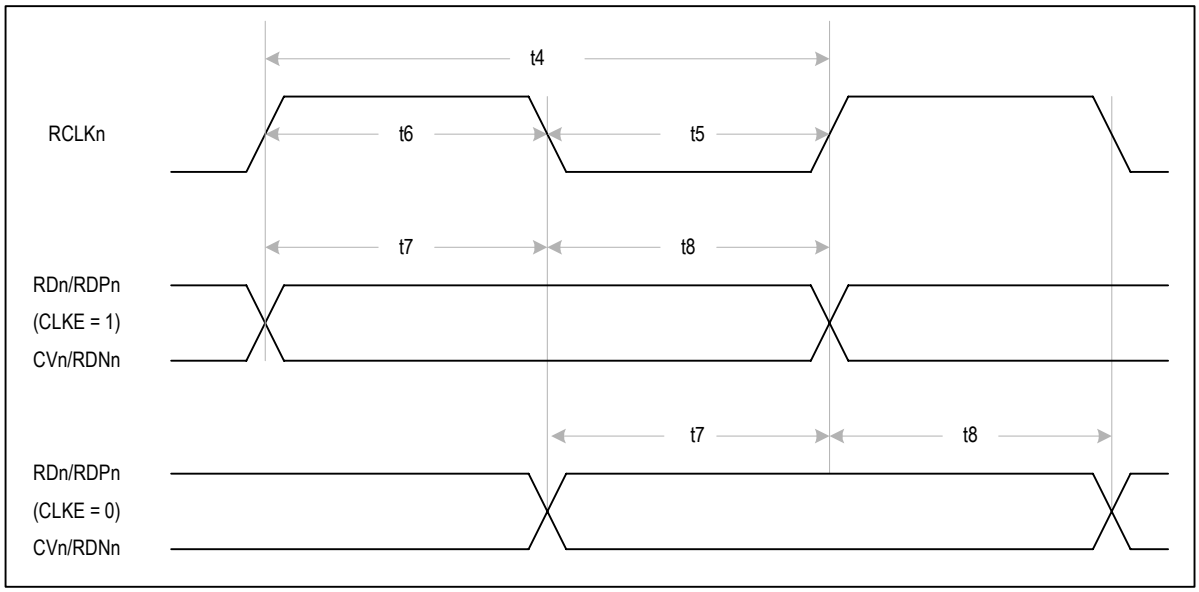


Figure-24 Receive System Interface Timing

JTAG TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	TCK Period	200			ns	
t2	TMS to TCK setup Time TDI to TCK Setup Time	50			ns	
t3	TCK to TMS Hold Time TCK to TDI Hold Time	50			ns	
t4	TCK to TDO Delay Time			100	ns	

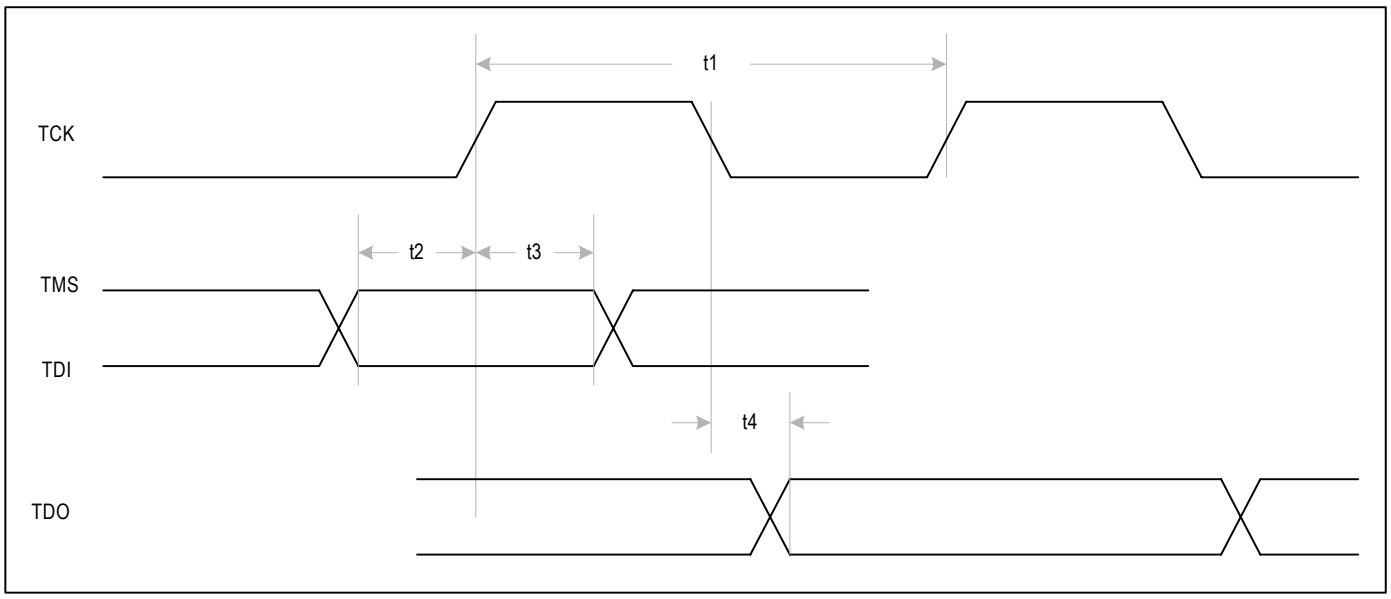


Figure-25 JTAG Interface Timing

PARALLEL HOST INTERFACE TIMING CHARACTERISTICS

INTEL MODE READ TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{RD}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{RD}$ Setup Time	0			ns	
t3	Inactive $\overline{RD}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid Address to Inactive ALE Setup Time (in Multiplexed Mode)	5			ns	
t5	Invalid $\overline{RD}$ to Address Hold Time (in Non-Multiplexed Mode)	0			ns	
t6	Active $\overline{RD}$ to Data Output Enable Time	7.5		15	ns	
t7	Inactive $\overline{RD}$ to Data High-Z Delay Time	7.5		15	ns	
t8	Active $\overline{CS}$ to RDY delay time	6		12	ns	
t9	Inactive $\overline{CS}$ to RDY High-Z Delay Time	6		12	ns	
t10	Inactive $\overline{RD}$ to Inactive $\overline{INT}$ Delay Time			20	ns	
t11	Address Latch Enable Pulse Width (in Multiplexed Mode)	10			ns	
t12	Address Latch Enable to $\overline{RD}$ Setup Time (in Multiplexed Mode)	0			ns	
t13	Address Setup time to Valid Data Time (in Non-Multiplexed Mode)	18		32	ns	
t14	Inactive $\overline{RD}$ to Active RDY Delay Time	10		15	ns	
t15	Active $\overline{RD}$ to Active RDY Delay Time	30		85	ns	
t16	Inactive ALE to Address Hold Time (in Multiplexed Mode)	5			ns	

1. The t1 is determined by the start time of the valid data when the RDY signal is not used.

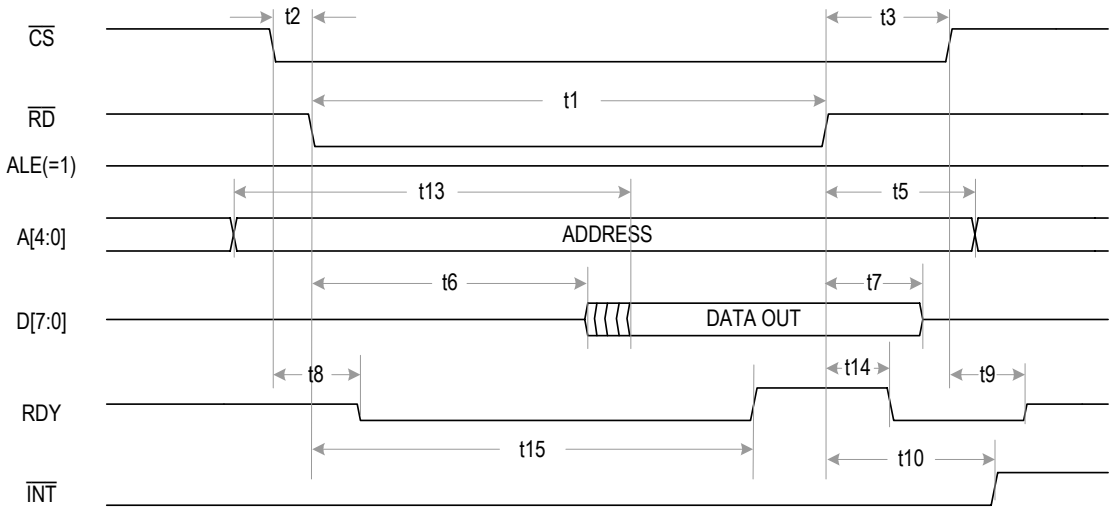


Figure-26 Non-Multiplexed Intel Mode Read Timing

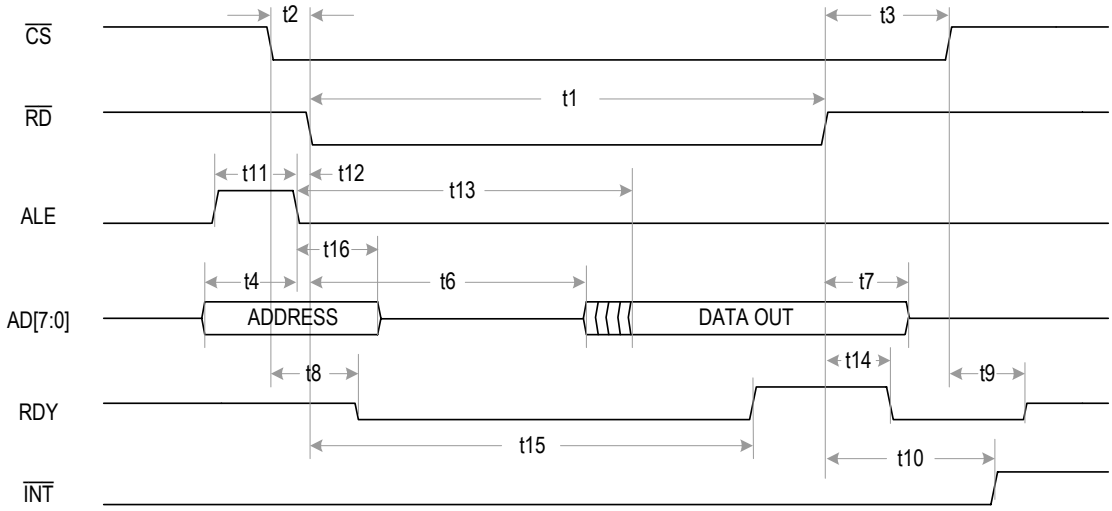


Figure-27 Multiplexed Intel Mode Read Timing

INTEL MODE WRITE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{WR}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{WR}$ Setup Time	0			ns	
t3	Inactive $\overline{WR}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid Address to Latch Enable Setup Time (in Multiplexed Mode)	5			ns	
t5	Invalid $\overline{WR}$ to Address Hold Time (in Non-Multiplexed Mode)	2			ns	
t6	Valid Data to Inactive $\overline{WR}$ Setup Time	5			ns	
t7	Inactive $\overline{WR}$ to Data Hold Time	10			ns	
t8	Active $\overline{CS}$ to Inactive RDY Delay Time	6		12	ns	
t9	Active $\overline{WR}$ to Active RDY Delay Time	30		85	ns	
t10	Inactive $\overline{WR}$ to Inactive RDY Delay Time	10		15	ns	
t11	Invalid $\overline{CS}$ to RDY High-Z Delay Time	6		12	ns	
t12	Address Latch Enable Pulse Width (in Multiplexed Mode)	10			ns	
t13	Inactive ALE to $\overline{WR}$ Setup Time (in Multiplexed Mode)	0			ns	
t14	Inactive ALE to Address hold time (in Multiplexed Mode)	5			ns	
t15	Address setup time to Inactive $\overline{WR}$ time (in Non-Multiplexed Mode)	5			ns	

1. The t1 can be 15 ns when RDY signal is not used.

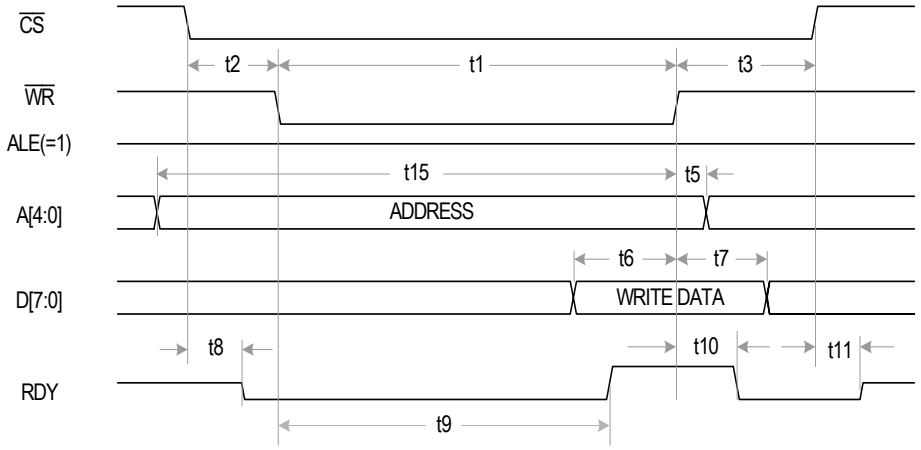


Figure-28 Non-Multiplexed Intel Mode Write Timing

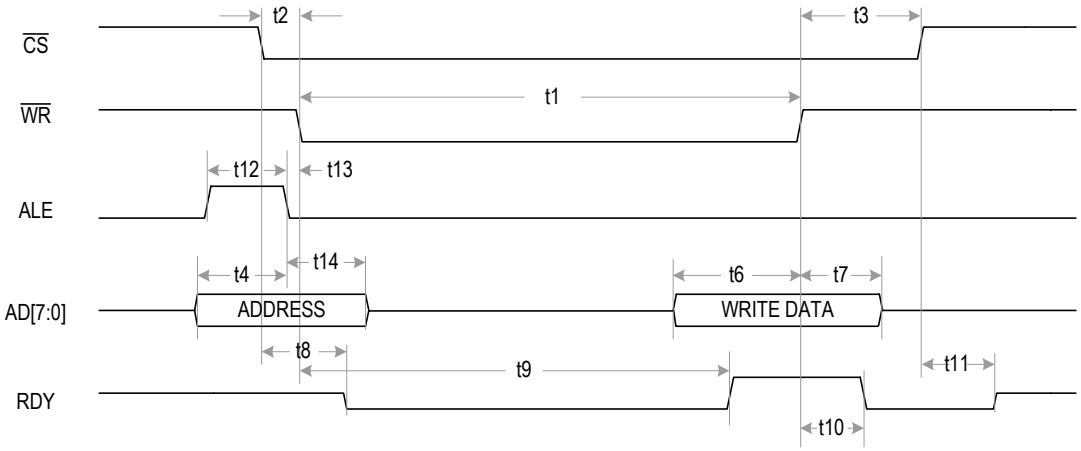


Figure-29 Multiplexed Intel Mode Write Timing

MOTOROLA MODE READ TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{DS}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{DS}$ Setup Time	0			ns	
t3	Inactive $\overline{DS}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid R/$\overline{W}$ to Active $\overline{DS}$ Setup Time	0			ns	
t5	Inactive $\overline{DS}$ to R/$\overline{W}$ Hold Time	0.5			ns	
t6	Valid Address to Active $\overline{DS}$ Setup Time (in Non-Multiplexed Mode)	5			ns	
t7	Active $\overline{DS}$ to Address Hold Time (in Non-Multiplexed Mode)	10			ns	
t8	Active $\overline{DS}$ to Data Valid Delay Time (in Non-Multiplexed Mode)	20		35	ns	
t9	Active $\overline{DS}$ to Data Output Enable Time	7.5		15	ns	
t10	Inactive $\overline{DS}$ to Data High-Z Delay Time	7.5		15	ns	
t11	Active $\overline{DS}$ to Active $\overline{ACK}$ Delay Time	30		85	ns	
t12	Inactive $\overline{DS}$ to Inactive $\overline{ACK}$ Delay Time	10		15	ns	
t13	Inactive $\overline{DS}$ to Invalid $\overline{INT}$ Delay Time			20	ns	
t14	Active $\overline{AS}$ to Active $\overline{DS}$ Setup Time (in Multiplexed Mode)	5			ns	

1. The t1 is determined by the start time of the valid data when the ACK signal is not used.

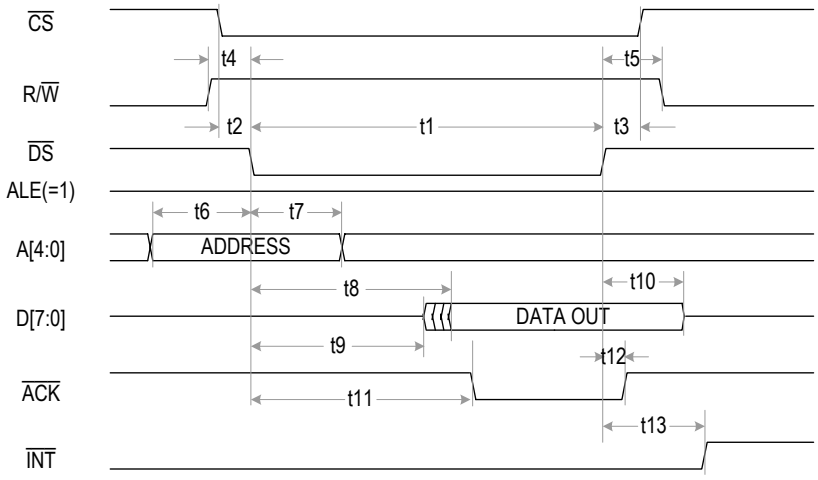


Figure-30 Non-Multiplexed Motorola Mode Read Timing

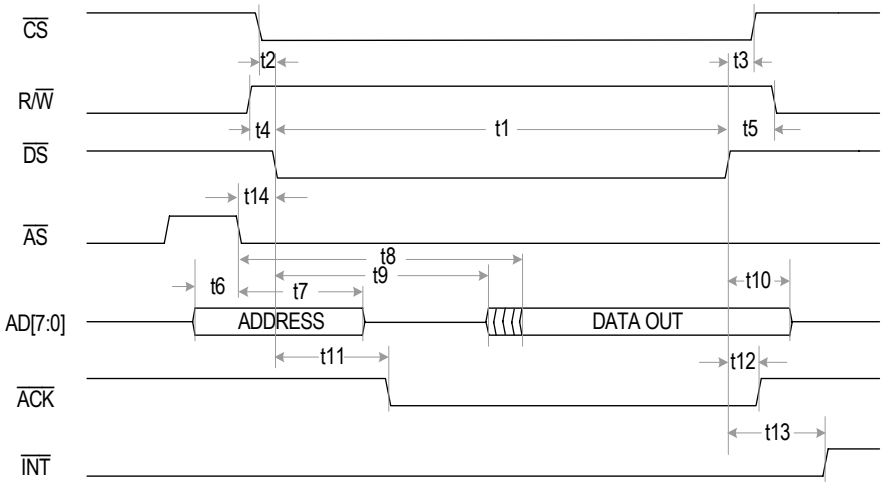


Figure-31 Multiplexed Motorola Mode Read Timing

MOTOROLA MODE WRITE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{DS}$ Pulse Width	90			ns	(1)
t2	Active $\overline{CS}$ to Active $\overline{DS}$ Setup Time	0			ns	
t3	Inactive $\overline{DS}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid R/$\overline{W}$ to Active $\overline{DS}$ Setup Time	10			ns	
t5	Inactive $\overline{DS}$ to R/$\overline{W}$ Hold Time	0			ns	
t6	Valid Address to Active $\overline{DS}$ Setup Time (in Non-Multiplexed Mode)	10			ns	
t7	Valid $\overline{DS}$ to Address Hold Time (in Non-Multiplexed Mode)	10			ns	
t8	Valid Data to Inactive $\overline{DS}$ Setup Time	5			ns	
t9	Inactive $\overline{DS}$ to Data Hold Time	10			ns	
t10	Active $\overline{DS}$ to Active $\overline{ACK}$ Delay Time	30		85	ns	
t11	Inactive $\overline{DS}$ to Inactive $\overline{ACK}$ Delay Time	10		15	ns	
t12	Active $\overline{AS}$ to Active $\overline{DS}$ (in Multiplexed Mode)	0			ns	
t13	Inactive $\overline{DS}$ to Inactive $\overline{AS}$ Hold Time (in Multiplexed Mode)	15			ns	

1. The t1 can be 15ns when the ACK signal is not used.

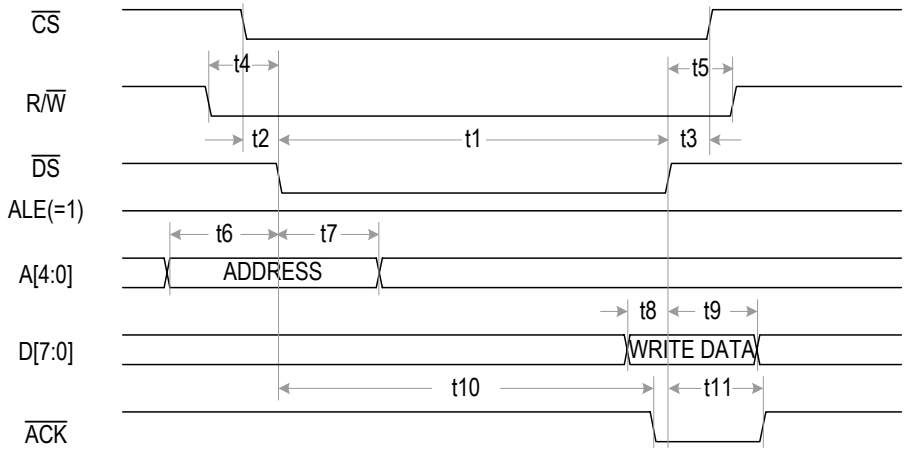


Figure-32 Non-Multiplexed Motorola Mode Write Timing

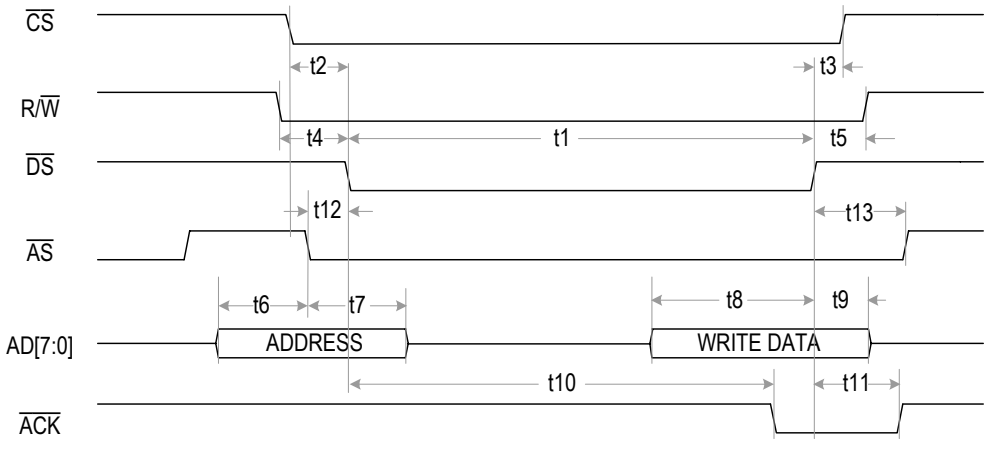


Figure-33 Multiplexed Motorola Mode Writing Timing

SERIAL HOST INTERFACE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	SCLK High Time	25			ns	
t2	SCLK Low Time	25			ns	
t3	Active $\overline{CS}$ to SCLK Setup Time	10			ns	
t4	Last SCLK Hold Time to Inactive $\overline{CS}$ Time	50			ns	
t5	$\overline{CS}$ Idle Time	50			ns	
t6	SDI to SCLK Setup Time	5			ns	
t7	SCLK to SDI Hold Time	5			ns	
t8	Rise/Fall Time (any pin)			100	ns	
t9	SCLK Rise and Fall Time			50	ns	
t10	SCLK to SDO Valid Delay Time		25	35	ns	Load = 50 pF
t11	SCLK Falling Edge to SDO High-Z Hold Time (CLKE = 0) or $\overline{CS}$ Rising Edge to SDO High-Z Hold Time (CLKE = 1)		100		ns	

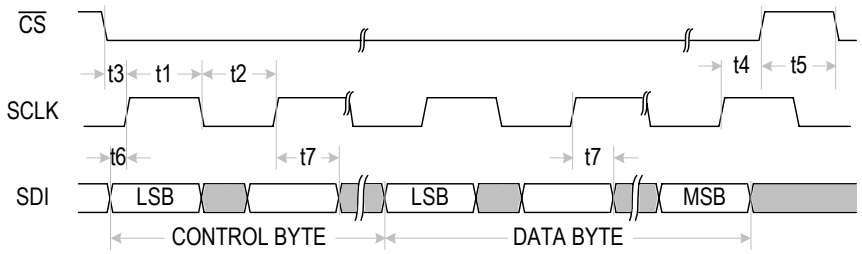


Figure-34 Serial Interface Write Timing

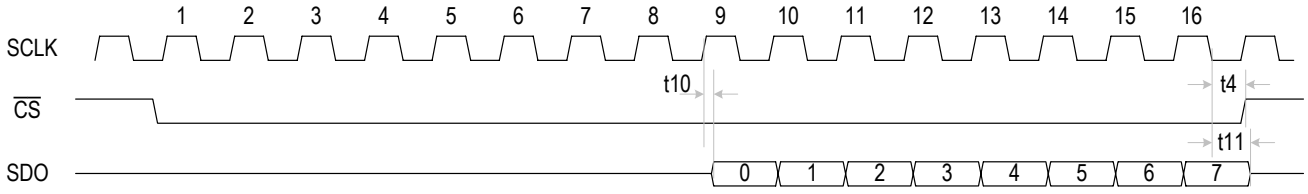


Figure-35 Serial Interface Read Timing with CLKE = 0

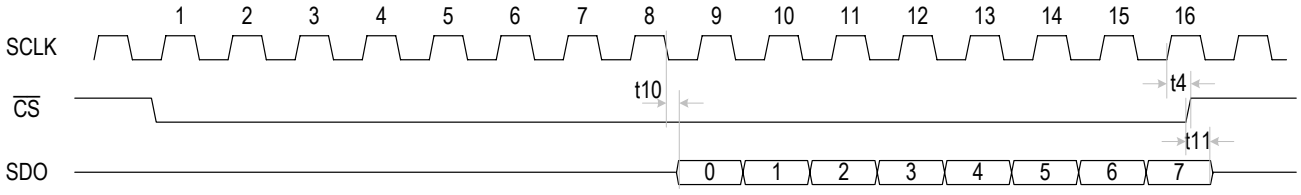
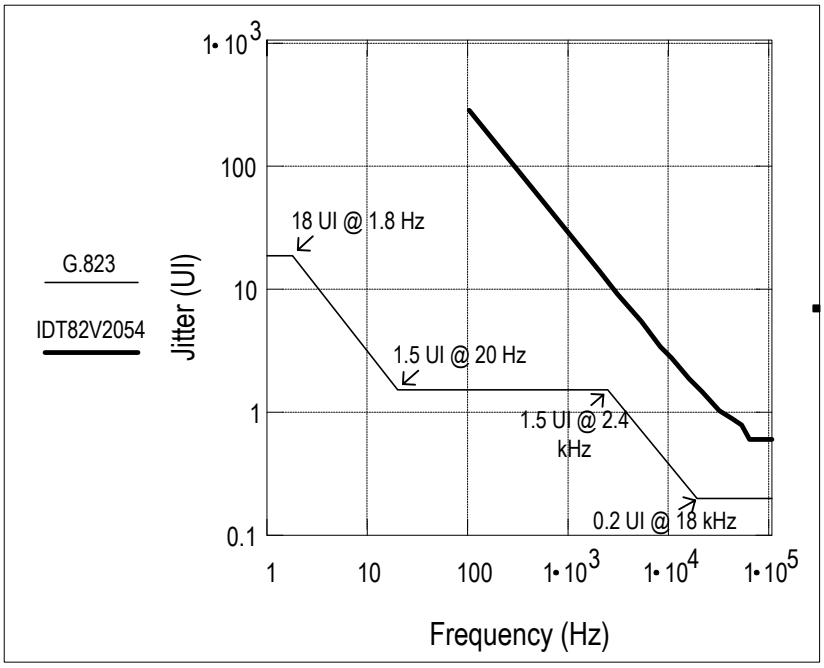


Figure-36 Serial Interface Read Timing with CLKE = 1

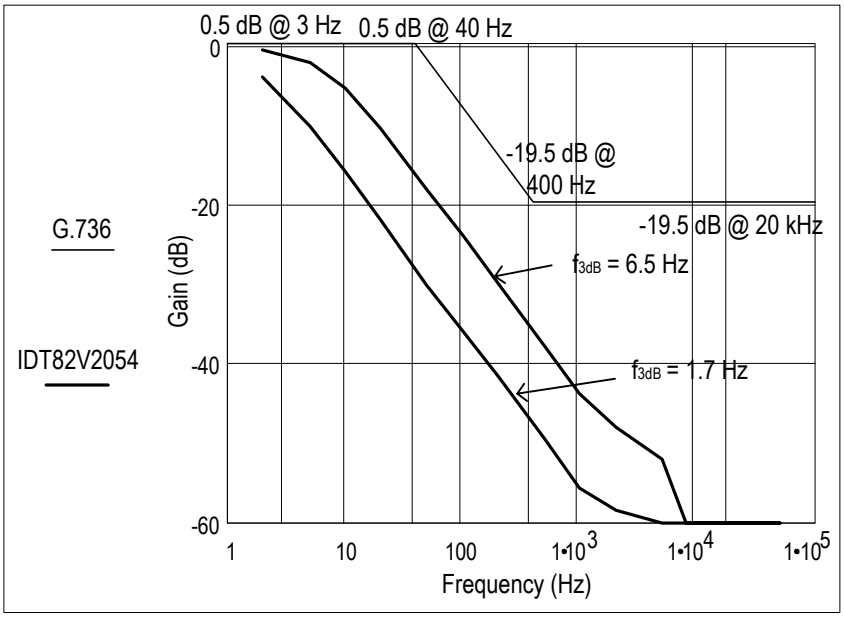
JITTER TOLERANCE PERFORMANCE



Test condition: PRBS 2^15-1; Line code rule HDB3 is used.

Figure-37 Jitter Tolerance Performance

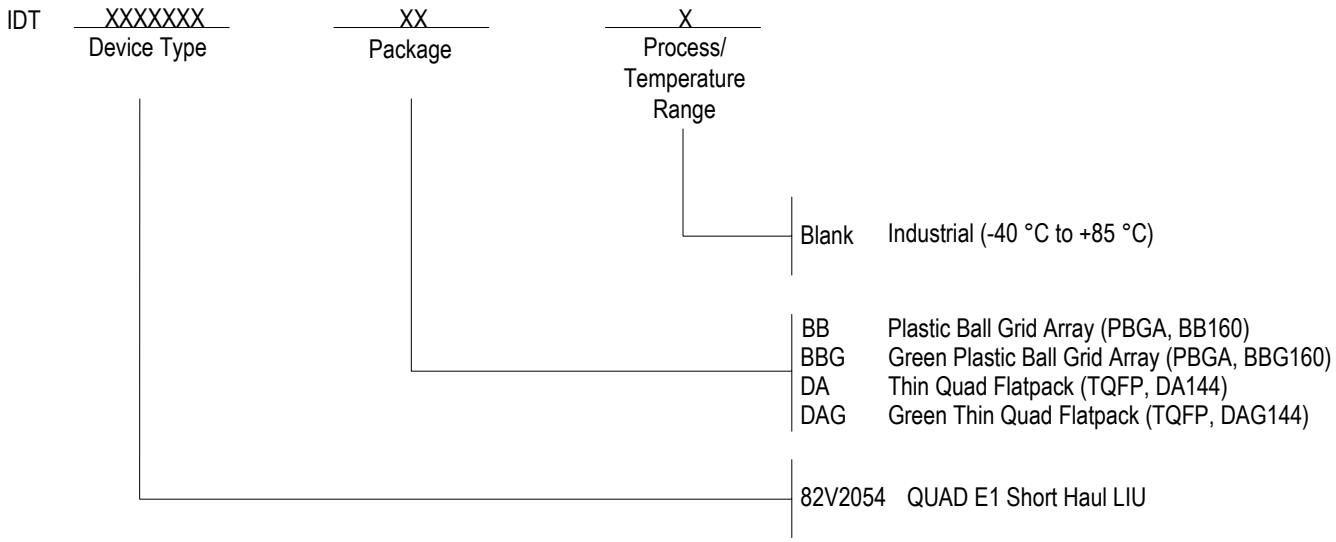
JITTER TRANSFER PERFORMANCE



Test condition: PRBS 2^15-1; Line code rule HDB3 is used.

Figure-38 Jitter Transfer Performance

ORDERING INFORMATION



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