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EXTERNAL ISSUE

## *DOCUMENT COVER PAGE*

**Note: This cover page establishes the Doc No., Title and current status of the attached document.**

| | | | | |
|---|---|---|---|---|
| Doc No. | SDSC-PSE-AN7135 | Issue Level | Rev | Eff Date |
| | | 1 | 5 | 23-FEB-06 |
| Doc Title | Product Specifications for AN7135 | Total no. of pages (excluding this page) | | 7 |

### Revision History

| Issue | Rev | Eff Date | S/N | Page | Change Details | Remarks |
|---|---|---|---|---|---|---|
| 1 | 4 | 15-FEB-04 | 1 | - | Added this cover page. | |
| | | | 2 | 6 | Removed this page. | |
| | | | 3 | 6A | Added this page for leadfree specification. | |
| | | | 4 | 6A | Amended Outer Lead Surface Process & | |
| | | | | | Chip Mounting Method. | |
| | 5 | 23-FEB-06 | 1 | 6A | Amended Outer Lead Surface process. | |

| Prepared | | Product Specifications | Ref No. | A-1 |
|---|---|---|---|---|
| Checked | | **AN7135** | Total Page | 7 |
| Approved | | | Page No. | 1 |

| | |
|---|---|
| Structure | Silicon Monolithic Bipolar IC |
| Appearance | FP12S Pin Plastic Package (with Fin) |
| Application | Low Frequency Power Amplifier |
| Function | 7.5W(3Ω) x 2 Channel Power amplifier<br>With Standby Function |

| A | Absolute Maximum Ratings | | | | |
|---|---|---|---|---|---|
| No. | Item | Symbol | Ratings | Unit | Note |
| 1 | Storage Temperature | Tstg | -55 ~ +150 | ° C | 1 |
| 2 | Operating Ambient Temperature | Topr | -30 ~ +75 | ° C | 1 |
| 3 | Operating Ambient Pressure | Popr | $1.013x10^5 \pm 0.61x10^5$ | Pa | |
| 4 | Operating Constant Acceleration | Gopr | 9,810 | $m/s^2$ | |
| 5 | Operating Shock | Sopr | 4,900 | $m/s^2$ | |
| 6 | Supply Voltage | $V_{CC}$ | 24 | V | |
| 7 | Supply Current | $I_{CC}$ | 4.0 | A | |
| 8 | Power Dissipation | $P_D$ | 62.5 | W | 2 |

| | | | |
|---|---|---|---|
| Operating Supply Voltage Range | $V_{CC}$ | 5V ~ 18V | Note 3 |

Note 1: The temperature of all item shall be Ta=25°C except storage temperature and operating ambient temperature.

Note 2: $R_{\theta j\text{-}c}$ = 2.0°C/W

Note 3: 24V during no signal.

| Eff. Date | Eff. Date | Eff. Date | Eff. Date |
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| 28-APR-94 | 20-APR-95 | 13-JUL-98 | 20-JUL-04 |

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| B | Electrical Characteristics (Unless otherwise specified, the ambient temperature is 25°C ± 2°C) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| No. | Item | Symbol | Test Cir-cuit | Conditions | Limits | | | Unit | Note |
| | | | | | min | typ | max | | |
| 1 | Quiescent Circuit Current | $I_{CQ}$ | 1 | $V_{IN}$=0mV | - | 14 | 20 | mA | |
| 2 | Output Noise Voltage | $V_{NO}$ | 1 | $V_{IN}$=0mV, $R_g$=10kΩ | - | 0.25 | 0.50 | mV | 1 |
| 3 | Voltage Gain | $G_V$ | 1 | $V_{IN}$=3mV | 42.5 | 44.5 | 46.5 | dB | |
| 4 | Total Harmonic Distortion | THD | 1 | $V_{IN}$=3mV | - | 0.40 | 0.75 | % | |
| 5 | Maximum Power Output | $P_O$ | 1 | THD=10% | 7.0 | 7.5 | - | W | |
| 6 | Channel Balance | CB | 1 | $V_{IN}$=3mV | -1 | 0 | +1 | dB | |
| 7 | Ripple Rejection | RR | 1 | Vcc(ripple) = 280mV<br>f(ripple) = 120Hz<br>Rg = 0Ω Sine wave | 45 | 50 | - | dB | 1 |
| 8 | Input Offset Voltage | $V_{IN\ (O.S)}$ | 1 | Input pin open | - | 10 | 30 | mV | |
| 9 | Standy-by current | $I_{STB}$ | 1 | Pin 3 open | - | - | 30 | μA | |

< Vcc = 15.0V, RL = 3Ω, Freq = 1kHz, Driving 2 channel >

Note 1) Use filter 15Hz ~ 30kHz (12dB/OCT) when measurement.

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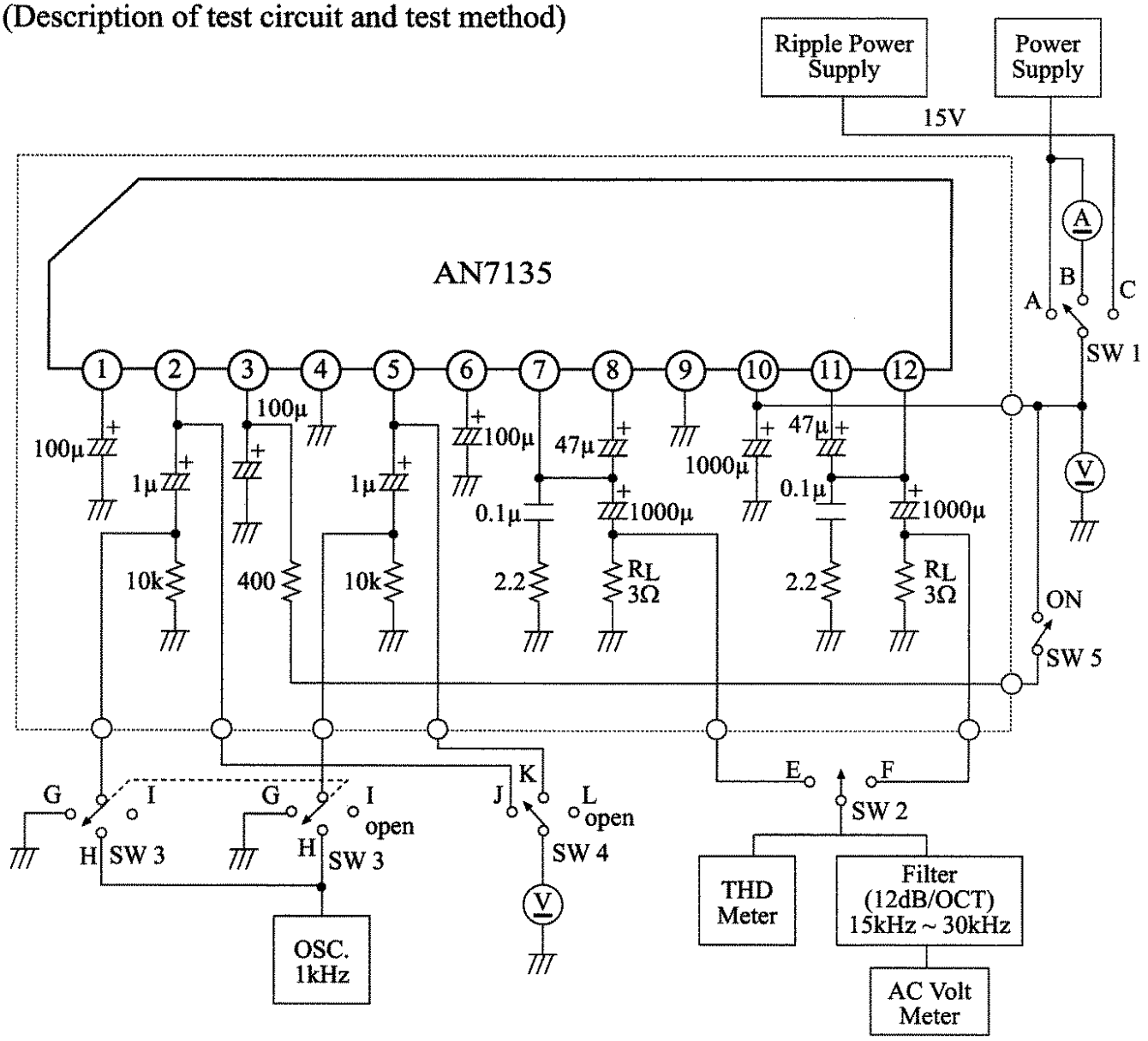
(Description of test circuit and test method)




| ITEM | SW 1 | SW 2 | SW 3 | SW 4 | SW 5 |
|---|---|---|---|---|---|
| B1 | B | - | G | L | ON |
| B2 | A | E or F | I | L | ON |
| B3 | A | E or F | H | L | ON |
| B4 | A | E or F | H | L | ON |
| B5 | A | E or F | H | L | ON |
| B6 | A | E or F | H | L | ON |
| B7 | C | E or F | G | L | ON |
| B8 | A | - | I | J or K | ON |
| B9 | A | - | I | - | OFF |

| Eff. Date | Eff. Date | Eff. Date | Eff. Date |
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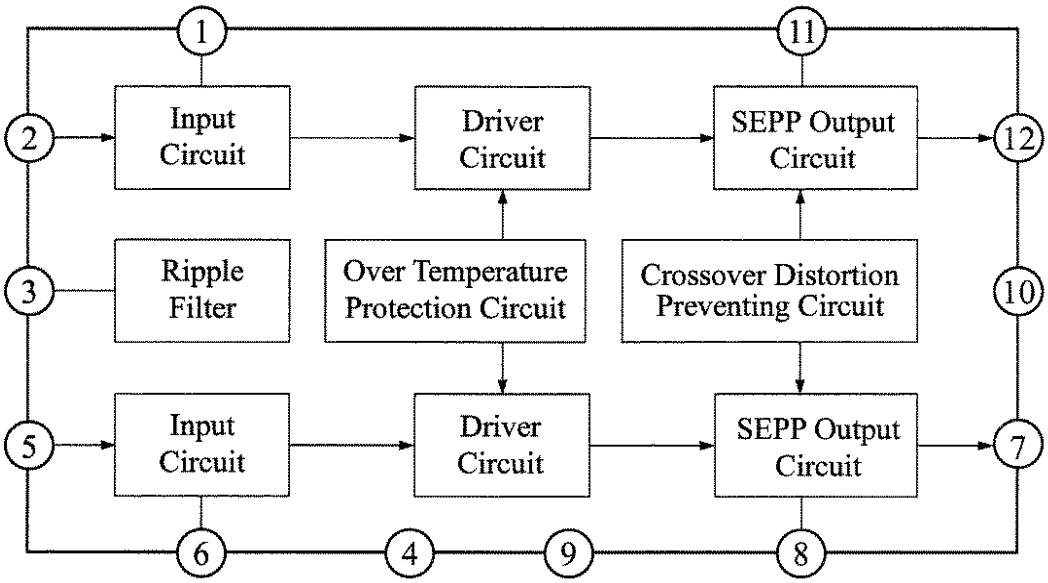
## Circuit Function Block Diagram




## Pin Descriptions

| Pin No. | Description | Pin No. | Description |
|---|---|---|---|
| 1 | Channel 1 negative feedback | 7 | Channel 2 output |
| 2 | Channel 1 input | 8 | Channel 2 bootstrap |
| 3 | Repple filter / Stand-by | 9 | GND (Output side) |
| 4 | GND (Input side) | 10 | Power supply |
| 5 | Channel 2 input | 11 | Channel 1 bootstrap |
| 6 | Channel 2 negative feedback | 12 | Channel 1 output |

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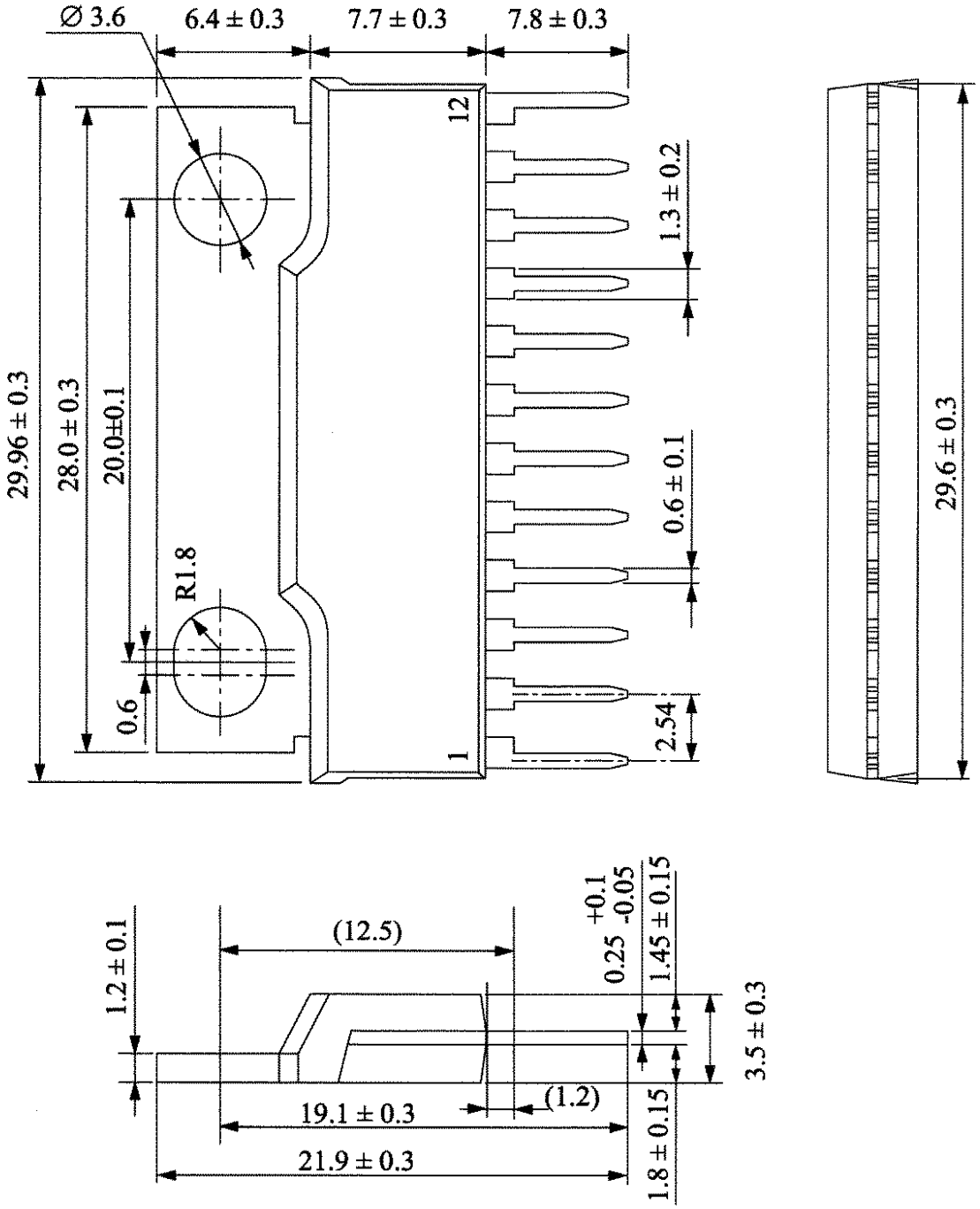
| Package Name | FP 12S |
|---|---|

Unit : mm




( ) : Reference value

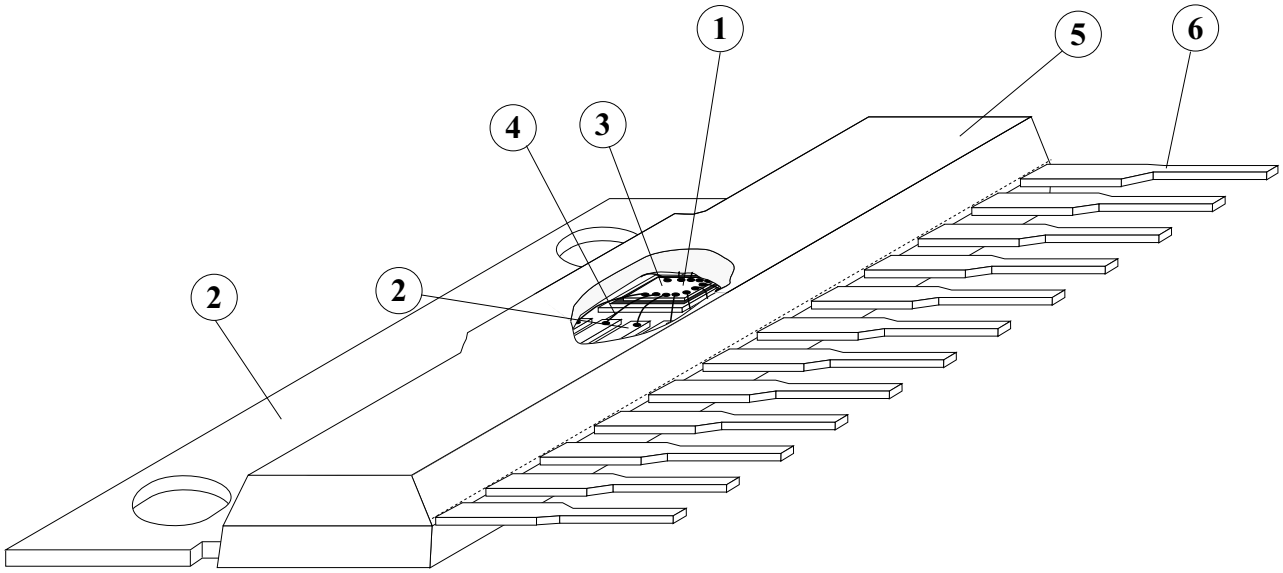
| Eff. Date | Eff. Date | Eff. Date | Eff. Date |
|---|---|---|---|
| 28-APR-94 | 20-APR-95 | 13-JUL-98 | 20-JUL-04 |

## (Structure Description)

| | | |
|---|---|---|
| Chip surface passivation | SiN, **PSG,** Others ( ) | 1 |
| Lead frame material | Fe group, **Cu group,** Others ( ) | 2, 6 |
| Inner lead surface process | **Ag plating,** Au plating, Others ( ) | 2 |
| *5 Outer lead surface process | General Customer: Solder Plating (98Sn-2Bi)<br>SC Buyback: Solder Dip (95.5Sn-2Ag-2Bi-0.5Cu) | 6 |
| Chip mounting method | Ag paste, Au-Si alloy, **Solder (95.5Pb-2.5Ag-2Sn)**,** | 3 |
| Wire bonding method | **Thermalsonic bonding,** Others ( ) | 4 |
| Wire material | **Au,** Others ( ) | 4 |
| Mold material | **Epoxy,** Others ( ) | 5 |
| Molding method | **Transfer mold,** Multiplunger mold, Others ( ) | 5 |
| Fin material | **Cu group,** Others ( ) | 7 |

** Under RoHS exemption clause, Lead (Pb) in high melting temperature type solder (ie. tin-lead solder alloy containing more than 85% of lead), is exempted until 2010.

**Package FP12S**




*5

(a) 62.50W Unlimited heatsink (θj-c = 2°C/W)

(b) 20.83W (θf=4.0°C/W)
Heat sink of 100cm² x 3mm Al (black lacquer) or
200cm² x 2mm Al (without lacquer)

(c) 15.63W (θf=6.0°C/W)
Heat sink of 100cm² x 2mm Al (without lacquer)

(d) 3.0W at Ta=30°C(θj-a=40°C/W) No Heat sink

## Power Dissipation $P_D$ -Ta