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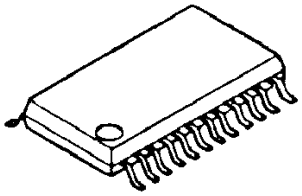
PRELIMINARY

CLASS D AMPLIFIER FOR DIGITAL AUDIO

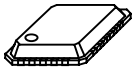
■ GENERAL DESCRIPTION

The **NJU8725** is an 800mW-output class D Amplifier featuring 6th ΔΣ modulation. It includes Digital Attenuator, Mute, and De-emphasis circuits. It converts digital source input to PWM signal output which is converted to analog signal with simple external LC low-pass filter. The **NJU8725** realizes very high power-efficiency by class D operation. Therefore, it is suitable for battery-powered applications and others.

■ PACKAGE OUTLINE



NJU8725V

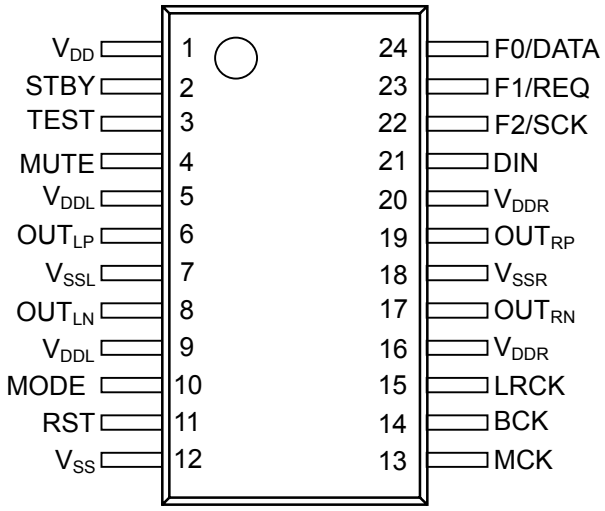


NJU8725KN1

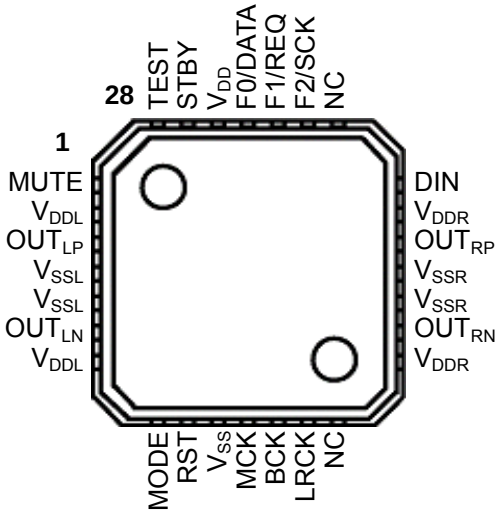
■ FEATURES

- Stereo BTL Power Amplifier
- Sixth-order $32f_S$ Over Sampling ΔΣ & PWM
- Internal $8f_S$ Over Sampling Digital Filter
- Sampling Frequency : 96kHz (Max.)
- De-Emphasis : 32kHz, 44.1kHz, 48kHz
- System Clock : $256f_S$
- Digital Processing : Attenuator 107step, LOG Curve
  : Mute
- Digital Audio Interface : 16bit, 18bit
  : I^2S, LSB Justified, MSB Justified
- Short Circuit Protection
- Operating Voltage : 2.4 to 3.6V
- Driving Voltage : V_{DD} to 5.25V
- C-MOS Technology
- Package Outline : SSOP24 / QFN28

■ PIN CONFIGURATION

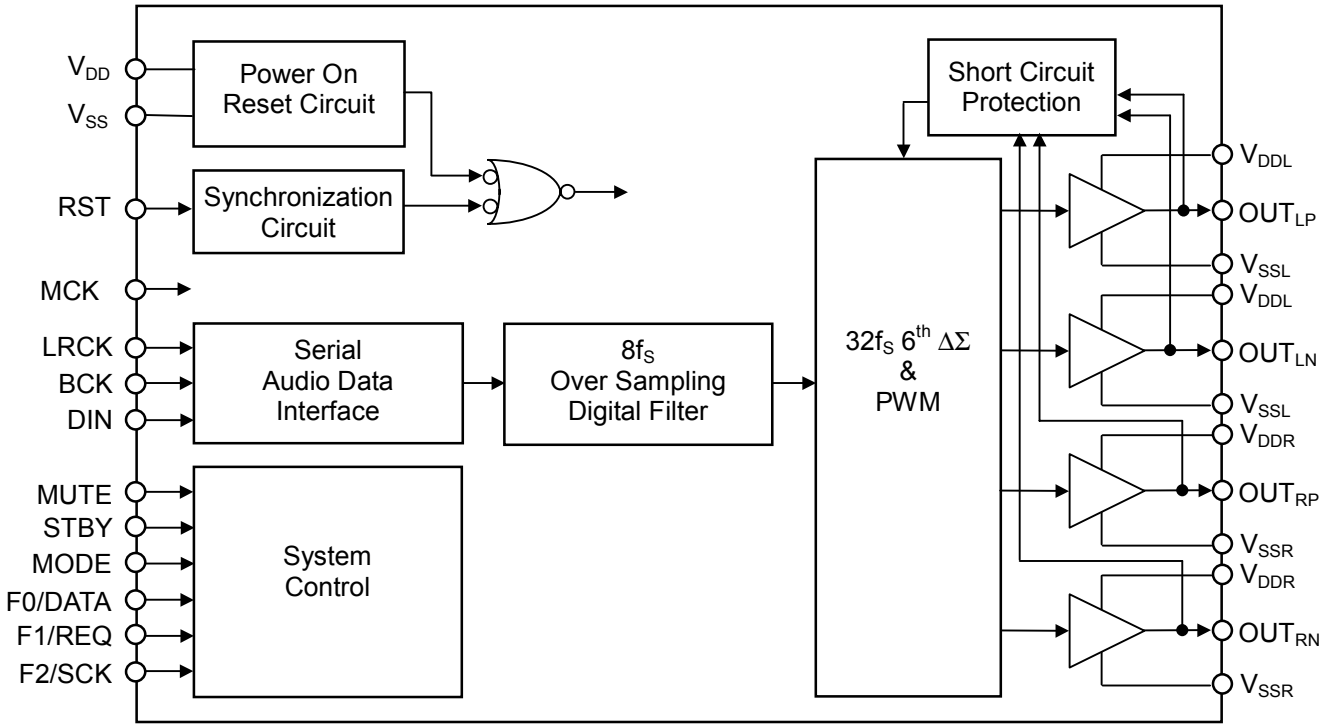


SSOP24



QFN28

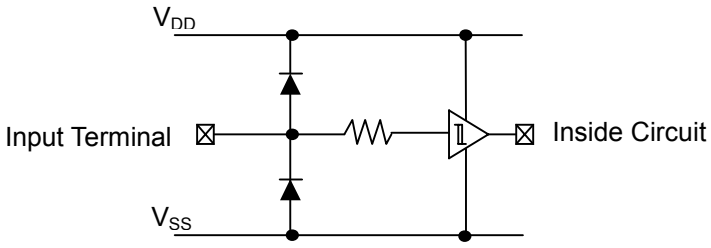
■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.		SYMBOL	I/O	FUNCTION
SSOP24	QFN28			
1	26	V_{DD}	–	Logic Power Supply, V_{DD}=3.3V
2	27	STBY	I	Standby Control Terminal Low : Standby ON High : Standby OFF
3	28	TEST	I	Manufacturer Testing Terminal Normally connect to GND.
4	1	MUTE	I	Mute Control Terminal Low : Mute ON High : Mute OFF
5	2	V_{DDL}	–	Lch Power Supply, V_{DDL}=V_{DD} to 5.0V
6	3	OUT_{LP}	O	Lch Positive Output Terminal
7	4,5	V_{SSL}	–	Lch Power GND, V_{SSL}=0V
8	6	OUT_{LN}	O	Lch Negative Output Terminal
9	7	V_{DDL}	–	Lch Power Supply, V_{DDL}=V_{DD} to 5.0V
10	8	MODE	I	Control Mode selection Terminal Low : Parallel Control Mode High : Serial Control Mode
11	9	RST	I	Reset Terminal Low : Reset ON High : Reset OFF
12	10	V_{SS}	–	Logic Power GND, V_{SS}=0V
13	11	MCK	I	Master Clock Input Terminal 256f_S clock inputs this terminal.
14	12	BCK	I	Serial Audio Data Bit Clock Input Terminal This clock must synchronize with MCK input signal.
15	13	LRCK	I	L/R Channel Clock Input Terminal This clock must synchronize with MCK input signal.
16	15	V_{DDR}	–	Rch Power Supply, V_{DDR}=V_{DD} to 5.0V
17	16	OUT_{RN}	O	Rch Negative Output Terminal
18	17,18	V_{SSR}	–	Rch Power GND, V_{SSR}=0V
19	19	OUT_{RP}	O	Rch Positive Output Terminal
20	20	V_{DDR}	–	Rch Power Supply, V_{DDR}=V_{DD} to 5.0V
21	21	DIN	I	Serial Audio Data Input Terminal
22	23	F2/SCK	I	MODE="Low" : Serial Audio Interface Format Selection Terminal 2 MODE="High" : Control Register Data Shift Clock Input Terminal The data is fetched into the control register by rise edge of SCK signal.
23	24	F1/REQ	I	MODE="Low" : Serial Audio Interface Format Selection Terminal 1 MODE="High" : Control Register Data Request Input Terminal
24	25	F0/DATA	I	MODE="Low" : Serial Audio Interface Format Selection Terminal 0 MODE="High" : Control Register Data Input Terminal
–	14,22	NC	–	Non connection

■ INPUT TERMINAL STRUCTURE



■ FUNCTIONAL DESCRIPTION

(1) Signal Output

PWM signals of L channel and R output from $OUT_{LP}/_{LN}$ and $OUT_{RP}/_{RN}$ terminals respectively. These signals are converted to analog signal by external 2nd-order or over LC filter. The output driver power supplied from V_{DDL}, V_{DDR}, V_{SSL}, and V_{SSR} are required high response power supply against voltage fluctuation like as switching regulator because Output THD is effected by power supply stability.

(2) Master Clock

Master Clock is $256f_S$ clock into MCK terminal for the internal circuit operation clock.

(3) Reset

"L" level input over than 3ms to the RST terminal is initialization signal to initialize the internal circuit. This initialization signal is synchronized with internal clock and executes logical OR with the internal power on reset signal. This Reset signal initializes the internal function setting registers also. During initialization, the output terminals are high-impedance.

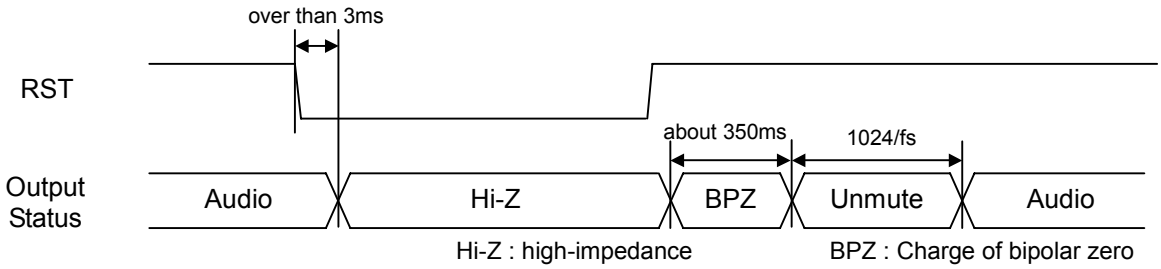


Figure 1. Reset Timing

(4) $8f_S$ Over Sampling Digital Filter

$8f_S$ Over Sampling Digital Filter interpolates Audio data and decreases aliasing noise.
It realizes Attenuation and De-Emphasis function by serial function control.

(5) $32f_S$ 6^{th} $\Delta\Sigma$ & PWM

$32f_S$ 6^{th} $\Delta\Sigma$ & PWM convert from Audio data of the $8f_S$ Over Sampling Digital Filter to the $32f_S$ one bit PWM data.

(6) Short Circuit Protection

Short Circuit Protection protects IC with output terminal of high-impedance condition when output terminal is shorted to GND or other output terminal.

The high-impedance condition is released automatically with master clock input, not released without master clock input.

(7) System Control

(7-1) Standby

Standby functions by “L” level input to the STBY terminal. In busy of Standby, conditions of digital audio format set, attenuation level, de-emphasis, and attenuator operation time are kept and output terminals are high-impedance.

(7-2) Control Mode Set

A control mode as shown below is selected by the MODE terminal.

MODE	Control Method	Function	Terminals
0	Parallel	Digital Audio interface Format Set	F0, F1, F2
1	Serial	Control Register serial data input	DATA, REQ, SCK

Parallel : Digital Audio Interface Format is set directly by using F0, F1, and F2 terminals.
Serial : **NJU8725** is controlled serial input data by 3-wire serial interface using DATA, REQ, and SCK terminals

By this setting, the function of F0/DATA, F1/REQ, and F2/SCK are changed.
Refer to「(8-5)F0,F1,F2」about function of F0, F1, and F2 terminals.
Refer to「(8)Control Register」about function of DATA, REQ, and SCK terminals.

(7-3) Mute

Mute functions by “L” signal into the MUTE terminal. In busy of mute, a current attenuation value becomes -∞ by internal digital attenuator. And MUTE is stopped by “H” signal into the MUTE terminal, the attenuation value returns from -∞ to previous value.

MUTE	Attenuation Level
0	-∞
1	Set Value

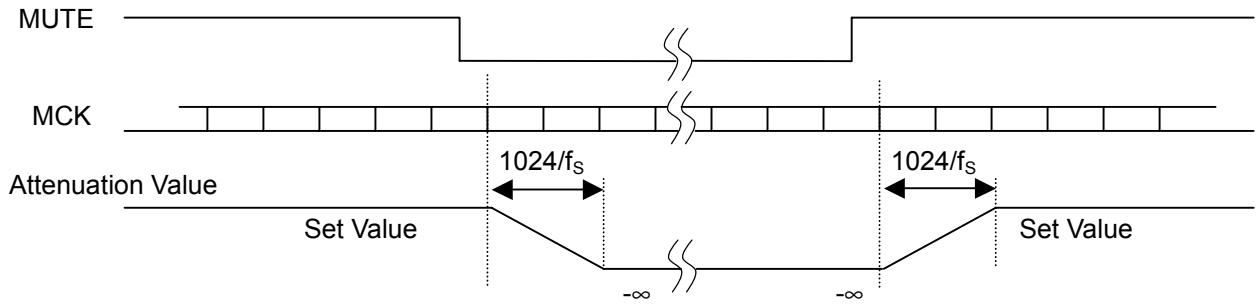


Figure 2. Mute Timing

(8) Serial Audio Data Interface

(8-1) Input Data Format Selection

The digital audio interface format is selected out of I^2S, MSB Justified or LSB Justified, and 16 bits or 18 bits data length.

(8-2) Input Timing

Digital audio signal data into DIN terminal is fetched into the internal shift register by BCK signal rising edge. The fetched data in the shift register are transferred by rising edge or falling edge of LRCK as shown below:

Data Format	Rising Edge	Falling Edge
I^2S	Lch Input Register	Rch Input Register
MSB Justified	Rch Input Register	Lch Input Register
LSB Justified	Rch Input Register	Lch Input Register

BCK and LRCK must be synchronized with MCK.

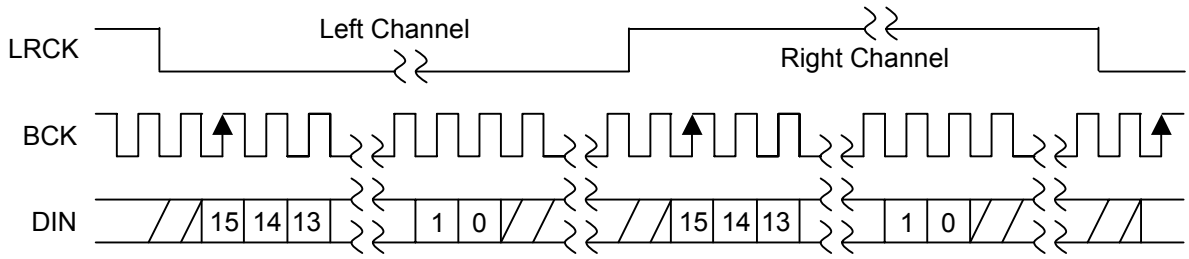


Figure 3.1. 16 bits I^2S Data Format

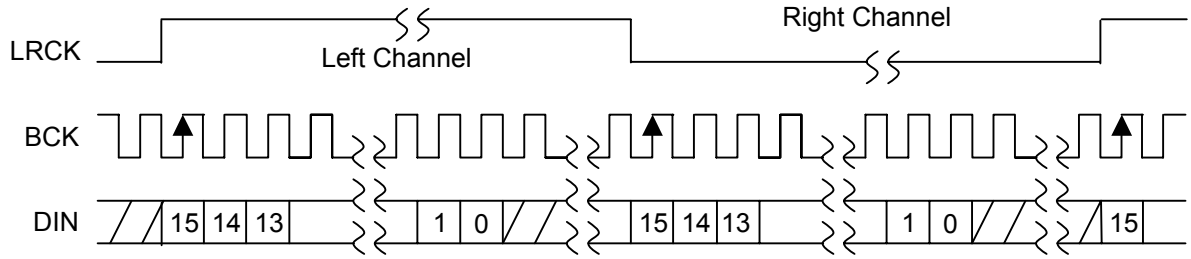


Figure 3.2. 16 bits MSB Justified Data Format

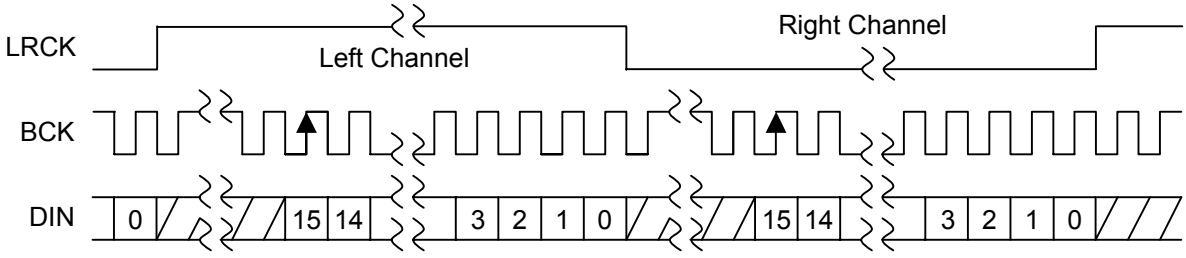


Figure 3.3. 16 bits LSB Justified Data Format

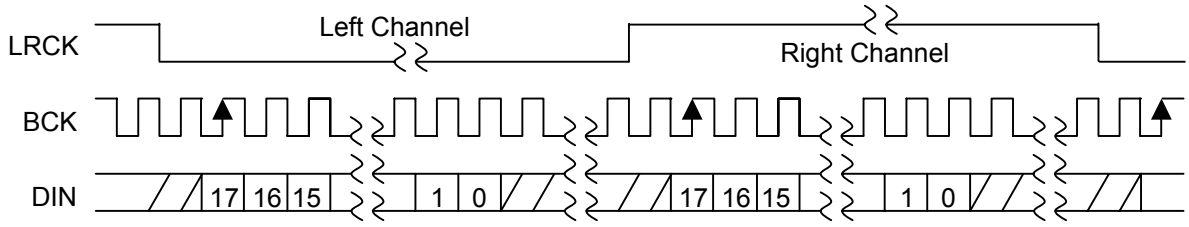


Figure 3.4. 18 bits I^2S Data Format

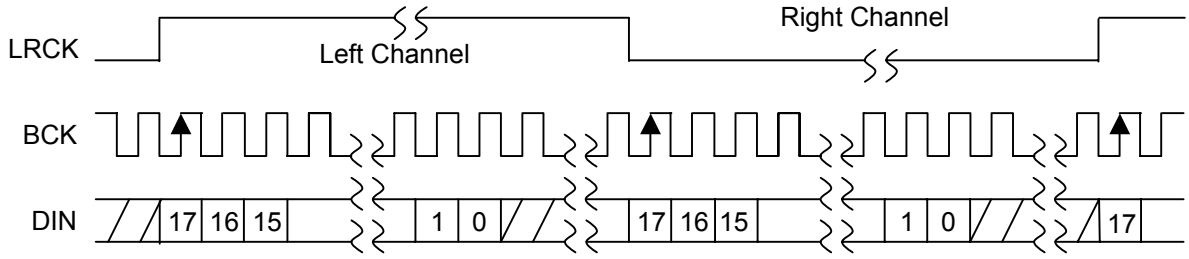


Figure 3.5. 18 bits MSB Justified Data Format

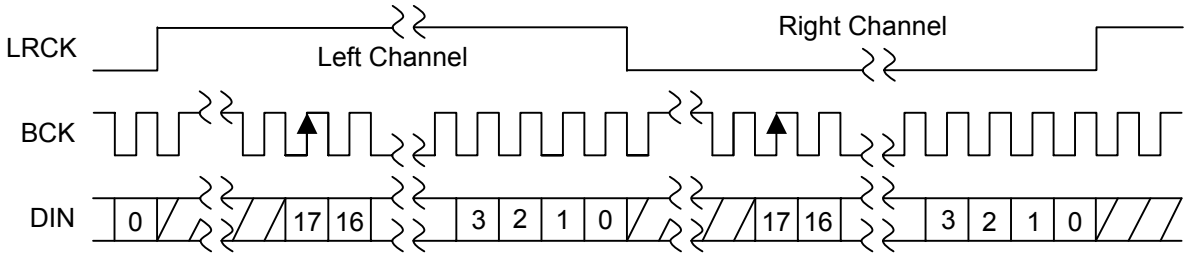


Figure 3.6. 18 bits LSB Justified Data Format

(8-3) Failure of Synchronization Operation

If the MCK clock fluctuates over than ±10 clocks against the LRCK and failure of synchronization is detected the attenuation value is set to -∞. When the LRCK synchronizes with MCK again, the attenuation value returns from -∞ to previous level.

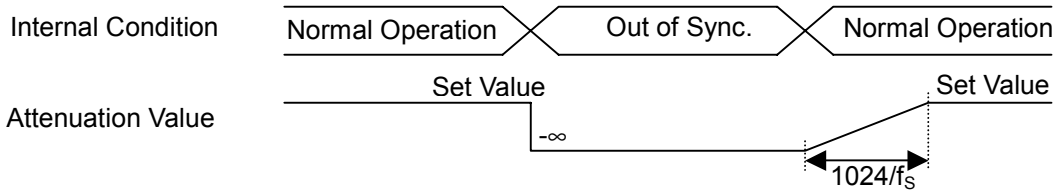


Figure 4. Out of Synchronization Operation

(9) Control Register

When Control Mode is set to Serial control by the Mode terminal, the control register sets various modes. The Control Data is fetched by the rising edge of F2/SCK and is set into the control register by the rising edge of F1/REQ. The latest 8 bits data are valid before the F1/REQ rising pulse.

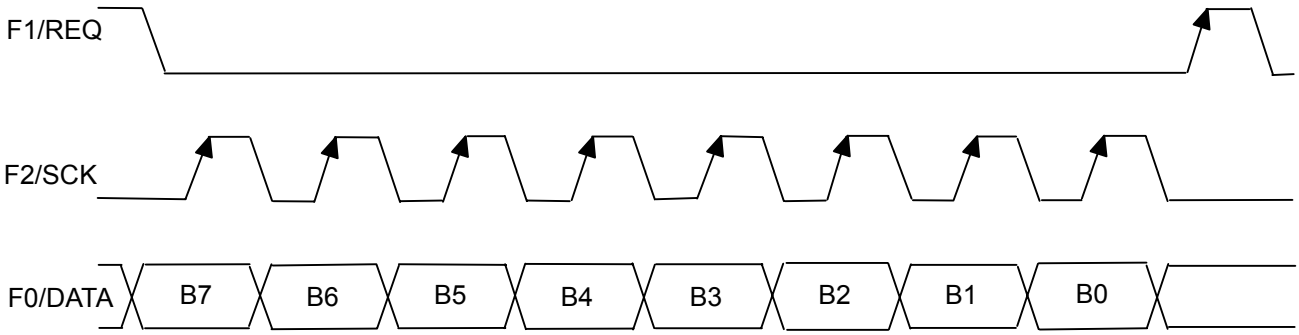


Figure 5. Control Register Timing

(9-1) Serial Data Format

B7	B6	B5	B4	B3	B2	B1	B0
0	ATTN6	ATTN5	ATTN4	ATTN3	ATTN2	ATTN1	ATTN0
1	0	0	0	0	0	DEMP1	DEMP0
1	0	0	1	F2	F1	F0	MUTE
1	0	1	0	0	0	0	RST
1	1	0	0	0	0	0	TEST
1	1	0	1	0	0	0	0
1	1	1	0	0	MUTT2	MUTT1	MUTT0
1	1	1	1	0	0	0	TRST

Do not set other data excepting this table.

(9-2) ATTN6 to ATTN0

When B7 is “0”, B0 to B6 set the attenuation data. When attenuation data is set, the attenuation value is changed to the target value in the period of transition time set by MUTT0 to MUTT2. The attenuation value (ATT) is fixed by following formula.

When ATT is 14h or less, the attenuator is set -∞ at reset. (When Control Mode is Parallel Control, ATT is fixed 0db.)

ATT=DATA -121[dB] DATA : attenuation point

7Fh=6 dB
7Eh=5dB
7Dh=4dB
:
79h=0dB
:
16h=-99dB
15h=-100dB
14h=-∞
13h=-∞
:
00h=-∞ (initial value)

(9-3) DEMP0, DEMP1

DEMP0 and DEMP1 control De-Emphasis on/off and sampling frequency.

DEMP1	DEMP0	De-Emphasis	Initial Value
0	0	OFF	✓
0	1	32kHz	
1	0	44.1kHz	
1	1	48kHz	

(9-4) MUTE

Mute operation is controlled by the “MUTE” as same as the MUTE terminal control.

MUTE	Mute Operation	Initial Value
0	OFF	✓
1	ON	

(9-5) F0, F1, F2

F0, F1, and F2 select Digital Audio Interface Format. As same as the F0/DATA, F1/REQ, and F2/SCK terminal control.

F0	F1	F2	Interface Format	Bit Length	Initial Value
0	0	0	I^2S	16	✓
0	0	1	MSB Justified	16	
0	1	0	LSB Justified	16	
1	0	0	I^2S	18	
1	0	1	MSB Justified	18	
1	1	0	LSB Justified	18	

(9-6) RST

When the RST is “1”, the control register and inner data (Digital filter, PWM modulator) are initialized.

RST	Reset Operation	Initial Value
0	OFF	✓
1	ON	

(9-7) TRST

When the TRST is “1”, only inner data (Digital filter, PWM modulator) is initialized.

TRST	Data Bus Initialize	Initial Value
0	OFF	✓
1	ON	

(9-8) MUTT2 to MUTT0

MUTT2 to MUTT0 set the attenuator transition time. This transition time is one attenuation step change time.

MUTT2	MUTT1	MUTT0	Operation Time	Initial Value
0	0	0	$1 / f_S$	✓
0	0	1	$2 / f_S$	
0	1	0	$4 / f_S$	
0	1	1	$8 / f_S$	
1	0	0	$16 / f_S$	
1	0	1	$32 / f_S$	
1	1	0	$64 / f_S$	
1	1	1	$128 / f_S$	

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage		V_{DD} V_{DDL} V_{DDR}	-0.3 to +4.0 -0.5 to +5.5 -0.5 to +5.5	V V V
Input Voltage		Vin	-0.3 to V_{DD}+0.3	V
Operating Temperature		Topr	-40 to +85	°C
Storage Temperature		Tstg	-40 to +125	°C
Power Dissipation	SSOP24	P_D	600	mW
	QFN28		640 *	

* : Mounted on two-layer board of based on the JEDEC.

Note 1) All voltage values are specified as V_{SS}= V_{SSR}= V_{SSL}=0V.

Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 3) Decoupling capacitors should be connected between V_{DD}-V_{SS}, V_{DDR}-V_{SSR} and V_{DDL}-V_{SSL} due to the stabilized operation.

■ ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{DD}=V_{DDL}=V_{DDR}=3.3V, f_S=44.1kHz, Input Signal=1kHz, Input Signal Level at Full Scale Output, MCK=256f_S, Load Impedance=8Ω, Measuring Band=20Hz to 20kHz, 2nd-order 34kHz LC Filter (Q=0.85), unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	Note
V_{DDL}, V_{DDR} Supply Voltage			V_{DD}	-	5.25	V	
V_{DD} Supply Voltage			3.0	3.3	3.6	V	
Output Power Efficiency	Eeff	Vo= 0dB	80	-	-	%	4
Output THD	THD	Vo=-6dB	-	-	0.1	%	
Output Power	Po	Vo= 0dB	TBD	800	-	mW/ch	
S/N	SN	A weight	85	90	-	dB	
Dynamic Range	Drange	A weight	85	90	-	dB	
Channel Separation	Echn	EIAJ(1kHz)	60	-	-	dB	
Output Level Difference Between Lch and Rch	CHD		-	-	3	dB	
Maximum Mute Attenuation	MAT		90	-	-	dB	
Passband Response	PR	20Hz to 20kHz	-	-	±1	dB	
Power Supply Current At Standby	I_{ST}	Stopping MCK, BCK, LRCK, DIN	-	-	10	μA	
Power Supply Current At Operating	I_{DD}	No-load operating No signal inputted	-	13	20	mA	
Input Voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V	
	V_{IL}		0	-	0.3V_{DD}	V	
Input Leakage Current	I_{LK}		-	-	±1.0	μA	

Note 4)

$$\text{Power Efficiency (\%)} = \frac{\text{OUT}_L \text{ Output Power} + \text{OUT}_R \text{ Output Power (W)}}{V_{DDL} \text{ Supply Power} + V_{DDR} \text{ Supply Power (W)}} \times 100$$

Note 5) Analog AC Characteristics Test System

Analog AC characteristics test system is shown in Figure 6. The analog AC characteristics of **NJU8725** is measured with 2nd-order LC LPF on the test board and Filters in the Audio Analyzer.

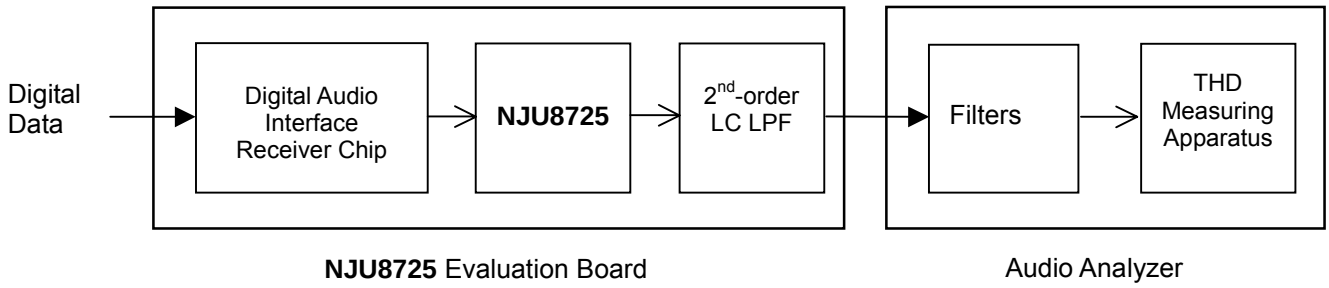
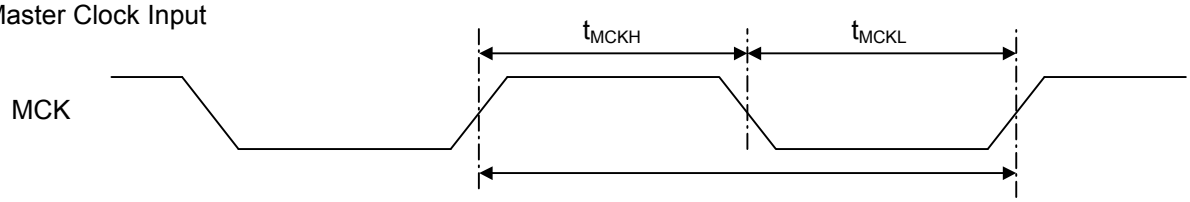


Figure 6. Analog AC Characteristics Measurement System

2nd-order LPF : fc=34kHz, refer to the LPF on Application Circuit.
Filters : 22Hz HPF + 20kHz 10th-order LPF
(with the A-Weighting Filter at measuring S/N and Dynamic-range)

■ TIMING CHARACTERISTICS

- Master Clock Input

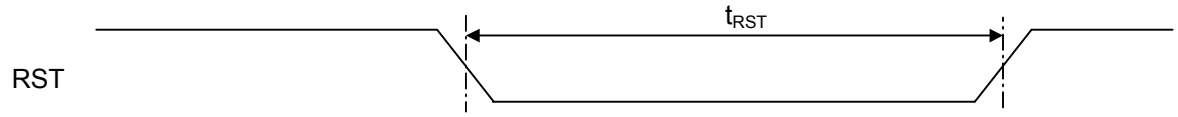


(Ta=25°C, V_{DD}=V_{DDL}=V_{DDR}=3.3V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MCK Frequency	f_{MCKI}	256f_S	7.28	-	27.648	MHz
MCK Pulse Width (H)	t_{MCKH}		12	-	-	ns
MCK Pulse Width (L)	t_{MCKL}		12	-	-	ns

Note 6) t_{MCKI} shows the cycle of the MCK signal.

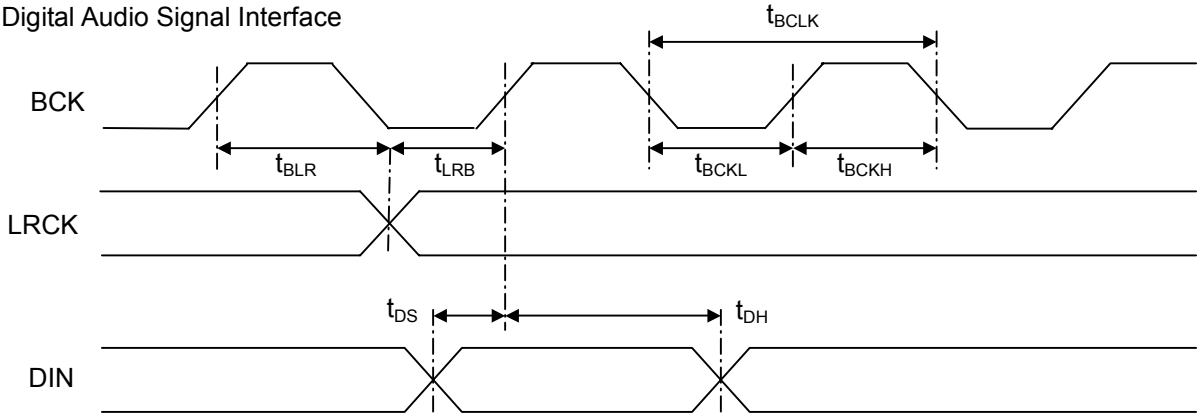
- Reset Input



(Ta=25°C, V_{DD}=V_{DDL}=V_{DDR}=3.3V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset Low Level Width	t_{RST}		3	-	-	ms

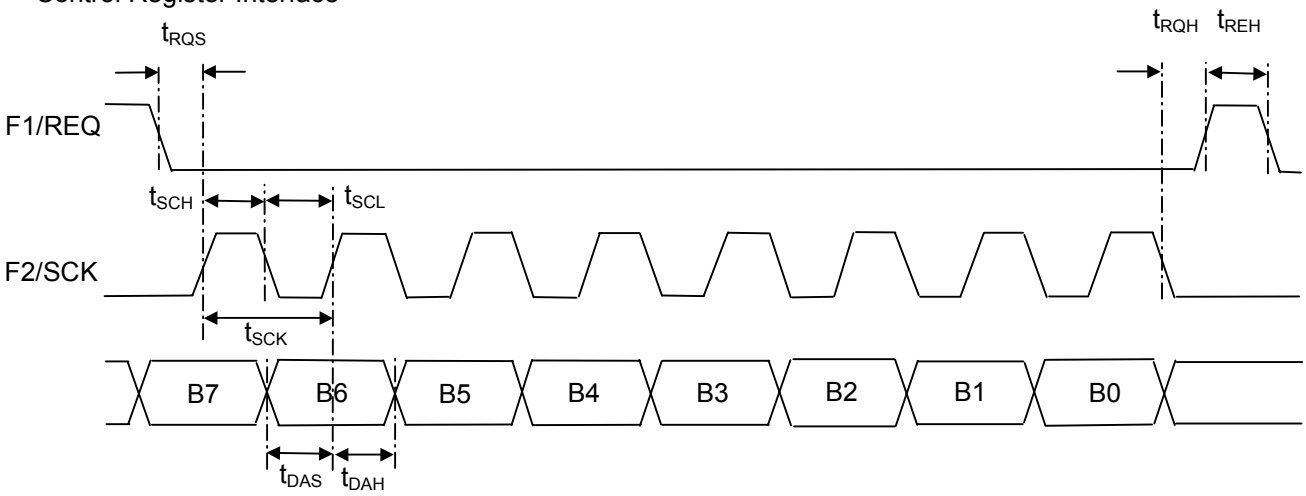
- Digital Audio Signal Interface



(Ta=25°C, V_{DD}=V_{DDL}=V_{DDR}=3.3V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio DAC Sampling Rate	f_S		28	-	100	KHz
DIN Setup Time	t_{DS}		20	-	-	ns
DIN Hold Time	t_{DH}		20	-	-	ns
BCK Period	t_{BCLK}		1/(128f_S)	-	-	ns
BCK Pulse Width (H)	t_{BCKH}		20	-	-	ns
BCK Pulse Width (L)	t_{BCKL}		20	-	-	ns
LRCK Hold Time	t_{BLR}		20	-	-	ns
LRCK Setup Time	t_{LRB}		20	-	-	ns

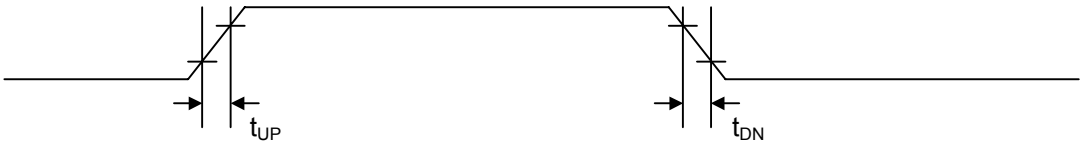
- Control Register Interface



(Ta=25°C, V_{DD}=V_{DDL}=V_{DDR}=3.3V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
F2/SCK Period	t_{SCK}		2	-	-	µs
F2/SCK Pulse Width (H)	t_{SCH}		0.8	-	-	µs
F2/SCK Pulse Width (L)	t_{SCL}		0.8	-	-	µs
F0/DATA Setup Time	t_{DAS}		0.8	-	-	µs
F0/DATA Hold Time	t_{DAH}		0.8	-	-	µs
F1/REQ Pulse Width (H)	t_{REH}		1.6	-	-	µs
F2/SCK Setup Time	t_{RQS}		0.8	-	-	µs
F1/REQ Hold Time	t_{RQH}		0.8	-	-	µs

- Input Signal Rise and Fall Time



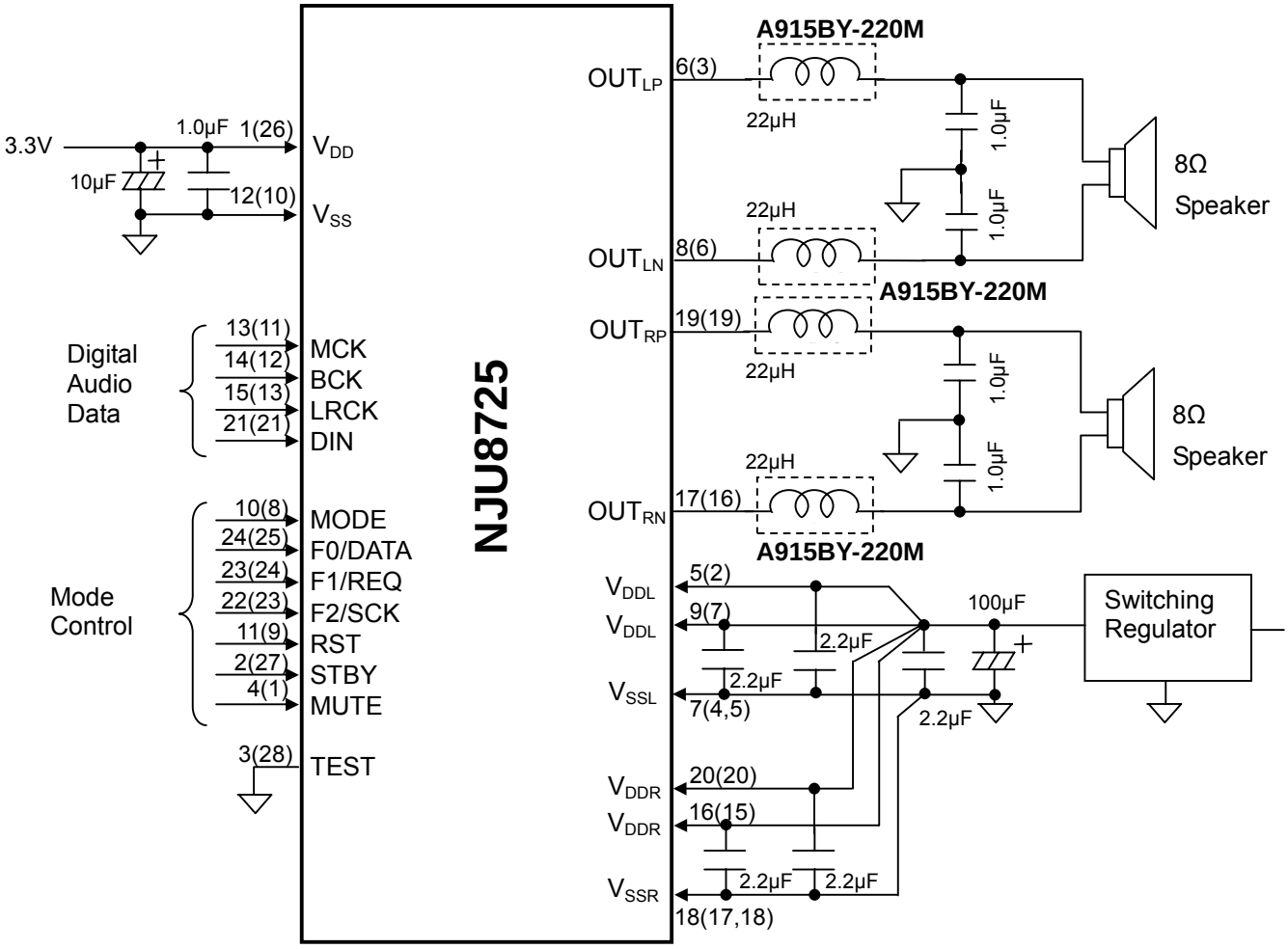
(Ta=25°C, V_{DD}=V_{DDL}=V_{DDR}=3.3V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise Time	t_{UP}		-	-	100	ns
Fall Time	t_{DN}		-	-	100	ns

Note 7) All timings are based on 30% and 70% voltage level of V_{DD}.

■ APPLICATION CIRCUIT

•A915BY-220M is manufactured by TOKO, INC.
For further information, please refer to its technical papers.



* () indicates pin number of QFN28.

Note 8) De-coupling capacitors must be connected between each power supply pin and GND pin.
Note 9) The power supply for V_{DDL} and V_{DDR} require fast driving response performance such as a switching regulator for THD.
Note 10) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please consider and check the circuit carefully to fit your application.