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DOCUMENT COVER PAGE

APPROVED
EXTERNAL ISSUE

Note: This cover page establishes the Doc No., Title and current status of the attached document.

Doc No.	SDSC-PSE-AN17822A	Issue Level	Rev	Eff Date
		1	2	28-MAR-05
Doc Title	Product Specifications for AN17822A	Total no. of pages (excluding this page)		17

Revision History

Issue	Rev	Eff Date	S/N	Page	Change Details	Remarks
1	1	16-DEC-04	1	-	Added this cover page.	
			2	7	Removed this page.	
			3	7A	Added this page for leadfree specification.	
			4	7A	Amended Outer Lead Surface Process &	
					Chip Mounting Method.	
	2	28-MAR-05	1	6	Removed physical product marking indications.	

Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pin Plastic Package (Power Type with Fin)
Application	Low Frequency Amplifier
Function	BTL 5.0W x 2ch Power Amplifier with Standby Function and Volume Function

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	°C	1
2	Operating Ambient Temperature	Topr	-25 ~ +70	°C	1
3	Operating Ambient Pressure	Popr	$1.013 \times 10^5 \pm 0.61 \times 10^5$	Pa	
4	Operating Constant Acceleration	Gopr	9810	m/s^2	
5	Operating Shock	Sopr	4900	m/s^2	
6	Supply Voltage	Vcc	14.4	V	2
7	Supply Current	Icc	2.0	A	
8	Power Dissipation	Pd	1.92	W	Ta=70°C

Operating Supply Voltage Range	Vcc	3.5V ~ 13.5V

Note 1: The temperature of all items shall be Ta = 25°C except storage temperature and operating ambient temperature.
Note 2: At no signal input

B	Electrical Characteristics	(Unless otherwise specified, the ambient temperature is 25°C ±2°C, Vcc = 8.0V, frequency = 1kHz and RL = 8Ω)							
No	Item	Symbol	Test Cct.	Conditions	Limits			Unit	Note
					Min	Typ	Max		
1	Quiescent Circuit Current	I_{CQ}	1	Vin = 0V, Vol = 0V	-	45	100	mA	
2	Standby Current	I_{STB}	1	Vin = 0V, Vol = 0V	-	1	10	μA	
3	Output Noise Voltage	V_{NO}	1	Rg = 10kΩ, Vol = 0V	-	0.25	0.4	mVrms	1
4	Voltage Gain	G_V	1	Po = 0.5W, Vol = 1.25V	39	41	43	dB	
5	Total Harmonic Distortion	THD	1	Po = 0.5W, Vol = 1.25V	-	0.20	0.5	%	
6	Maximum Power Output 1	Po1	1	THD = 10%, Vol = 1.25V	2.4	3.0	-	W	
7	Maximum Power Output 2	Po2	1	Vcc = 11V THD = 10%, Vol = 1.25V	4.0	5.0	-	W	
8	Ripple Rejection Ratio	RR	1	Rg = 10kΩ, Vol = 0V Vr = 0.5Vrms, fr = 120Hz	30	50	-	dB	1
9	Output Offset Voltage	V_{off}	1	Rg = 10kΩ, Vol = 0V	-200	0	200	mV	
10	Volume Attenuation Ratio	Att	1	Po = 0.5W, Vol = 0V	70	80	-	dB	1
11	Channel Balance 1	CB1	1	Po = 0.5W, Vol = 1.25V	-1	0	1	dB	
12	Channel Balance 2	CB2	1	Po = 0.5W, Vol = 0.6V	-2	0	2	dB	
13	Middle Voltage Gain	G_{Vm}	1	Po = 0.5W, Vol = 0.6V	27.5	30.5	33.5	dB	
14	Channel Crosstalk	CT	1	Po = 0.5W, Vol = 1.25V	40	55	-	dB	

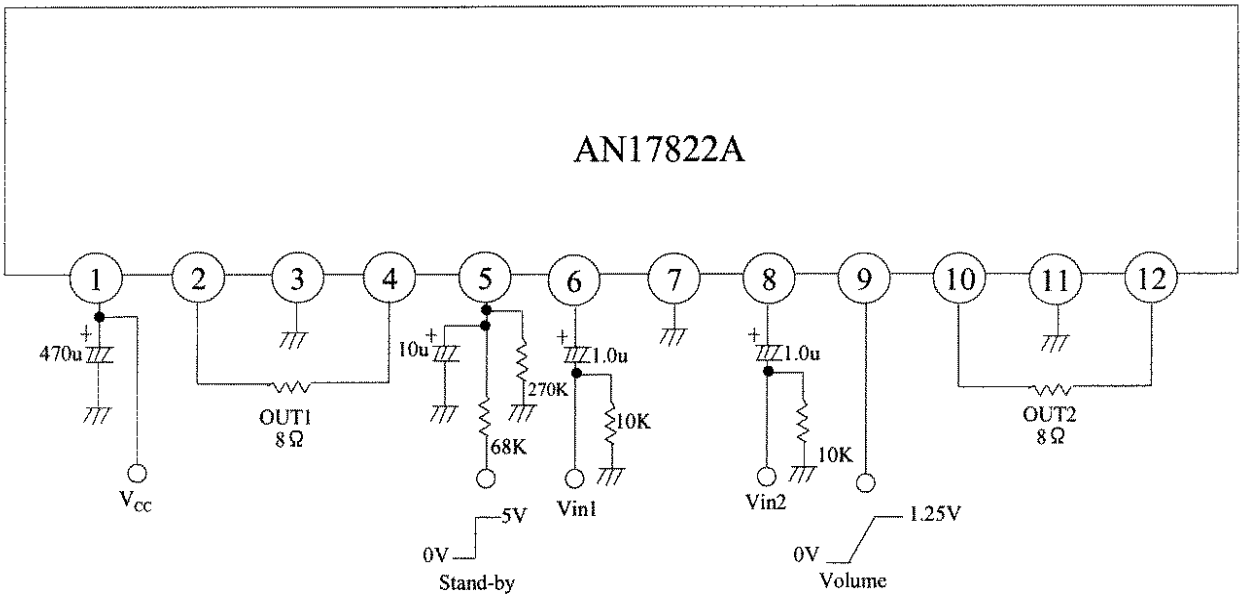
Note 1) For this measurement, use the BPF = 15Hz ~ 30kHz (12dB/OCT)

B	Electrical Characteristics	(Unless otherwise specified, the ambient temperature is 25°C ±2°C, Vcc = 8.0V, frequency = 1kHz and RL = 8Ω)							
No	Item	Symbol	Test Cct.	Conditions	Limits			Unit	Note
					Min	Typ	Max		
1	Standby pin current	I_{STB2}	1	Vin = 0V, V_{STB} = 3.0V	-	-	25	μA	
2	Volume pin current	I_{VOL}	1	Vin = 0V, Vol = 0V	-12	-	-	μA	
3	Input Impedance	Zi	1	Vin = ±0.3V_{DC}	24	30	36	kΩ	

Note) The above characteristics are reference values determined for IC design, but not guaranteed values for shipping inspection. If problems were to occur, counter measures will be sincerely discussed.

(Description of test circuit and test method)

Test Circuit 1

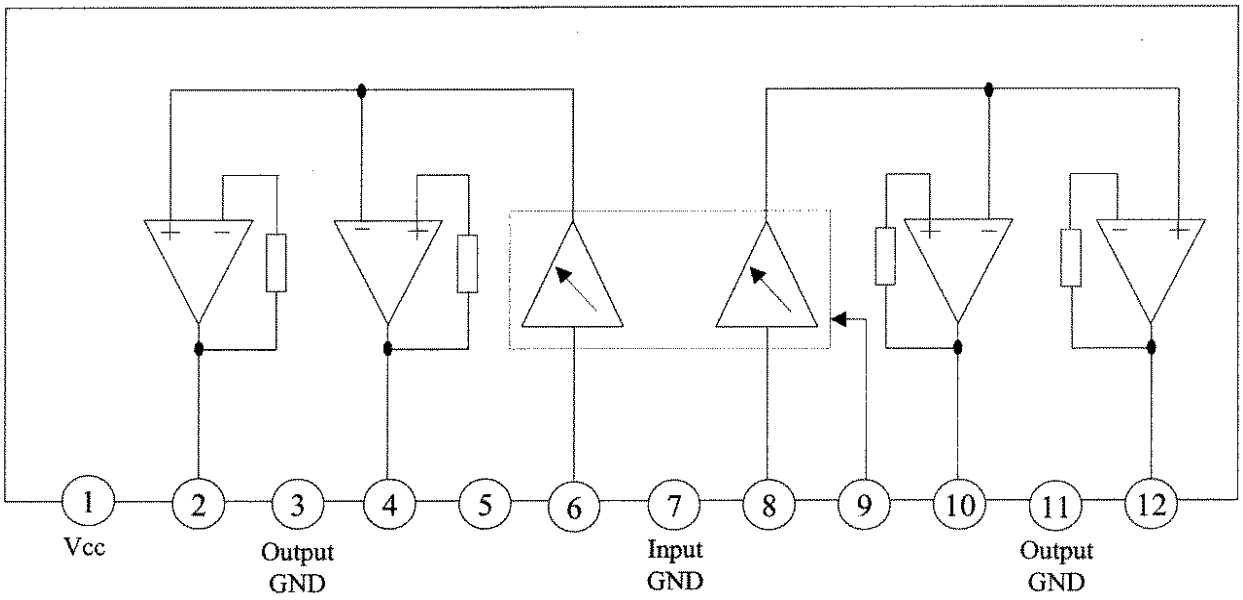


Note) If the standby pin is open or 0V, the IC is on standby state.

The IC is in the state of volume minimum if the Volume pin is ground.

The IC is in the state of volume maximum if the Volume pin is open.

Circuit Function Block Diagram



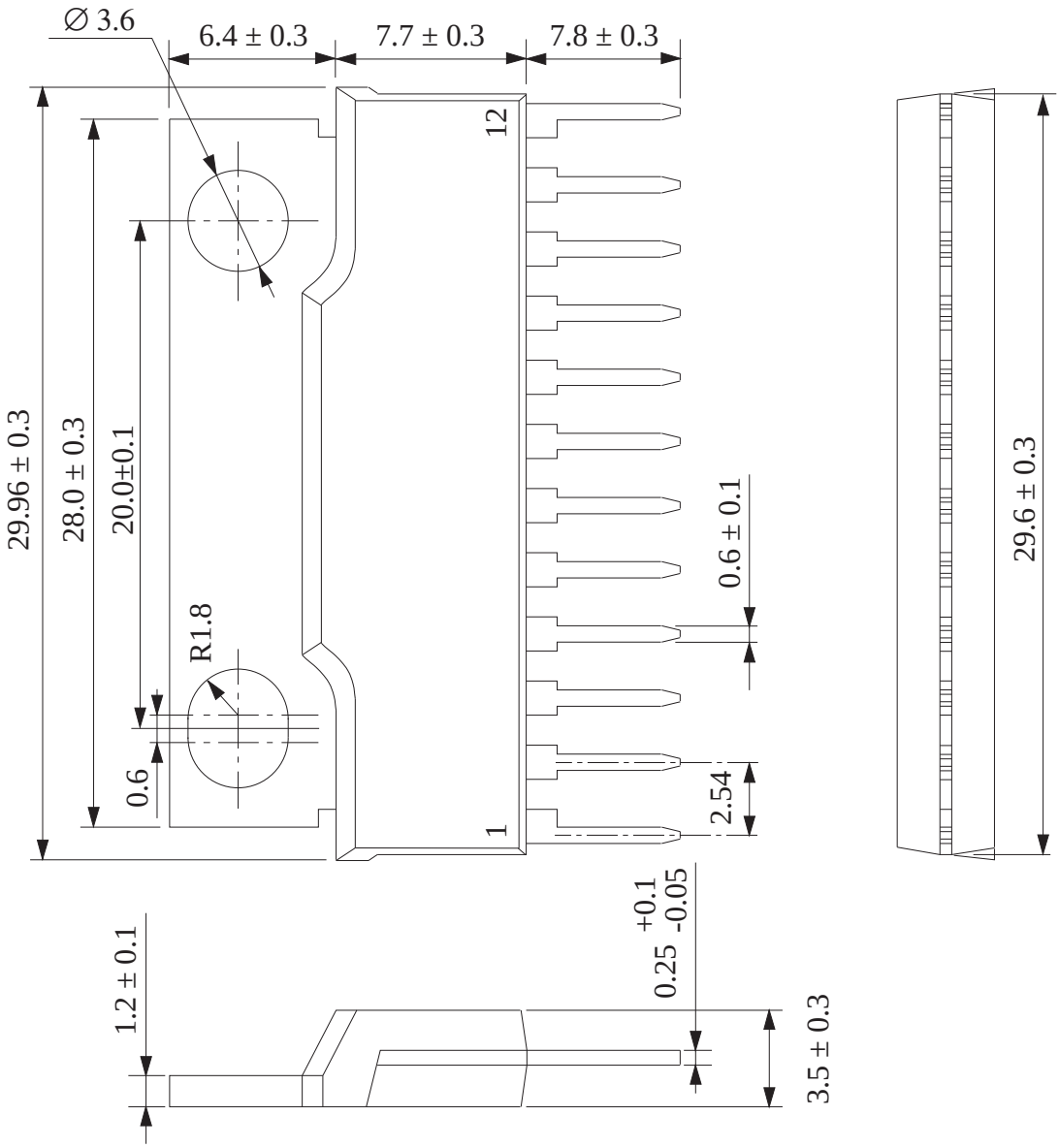
Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Vcc	7	GND (Input)
2	Ch.1 Output (+)	8	Ch.2 Input
3	GND (Ch. 1 Output)	9	Volume
4	Ch.1 Output (-)	10	Ch.2 Output (-)
5	Standby	11	GND (Ch.2 Output)
6	Ch.1 Input	12	Ch.2 Output (+)

12-SIL(FP)

Package Name	FP-12S

Unit : mm



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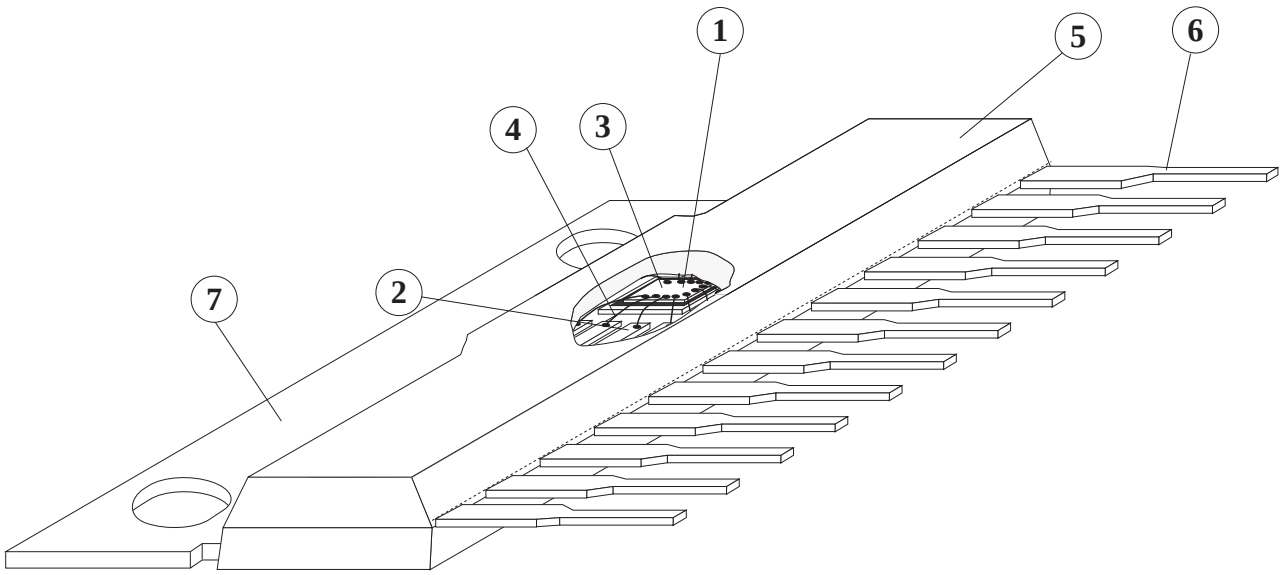
24-DEC-2003	-	28-MAR-05	

(Structure Description)

Chip surface passivation	[SiN,] PSG, Others ( )	1
Lead frame material	Fe group, [Cu group,] Others ( )	2, 6
Inner lead surface process	[Ag plating,] Au plating, Others ( )	2
*1 Outer lead surface process	[Solder plating (98Sn-2Bi),] Solder dip, Others ( )	6
*1 Chip mounting method	Ag paste, Au-Si alloy, [Solder (95.5Pb-2.5Ag-2Sn)**]	3
Wire bonding method	[Thermalsonic bonding,] Others ( )	4
Wire material	[Au,] Others ( )	4
Mold material	[Epoxy,] Others ( )	5
Molding method	[Transfer mold,] Multiplunger mold, Others ( )	5
Fin material	[Cu group,] Others ( )	7

Package FP-12S

**Under RoHS exemption clause, Lead (Pb) in high melting temperature type solder (i.e. tin-lead solder alloys containing more than 85% of lead), is exempted until 2010.

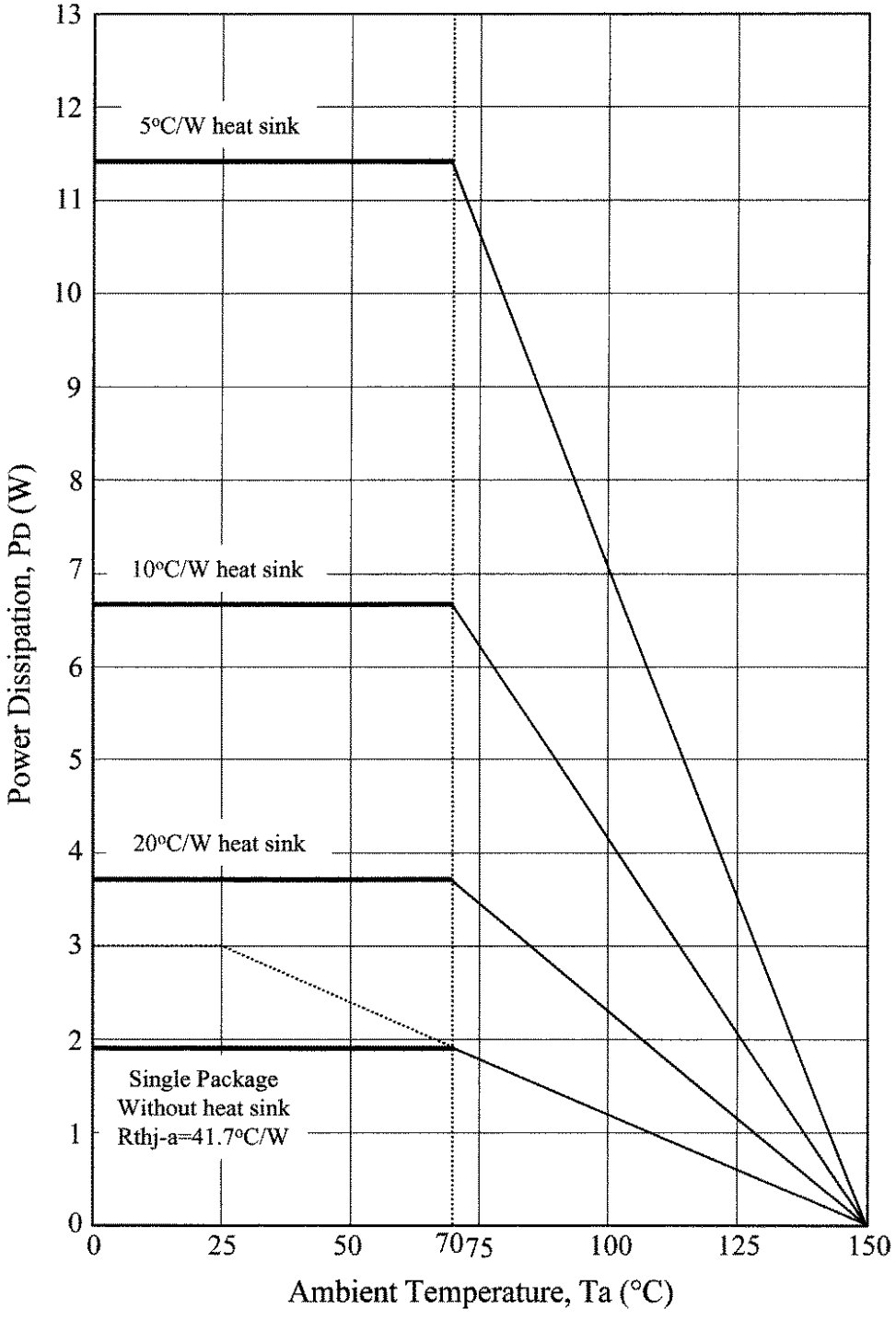


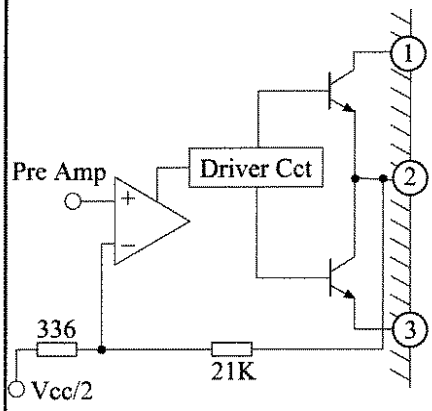
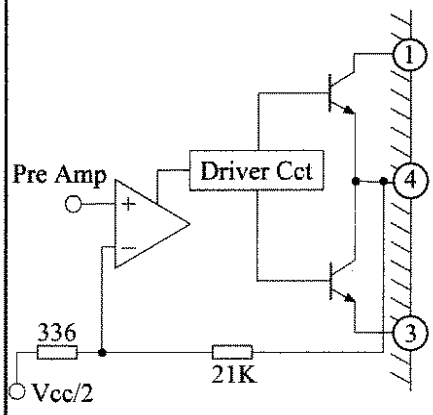
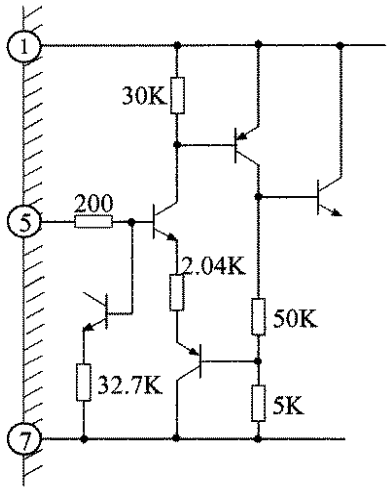
*1

(Rth(j-c) = 2°C/W
Rth(j-a) = 41.7°C/W)

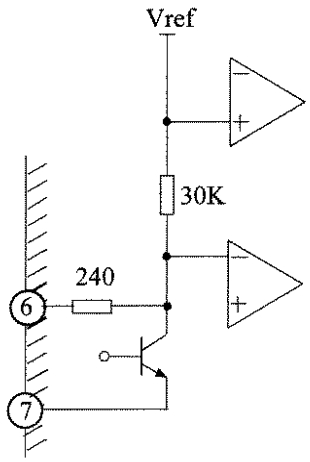
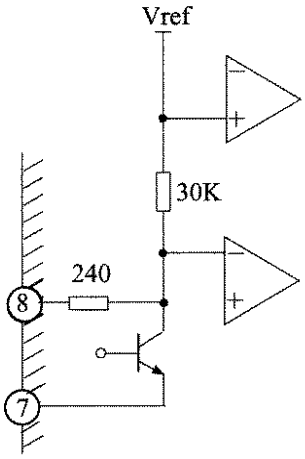
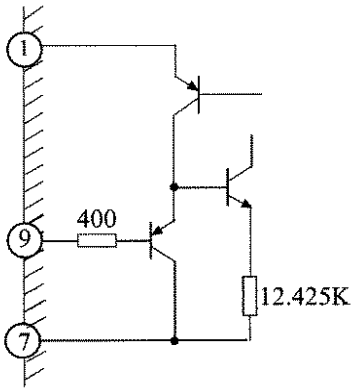
FP-12S Package Power Dissipation

PD- Ta

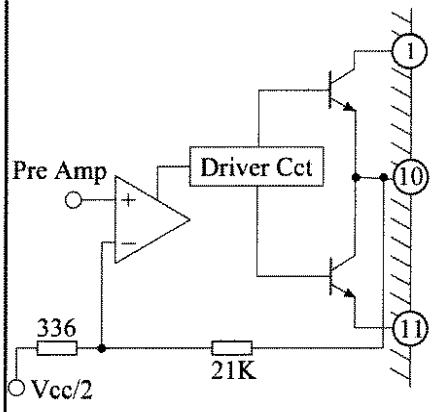
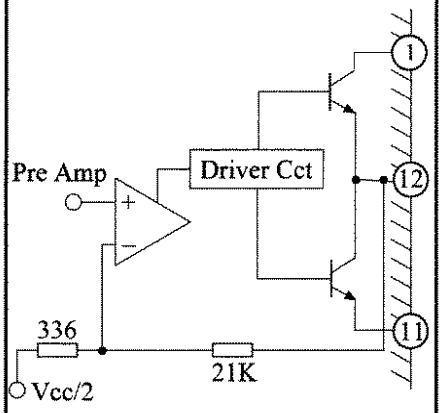


	Functions	Adjacent Circuitry	Descriptions	DC Bias (V)
1	VCC		This is the power supply pin.	Typ 8V
2	Channel 1 Output(+)		This is the positive output terminal of channel 1.	Vcc/2
3	GND		Channel 1 Ground	0V
4	Channel 1 Output(-)		This is the negative output terminal of channel 1.	Vcc/2
5	Standby		Standby Control Pin Standby "ON" = 0V Standby "OFF" = 5V	Typ 5V

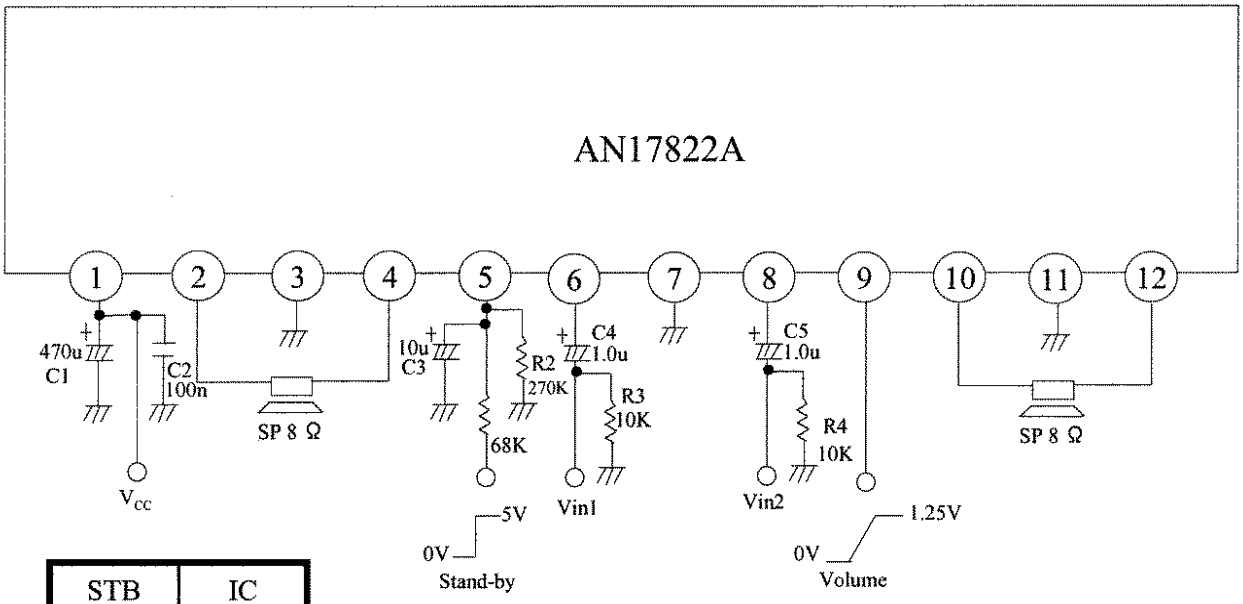
Eff. Date	Eff. Date	Eff. Date	Eff. Date	
24-DEC-2003				

Pin No.	Functions	Adjacent Circuitry	Descriptions	DC Bias (V)
6	Channel 1 Input		This is the channel 1 input terminal.	1.45V
7	GND		Input Ground	0V
8	Channel 2 Input		This is the channel 2 input terminal.	1.45V
9	Volume		Volume Control Pin Volume "OFF" = 0V Max Volume = 1.25V	

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
24-DEC-2003				

Pin No.	Functions	Adjacent Circuitry	Descriptions	DC Bias (V)
10	Channel 2 Output(-)		This is the negative output terminal of channel 2.	Vcc/2
11	GND		Channel 2 Ground.	0V
12	Channel 2 Output(+)		This is the positive output terminal of channel 2.	Vcc/2

Application Circuit



STB	IC
0V	OFF
5V	ON

Application Information

Supply Decoupling

To ensure a stable supply and achieve better ripple rejection, decoupling capacitors need to be connected to VCC. (Pin1)

Decoupling capacitors should have small Equivalent Series Resistance (ESR). This is to prevent resistive losses and introduction of undesirable phase shift to internal circuits.

A ceramic capacitor of 100nF in parallel with a non-ceramic (Tantalum or Aluminum Electrolytic) capacitor of 470uF are suggested. This combination has a small ESR over a wide frequency range.

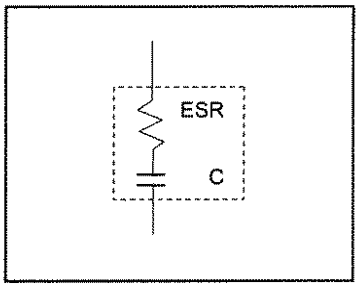


FIG 1. A Practical Capacitor

Although small in size and ESR, large valued ceramic capacitor is not advisable to use. Current surges during power ON/OFF might store energy in the inductances of the power leads; and a large voltage spike could be created when the stored energy is transferred from the inductances to the ceramic capacitor. The amplitude of the spike could exceed twice the supply voltage.

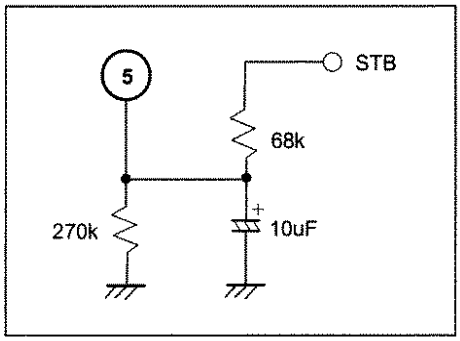


FIG 2. Standby Circuits

If the Standby voltage is provided by a microcontroller, the suppression of "Pop" could even be better.

The microcontroller can set a delay of 100-200ms between the supply and Standby ON/OFF.

The 68k and 270k resistor also form a voltage divider, which determines the Standby threshold.

Standby Operation

Standby pin should be connected with carefully selected components in order to avoid "Pop Noise" during Standby ON/OFF transient.

The 68k resistor and 10uF capacitor pair can delay the rising of voltage at Pin5 to reach the Standby threshold. When Standby is switching on together with supply, this delay would be very useful to ensure no "Pop Noise".

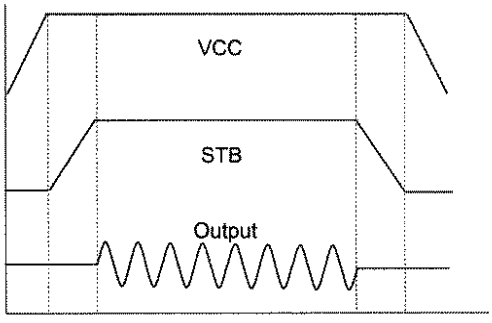


FIG 3. Standby ON/OFF Logic

Power Dissipation and Heat Sink

Before start of the discussion, a few terms have to be defined.

P_D: Power Dissipation
T_J: Junction Temperature
T_C: Case Temperature
T_A: Ambient Temperature
θ_{JC}: Thermal Resistance (Junction to Case)
θ_{CA}: Thermal Resistance (Case to Ambient, normally of heat sink)

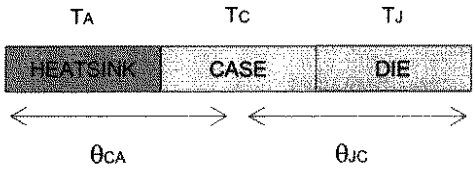


FIG 4. Simplified Illustration of IC and Heat Sink Attached

The following two equations represent the relations of these terms.

$$(T_J - T_C) / \theta_{JC} = P_D \qquad (1)$$
$$(T_C - T_A) / \theta_{CA} = P_D' \qquad (2)$$

For reliable, long-term, continuous operation, junction temperature should not exceed 125°C and θ_{JC} for FP-12S package is 2°C/W. Put these values in Equation 1. After specify the P_D, T_C can be determined.

Assume no heat loss at the casing, i.e. all power is dissipated to the ambient through heat sink, which is quite true. So $P_D = P_D'$. Since T_C is also known, one can determine the following using Equation 2:

a) The rating of heat sink for specific maximum operating ambient temperature, or
b) The maximum operating ambient temperature for specific heat sink rating.

A more general equation can be used for rough calculation.

$$(T_J - T_A) / \theta_{JA} = P_D \qquad (3)$$
$$\theta_{JA} = \theta_{CA} + \theta_{JC} \qquad (4)$$

In this case, θ_{JA} is total thermal resistance of the heat sink and IC package. Therefore, for specified power dissipation, either heat sink rating or maximum operating ambient temperature can be decided if the other is known.

Take note that it's essential to know P_D value before hand in order to work out other quantities. P_D calculation is as shown.

$$P_D = V_{CC} \times I_{CC} - P_{O\_TOTAL} \qquad (5)$$

V_{CC}: DC supply voltage
I_{CC}: RMS value of IC current
P_{O_TOTAL}: Total output power

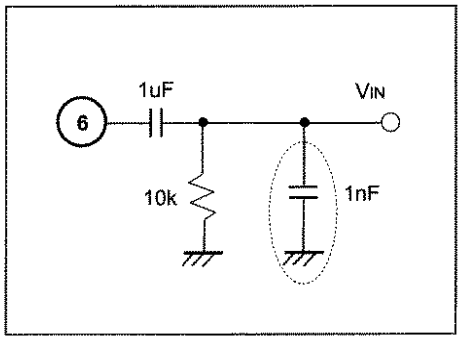


FIG 5. Input DC Decoupling

Input DC Decoupling

Before the input signal reaches differential amplifier stage, its DC component should be removed.

The capacitor of 1uF pass only AC signal and the 10k resistor forms a DC path to ground.

The 1nF capacitor in parallel to the 10k resistor is optional and it serves to filter out high frequency noise at the input.

Output Zobel Network

It should be noted that this device is designed such that the Zobel network (RC pair) at the output pins is not necessary for stable operation.

In practical application, the Zobel network may be applied optionally for two reasons:

a) Ensuring stability for different PCB layout and speaker types.

b) Ability to withstand to high ESD levels.

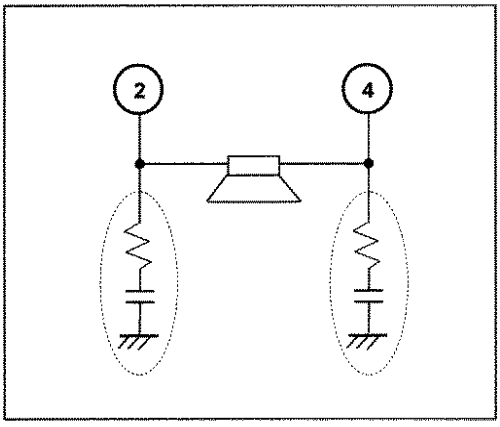


FIG 6. Output Zobel Network

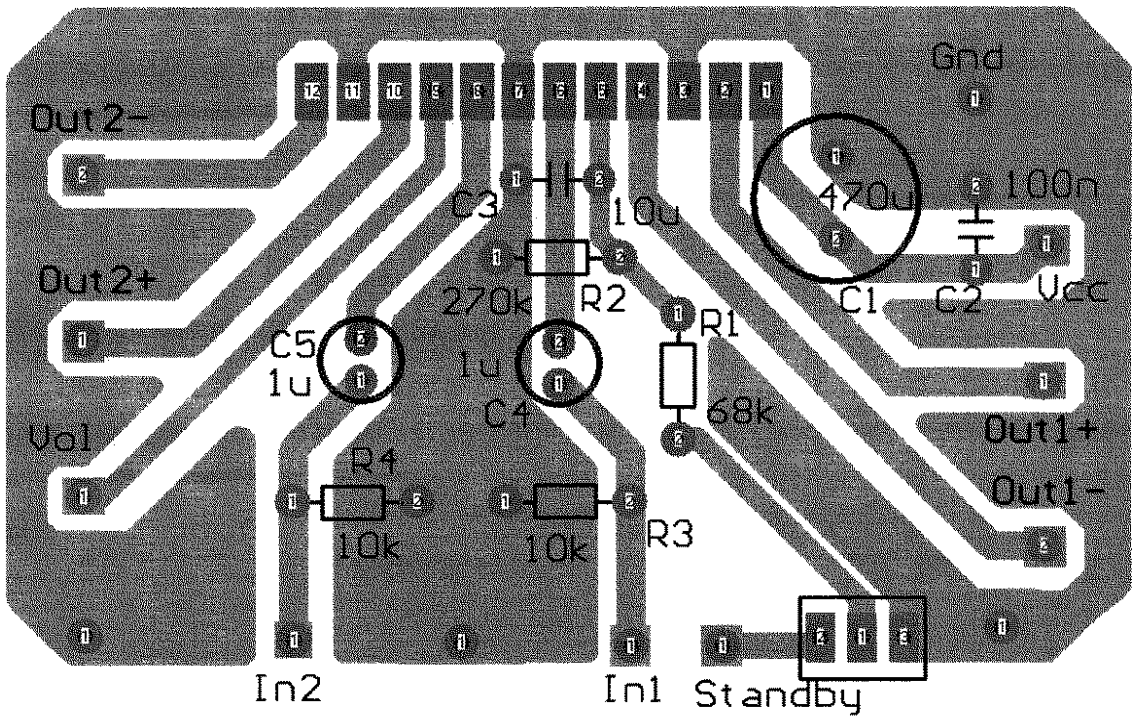
PCB Layout

Good PCB layout can improve chip's performances.

To reduce stray capacitances at the inputs and outputs, external components are to be placed as close to the pins as possible.

PCB traces conducting huge current, such as those connected to supply or outputs, should be kept short and wide. This will keep inductances low and resistive loss to a minimum.

The Layout of test board is as shown below.



(Precautions for use)

1. Make sure that the IC is free of any pin short-circuiting, ground short-circuiting, pin shift and reverse insertion.

2. Ground the radiation fin so that there will be no difference in electric potential between the radiation fin and ground.

3. The thermal protection circuit operates at a Tj of approximately 150°C. The thermal protection circuit is reset automatically when the temperature drops.

4. Make sure that the heat radiation design is effective enough if the Vcc is comparatively high or the IC operates high output power.

5. Connect only ground pin for signal sources to the signal GND pin of the amplifier on the previous stage.