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SANYO Semiconductors
DATA SHEET

LA4809M — Monolithic Linear IC Stereo Headphone Amplifier

Overview

LA4809M is a 2-channels power amplifier to drive the headphone with wide supply voltage range.
To minimize the effects of power supply, the regulator circuit for control of the output power is built-in to enable setting of the output power value adequate for the headphone amplifier (2 types of set value available). This product also has the standby function, and is suitable as a driver for wide-ranging headphone.

Applications

Headphone driver for TV and audio equipment

Features

- 2-channels power amplifier built-in (maximum output power value changeable according to the setting)
  - Maximum output power A = 55mW Standard (Pin 10 : Open)
  - Maximum output power B = 160mW Standard (Pin 10 : GND)
    - *V_{CC} = 12V, R_L = 16Ω, THD = 10%
    - *Change to another power value possible by adding the external parts
- Regulator built-in : Limited change of the output power value due to fluctuation of supply voltage
  High-Ripple rejection ratio
- Standby function (also used for voice muting) : Current drain at standby = 0.01μA Standard (V_{CC} = 12V)
- Overheat protection circuit built-in
- Wide supply voltage range (differing according to the set value of maximum output power) : V_{CC} = 3.6V to 17V

SANYO Semiconductor Co., Ltd.
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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max	Without signal	18	V
Allowable power dissipation	Pd max	* Mounted on a printed circuit board.	1.75	W
Maximum junction temperature	Tj max		150	°C
Operating temperature	Topr		-30 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

* Evaluation board of SANYO Semiconductor : 50mm × 50mm × 0.8mm (Glass epoxy double-side PCB)

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		12	V
Recommended load resistance	R_L		16 to 32	Ω
Operating supply voltage range	V_{CC} op-1	mode-B (for P_O max = 160mW)	6.2 to 17	V
	V_{CC} op-2	mode-A (for P_O max = 55mW)	4.2 to 17	V
	V_{CC} op-3	* Depending on the output power value when the external part is added	3.6 to 17	V

* Determine the supply voltage with due consideration of the allowable power dissipation.
* Note that the supply voltage range is limited depending on the setting of the maximum output power value.

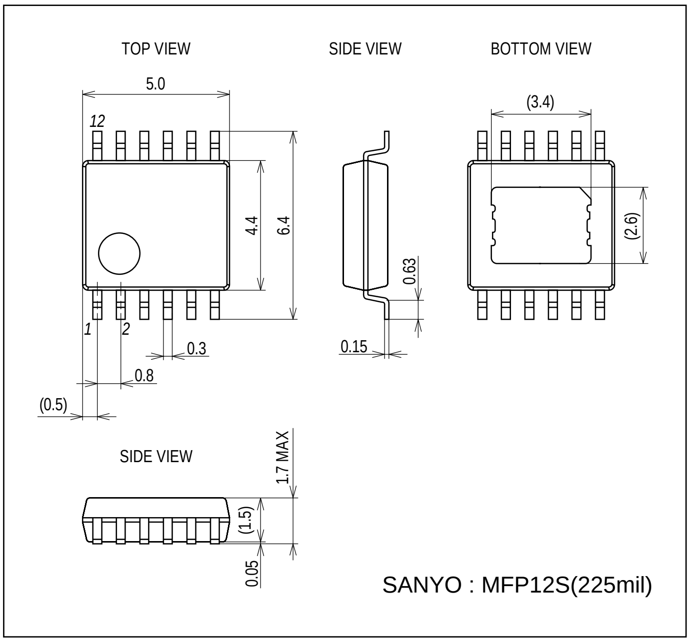
Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, R_L = 16Ω, fin = 1kHz, V3 = 2V, Pin 10 : open

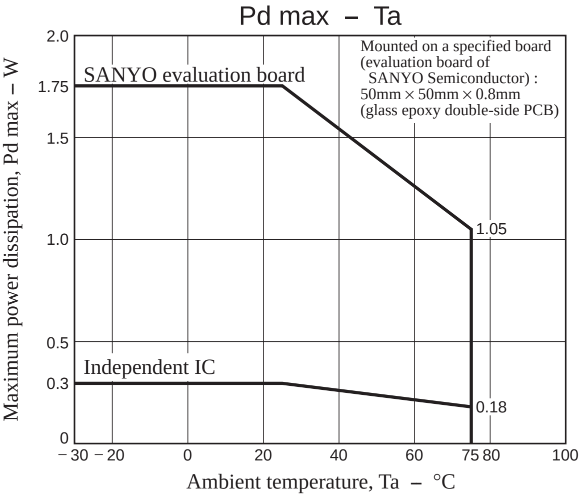
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current drain	$I_{CCO}P$	No signal		3.8	6.5	mA
Standby current drain	I_{STBY}	No signal, Standby mode (V3 = 0.3V)		0.01	5	μA
Maximum output power-A	P_OMAXA	THD = 10%, mode-A	30	55		mW
Maximum output power-B	P_OMAXB	THD = 10%, mode-B (Pin 10 : gnd)	87	160		mW
Voltage gain	VG	Vin = -20dBV	10.2	11.7	13.2	dB
Channel balance	CHB	Vin = -20dBV	-1.5	0	+1.5	dB
Total harmonic distortion	THD	Vin = -20dBV		0.15	0.7	%
Output noise voltage	V_NOUT	Rg = 620Ω, 20 to 20kHz		18	50	μVrms
Channel separation	CHsep	Vin = -15dBV	60	72		dB
Mute attenuation level	VMT	Vin = -10dBV, Standby mode (V3 = 0.3V)	-80	-88		dBV
Ripple rejection ratio	SVRR	Rg = 620Ω, fr = 100Hz, Vr = -10dBV	70	81		dB
Pin 2 voltage-A	V2A	mode-A		2.1		V
Pin 2 voltage-B	V2B	mode-B (Pin 10 : gnd)		3.1		V
STBY control HIGH voltage	VSBH	(Circuit power mode)	2		9	V
STBY control LOW voltage	VSBL	(Circuit standby mode)	0		0.6	V

* mode-A (Pin 10 = open) : P_O max = 55mW
  Pin 2 voltage : V2 = 2.1V, Internal regulator voltage : Vreg = 2 × V2 = 4.2V, Amp operating reference voltage : Vref = 1 × V2 = 2.1V
  mode-B (Pin 10 = gnd) : P_O max = 160mW
  Pin 2 voltage : V2 = 3.1V, Internal regulator voltage : Vreg = 2 × V2 = 6.2V, Amp operating reference voltage : Vref = 1 × V2 = 3.1V

Package Dimensions

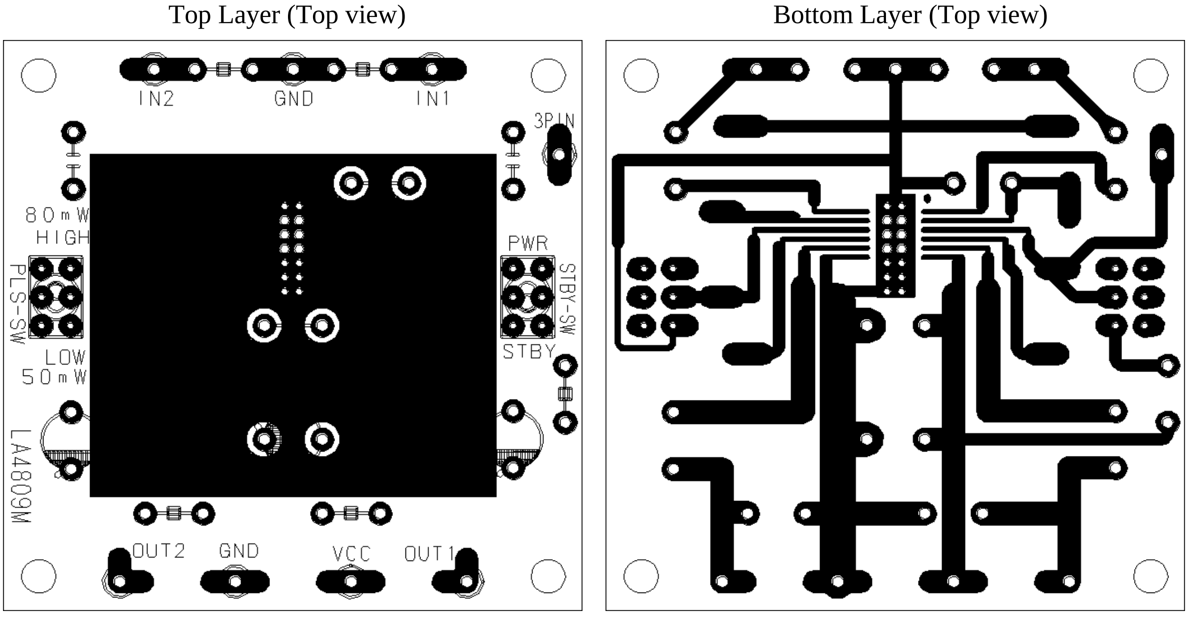
unit : mm (typ)
3384



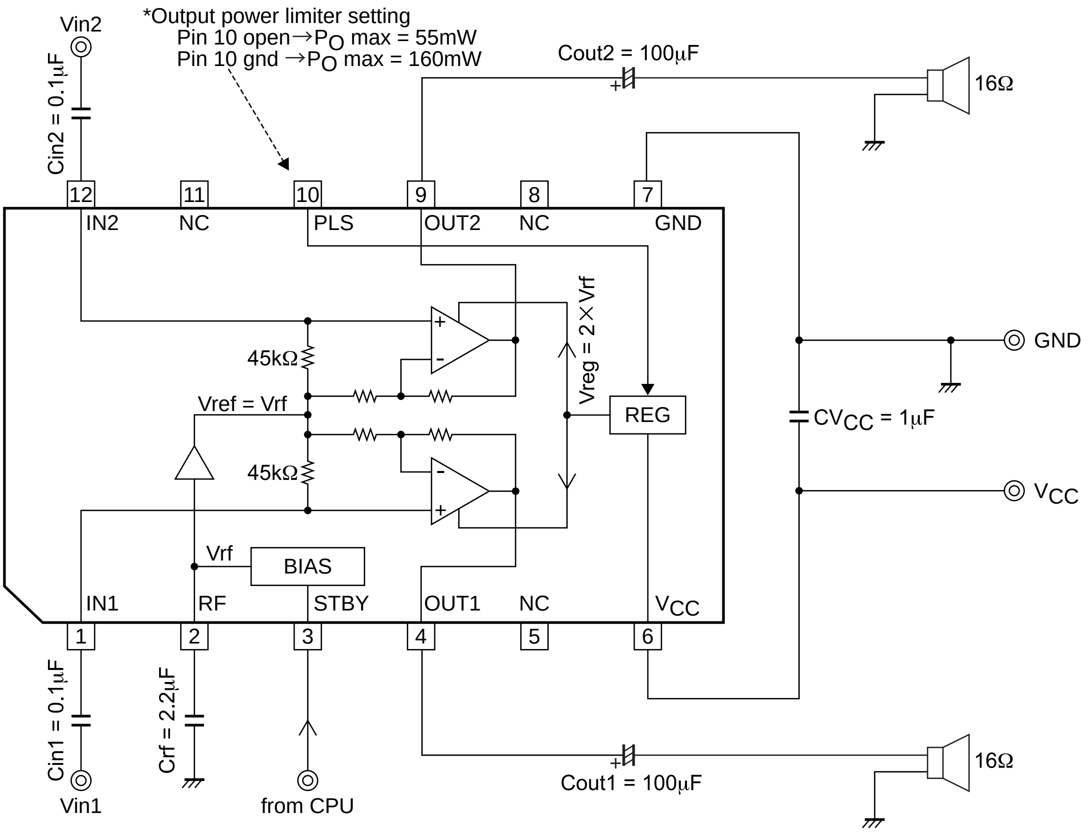


Evaluation board

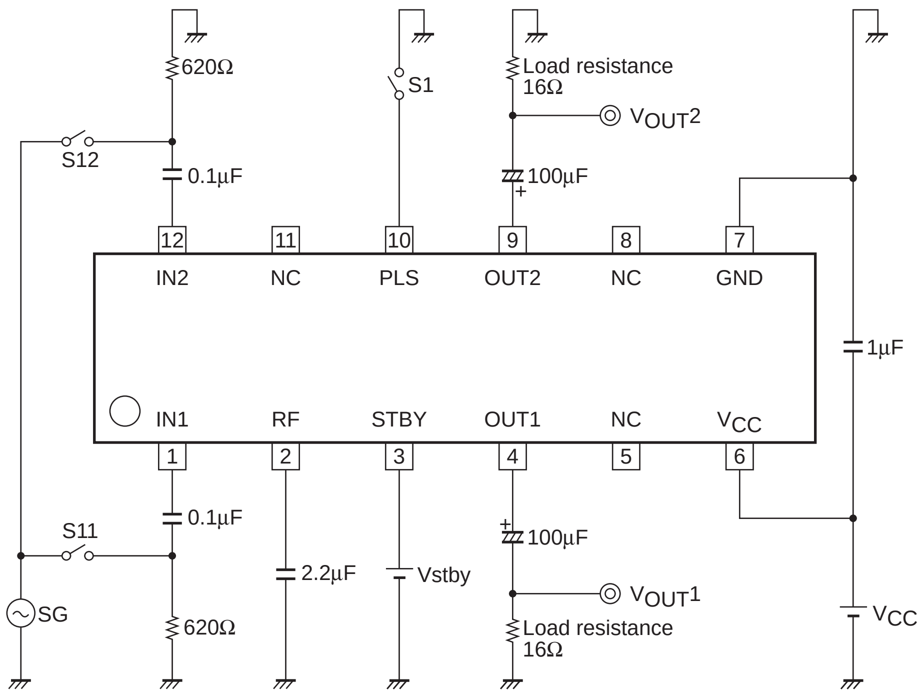
Copper foil pattern diagram
(Dimensions : 50mm × 50mm × 0.8mm)



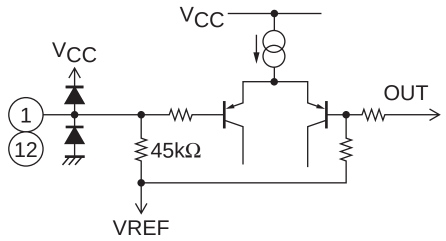
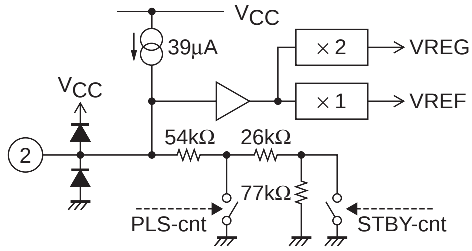
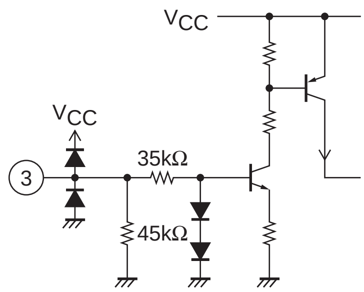
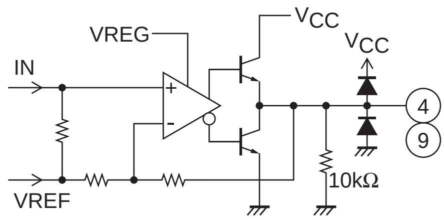
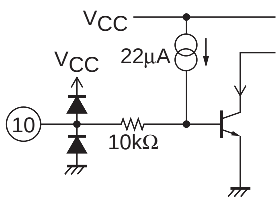
Block Diagram and Sample Application Circuit



Test Circuit Diagram



Pin Functions

Pin No.	Pin Name	Pin Voltage (V)		Description	Equivalent Circuit
		mode-A	mode-B		
1 12	IN1 IN2	2.1	3.1	Amplifier input pin.	
2	RF	2.1	3.1	Reference voltage pin.	
3	STBY	Applied	Applied	Standby control pin. (to which the external voltage is applied)	
4 9	OUT1 OUT2	2.1	3.1	Amplifier output pin.	
5 8 11	NC			NC pin.	
6	V_{CC}	Applied	Applied	Power pin. (to which the external voltage is applied)	
7	GND	GND	GND	GND pin.	
10	PLS	0.69	GND	Output power selection pin.	

Cautions for use

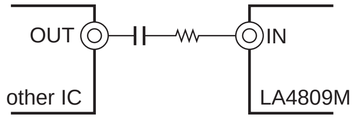
1. Input coupling capacitors (Cin1, Cin2)
   Cin1 (Cin2) is an input coupling capacitor, which is intended for DC cut. This capacitor forms a high pass filter together with the internal resistance of 45kΩ attenuating the bass frequency signal. Set the capacitance value with due consideration of the cut-off frequency.
   Note that the cut-off frequency is expressed as follows :
   1ch ⇒ $fc1 = 1/ (2\pi \times Cin1 \times 45000)$
   2ch ⇒ $fc2 = 1/ (2\pi \times Cin2 \times 45000)$
   This capacitor also affects the pop noise at a time of falling. Note that setting the higher capacitance value causes delay of the capacitor discharge rate, causing louder pop noise.

2. Output coupling capacitors (Cout1, Cout2)
   Cout1 (Cout2) is an output coupling capacitor, which is intended for DC cut. This capacitor forms a high pass filter together with the load impedance of R_L, attenuating the bass frequency signal. Set the capacitance value with due consideration of the cut-off frequency. Normally, the chemical capacitor is used. When setting the capacitance value, take into account the characteristics of the chemical capacitor, namely, the capacitance value of chemical capacitor tends to decrease at low temperature.
   Note that the cut-off frequency is expressed as follows :
   1ch ⇒ $fc3 = 1/ (2\pi \times Cout1 \times R_L)$
   2ch ⇒ $fc4 = 1/ (2\pi \times Cout2 \times R_L)$
   This capacitor also affects the pop noise at a time of rising. Note that setting the higher capacitance value causes louder pop noise.

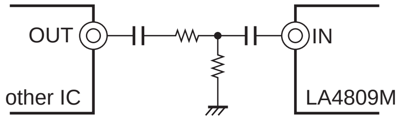
3. Power supply line capacitor (CV_{CC})
   CV_{CC} is intended to stabilize the power supply line. Arrange this capacitor as near to IC as possible and always use the ceramic capacitor with superior high frequency characteristics.
   Increase the capacitance value when the power supply line is relatively unstable.

4. Pin 2 capacitor (Crf)
   Crf is a capacitor to determine the transient response characteristics of the Pin 2 voltage (reference voltage) : Vrf. At a time of rising, this is charged by the internal constant-current source (about 39μA). At a time of falling, this is discharged by the internal resistance (about 157kΩ). Due attention must be paid because pop noise and the amplifier rise / fall time change depending on the transient response characteristics of Pin 2 voltage. Decreasing the capacitance value to shorten the response time, pop noise becomes louder. Therefore, the use of the value shown below as the capacitance value is recommended. As this capacitor reduces the power supply ripple component, decrease in the capacitance value results in lowering of the ripple removal ratio.
   Crf recommended values : 1μF to 3.3μF

5. Voltage gain
   The voltage gain of amplifier is determined by the internal resistance and is fixed at about 11.7dB. When the output level is to be changed, attempt attenuation with the resistor in the forward stage of input as shown in Fig.1. To enhance the degree of attenuation, use two resistors as shown in Fig.2 so as to reduce internal-resistor variation factors. Though attenuation in the backward stage of output as shown in Fig.3 is possible, this may cause decrease in the maximum output power.



(Low attenuation degree)
Fig.1



(High attenuation degree)
Fig.2

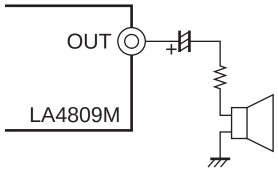


Fig.3

6. Load capacitance
   When connecting a capacitor between the output pin and GND for an anti-electric wave radiation measure, this capacitor may cause decrease in the phase margin of power amplifier, resulting in the oscillation phenomenon. When connecting this capacitor, pay attention to its capacitance value.
   Recommended capacitance value : 560pF or less, or 0.01μF to 0.1μF

7. Selection of the maximum output power value (handling of Pin 10)

This IC enables selection of two types of maximum output power value according to the handling method of Pin 10. The regulator circuit for output power control is built in, in which, by changing the voltage of Pin 2, the regulator voltage : Vreg is changed to enable selection of the maximum output power value.

Mode-A (P_O max = 55mW) : Pin 10 set to the OPEN state
Pin 2 voltage : V2 = 2.1V,
Internal regulator voltage : Vreg = 4.2V,
Amplifier operating reference voltage : Vref = 2.1V

Mode-B (P_O max = 160mW) : Pin 10 connected to the GND line
Pin 2 voltage : V2 = 3.1V,
Internal regulator voltage : Vreg = 6.2V,
Amplifier operation reference voltage : Vref = 3.1V

When the maximum output power value is to be changed under CPU control, use the NPN transistor as shown in Fig.4, so that the Pin 10 voltage approaches the GND potential (0.1V or below) sufficiently.

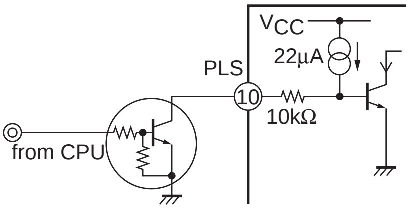


Fig.4

8. Change of the maximum output power value (by handling Pin 2)

Pin 2 voltage : V2 is determined from the constant-current source and internal resistance as shown in Fig.5.

Operating ⇒ Mode-A : 54kΩ used
Mode-B : 80kΩ (54kΩ + 26kΩ) used

Not operating (at a time of falling) ⇒ 157kΩ (54kΩ + 26kΩ + 77kΩ) used

The internal regulator voltage and amplifier operating reference voltage are generated from this Pin 2 voltage.

Regulator voltage : Vreg = V2 × 2
Amplifier operating reference voltage : Vref = V2 × 1

Accordingly, to change the maximum output power value, connect the resistance : Rrf between Pin 2 and GND as shown in Fig.5. This will cause change in the Pin 2 voltage. Note that, in view of circuit operation, the Pin 2 voltage must be set to 1.6V or above.

If the discharge constant is not to be changed, Use the NPN transistor to control the Rrf connection as shown in Fig.6.

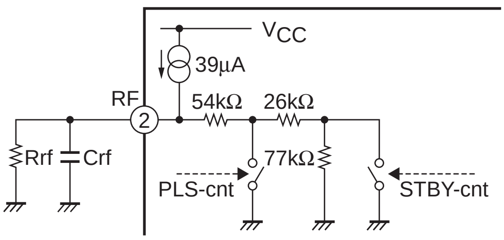


Fig.5

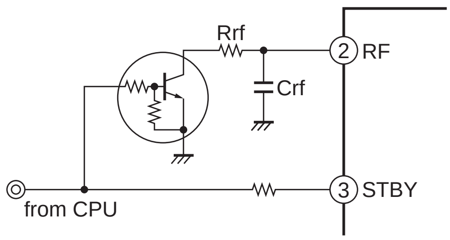


Fig.6

9. Standby pin (Pin 3)

By controlling the standby pin, the mode can be changed over between standby and operation. Though this control is possible directly by the CPU output port, the control may be exposed to adverse affect of digital noise from CPU. It is recommended therefore to insert series resistance (1kΩ or more).

Standby mode ⇒ V3 = 0V to 0.6V
Operation mode ⇒ V3 = 2V to 9V (for V_{CC} = 9V or above), V3 = 2V to V_{CC} (for V_{CC} = less than 9V)

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When the standby function is not to be used, Pin 3 may be interlocked with power supply as shown in Fig.7. However, due care must be taken in this case because such interlock makes the effectiveness of the pop noise reduction circuit null, resulting in extremely large pop noise at a time of rising and falling. There are also methods to reduce the pop noise by using two capacitors as shown in Fig.8. If pop noise is to be suppressed sufficiently, CPU control of the standby pin is recommended.

Note that the approximate inrush current; I3 into the standby pin is calculated as follows :

Pin 3 inrush current (unit : A) : $I3 = (5 \times V_{CC} - 4) \times 10^{-5} / Rst$

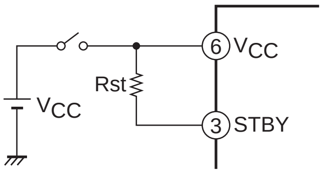


Fig.7

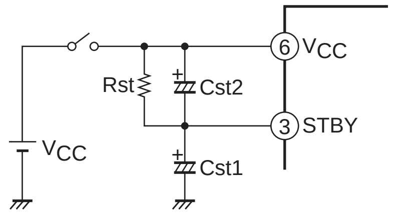


Fig.8

10. Operating power supply voltage range

The applicable power supply voltage range varies depending on the setting conditions of the maximum output power value. Use this range while taking into account the Pin 2 voltage. As a guideline, the supply voltage at the lowest point to be used must be two times the Pin 2 voltage.

Note that the minimum operating supply voltage must be 3.6V.

mode-B ⇒ V_{CC} op = 6.2V to 17V

mode-A ⇒ V_{CC} op = 4.2V to 17V

At change of the output power value due to external resistance ⇒ V_{CC} op = 2 × V2 to 17V (V2 ⇒ Pin 2 voltage)

11. Handling of NC pins (Pins 5, 8, and 11)

NC pins are not connected to anything internally and may be left in the OPEN state. To enhance the heat sink effect as much as possible, connection of NC pins to the GND line is recommended.

In particular, Pin 5 should be connected to the GND line so as to protect Pin 4 (the first output).

If the pins 4 and 5 section and the pins 5 and 6 section are bridged with solder simultaneously, the output pin enters the powering (short to power) state, allowing the large current to flow into the output pin, resulting in deterioration or damage of internal elements. Risk of deterioration or damage may be reduced when Pin 5 is connected to GND. When the output pin voltage is about 0.7V or less, drive and power stages of the power amplifier circuit used becomes inoperable. In this context, the protection in case of ground fault is provided.

12. Heat protective circuit

The heat protective circuit is incorporated in IC and can reduce the risk of damage/deterioration in case of abnormal heat generation due to certain reasons. This protective circuit is activated when the junction temperature : Ti of the chip in IC increases to about 160°C, shutting OFF current supply to the power amplifier. The signal is not output anymore. When the chip temperature lowers (to about 130°C), the circuit is automatically reset.

Note that this circuit is not always capable of preventing damage/deterioration and should be handled with utmost care. In case of abnormal heating, turn OFF power supply immediately and identify the probable causes.

13. Short-circuit between pins

Power ON while leaving the pins in the short-circuit state may cause deterioration or damage. When installing IC to the substrate, check if pins are short-circuited with solder before turning power supply ON.

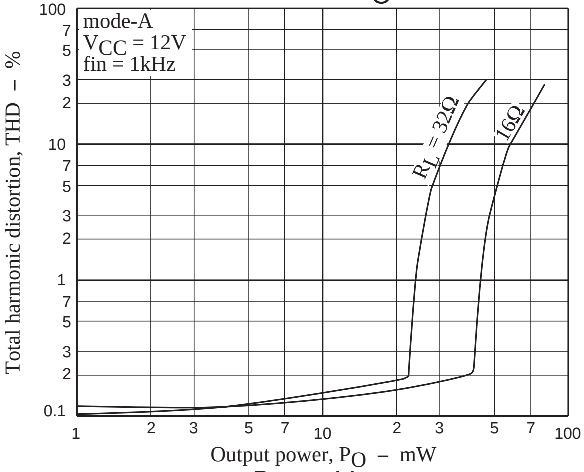
14. Load short-circuit

Leaving the loads in the short-circuit state over a long period of time may cause deterioration or damage. Never short-circuit loads.

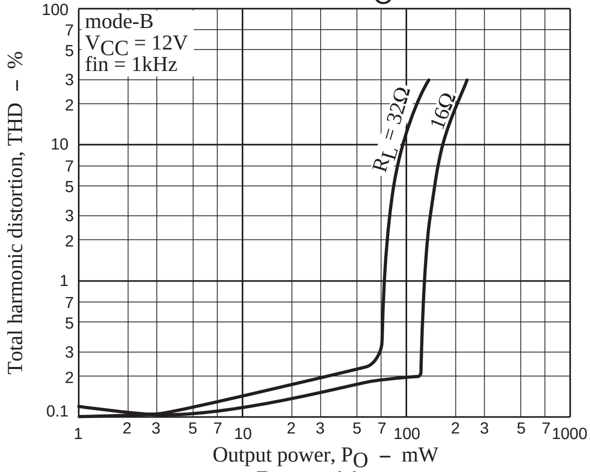
15. Maximum rating

When the product is used near the maximum rating, even the smallest change in the conditions may cause exceeding of the maximum rating, possibly leading to the fracture accident. Take the sufficient fluctuation margin for the supply voltage and always use the product within a range never exceeding the maximum rating. The package used for this IC has the low heat sink effect as a single unit. When the working supply voltage is high, solder the backside heat sink pad to ensure sufficient heat sink performance with copper foil of printed circuit board.

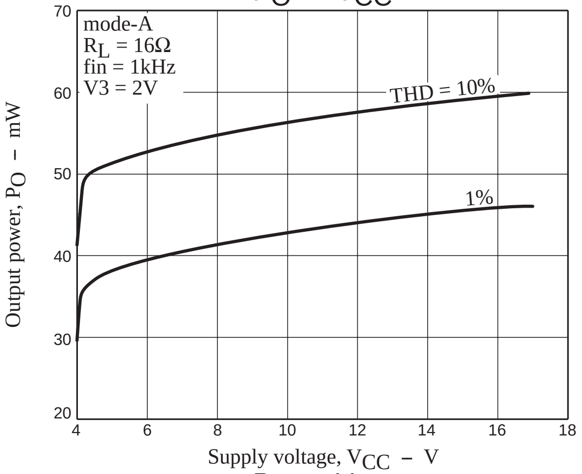
THD – P_O



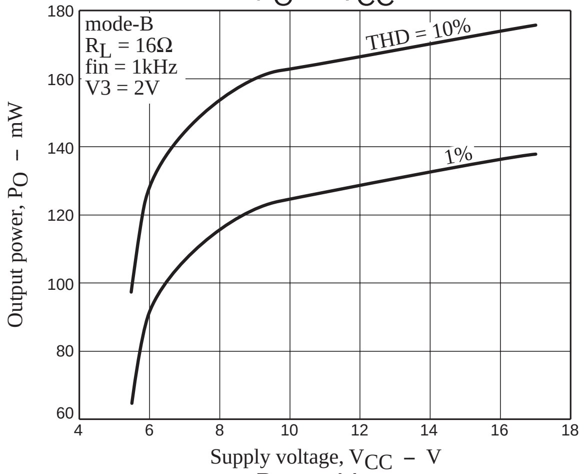
THD – P_O



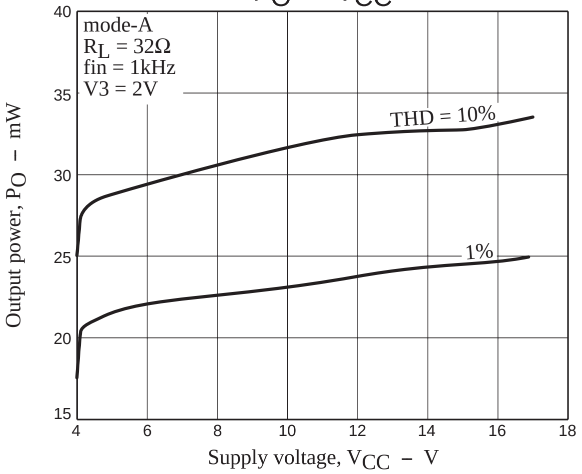
P_O – V_{CC}



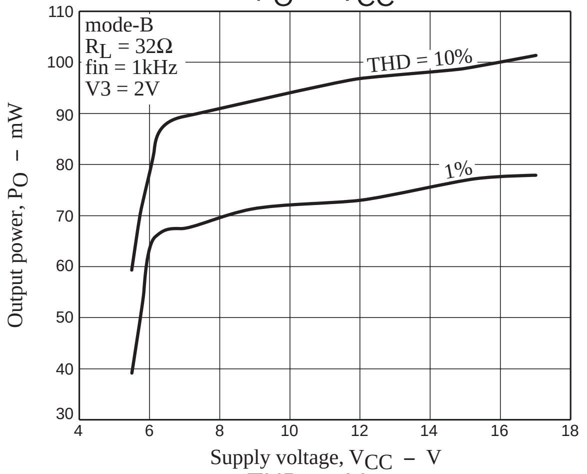
P_O – V_{CC}



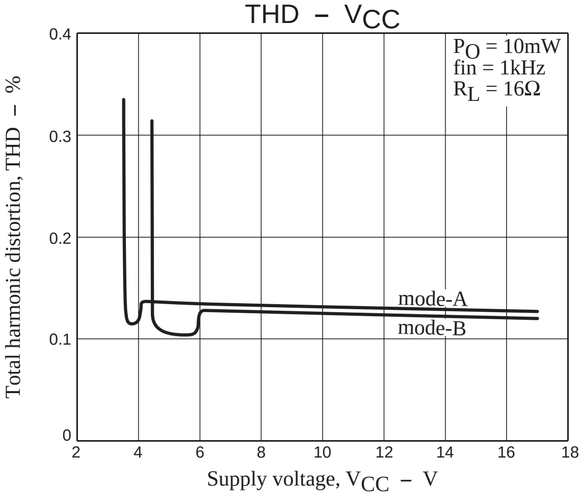
P_O – V_{CC}



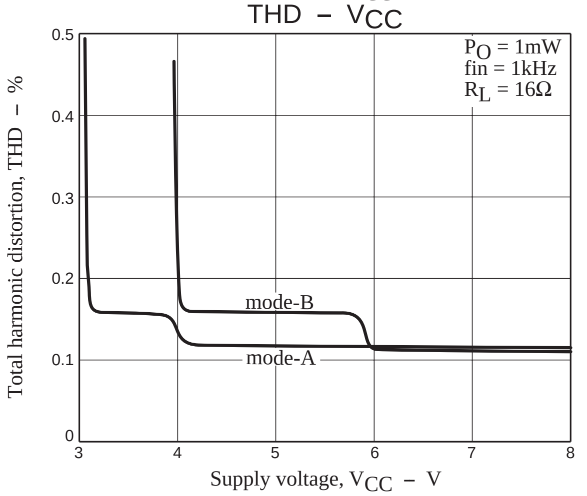
P_O – V_{CC}



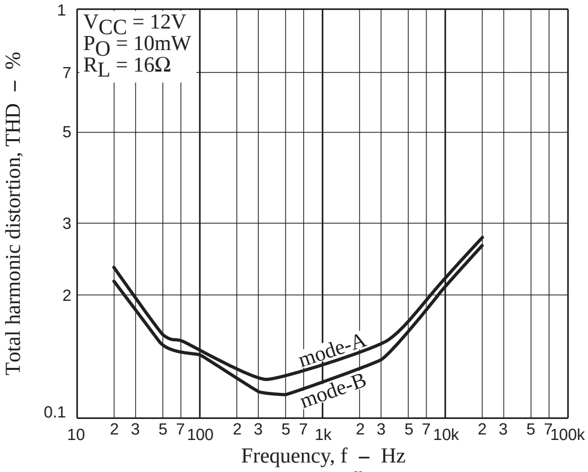
THD – V_{CC}



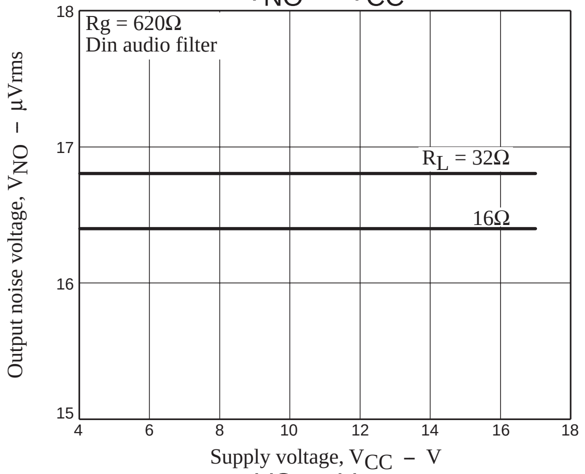
THD – V_{CC}



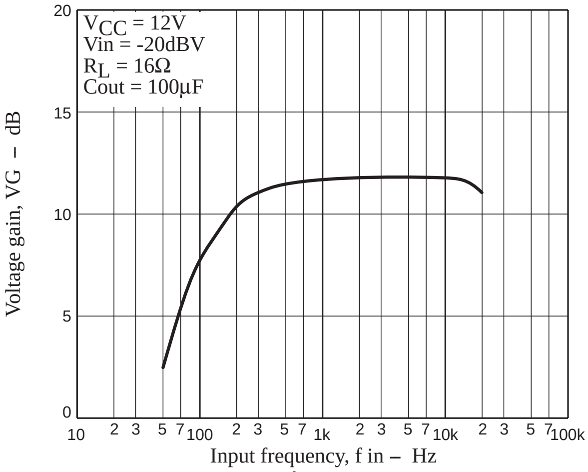
THD – f



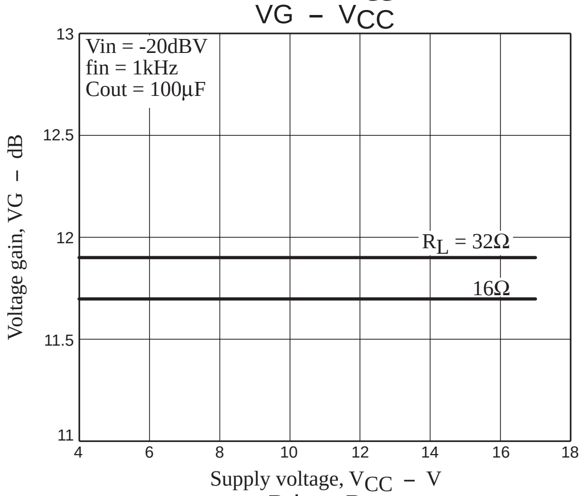
VNO – VCC



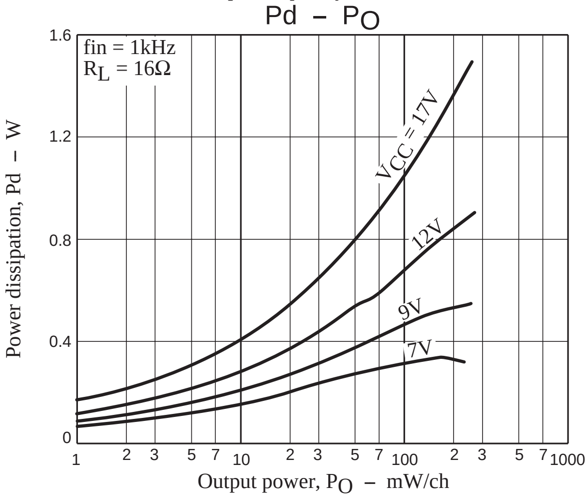
VG – fin



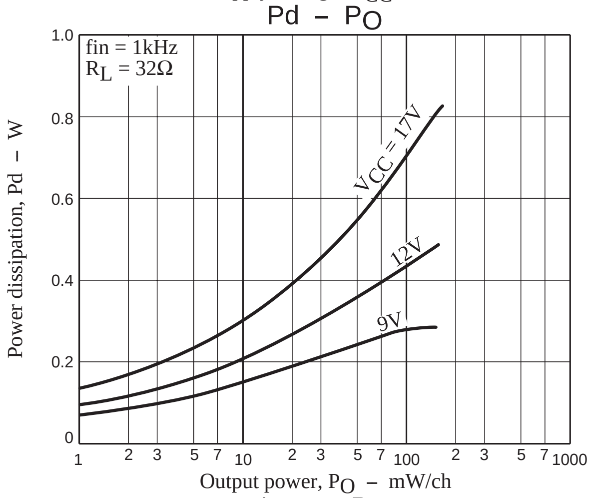
VG – VCC



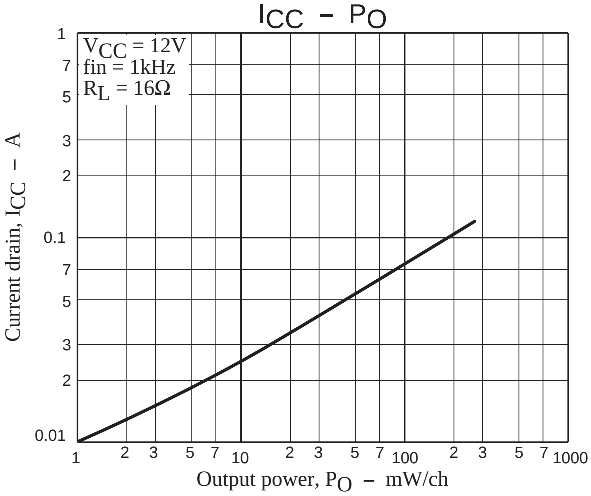
Pd – PO



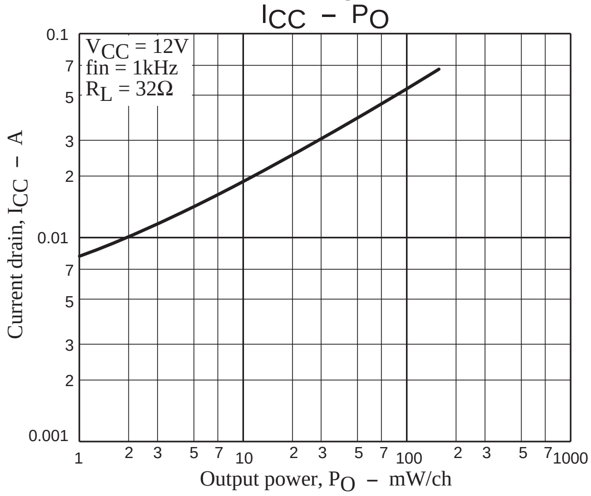
Pd – PO



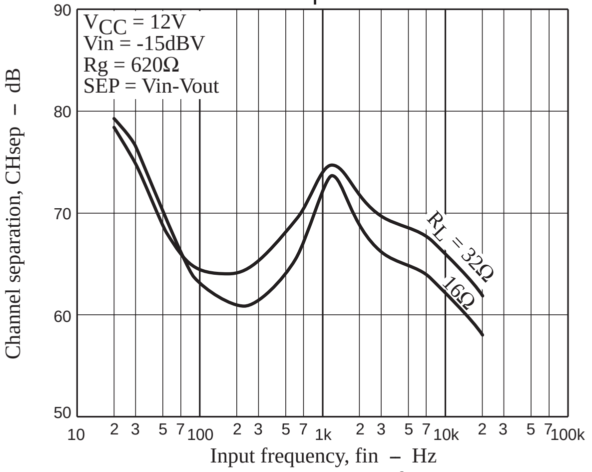
ICC – PO



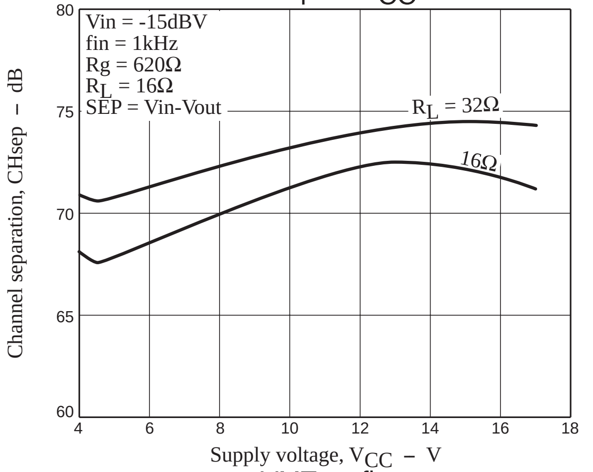
ICC – PO



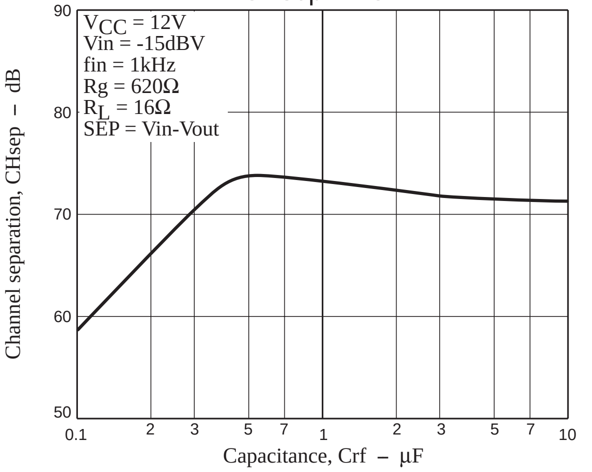
CHsep – fin



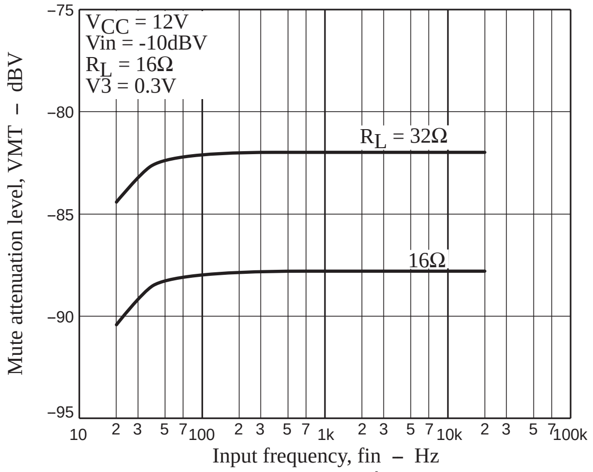
CHsep – VCC



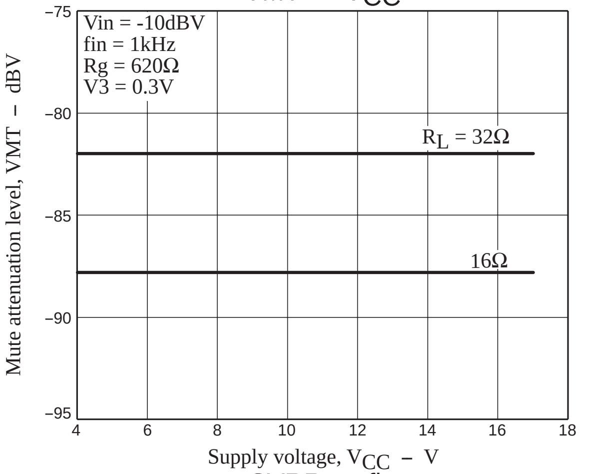
CHsep – Crf



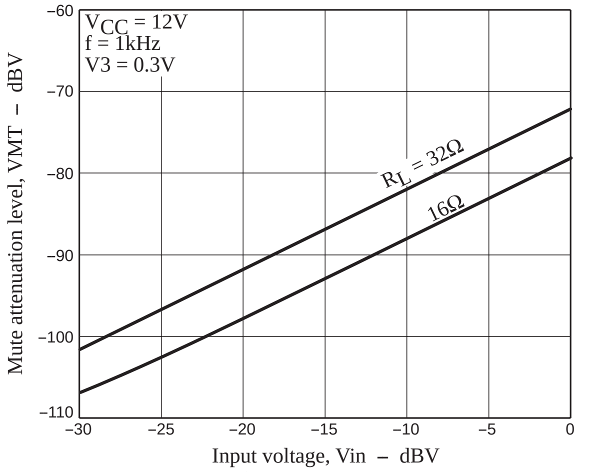
VMT – fin



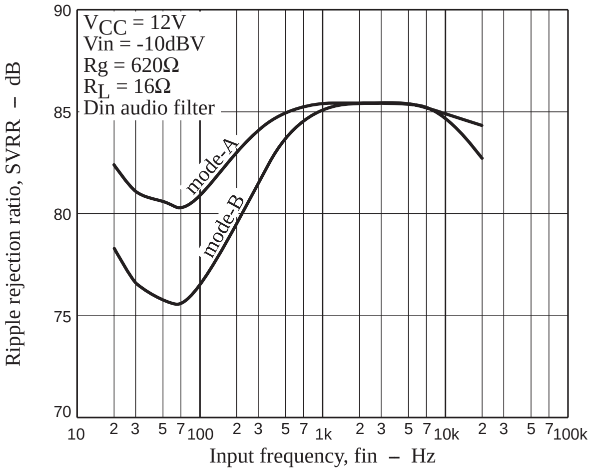
VMT – VCC



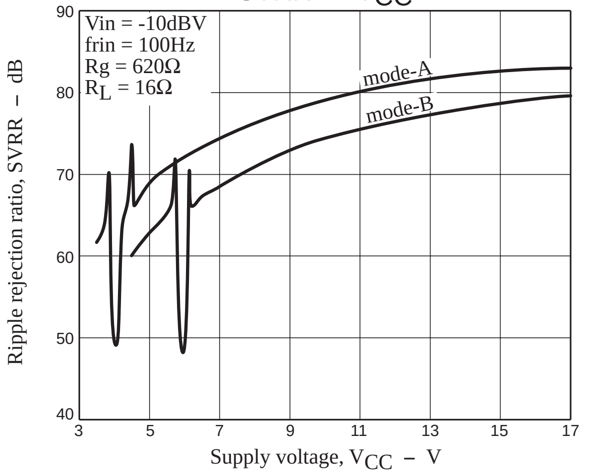
VMT – Vin



SVRR – fin



SVRR – VCC



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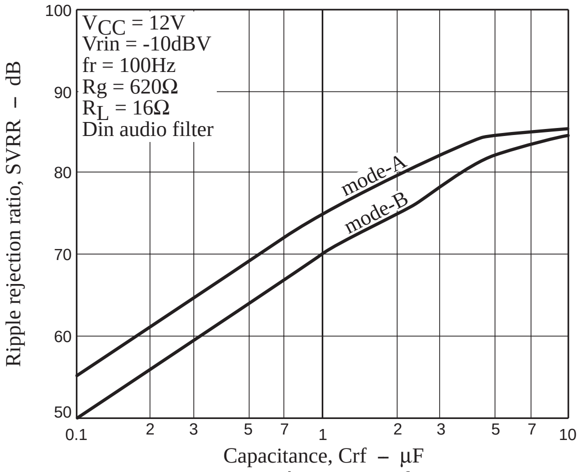
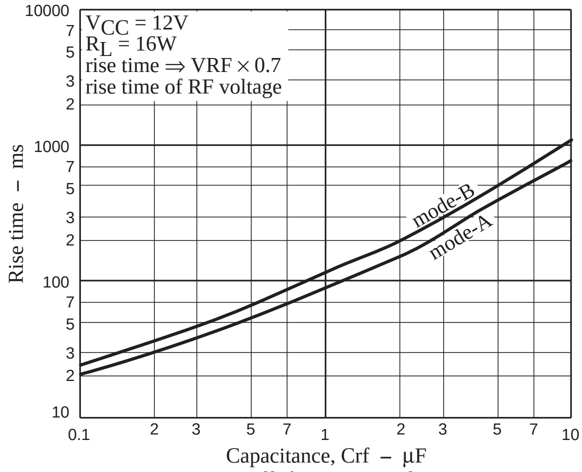
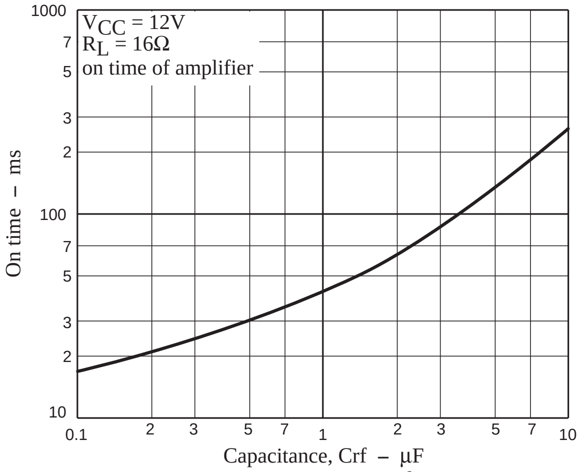


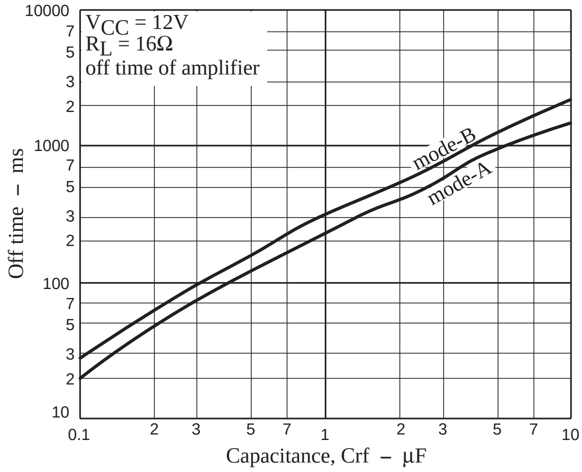
Rise time – Crf



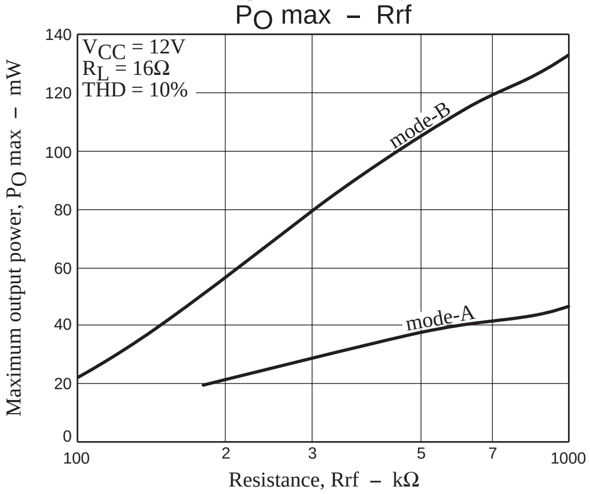
On time – Crf



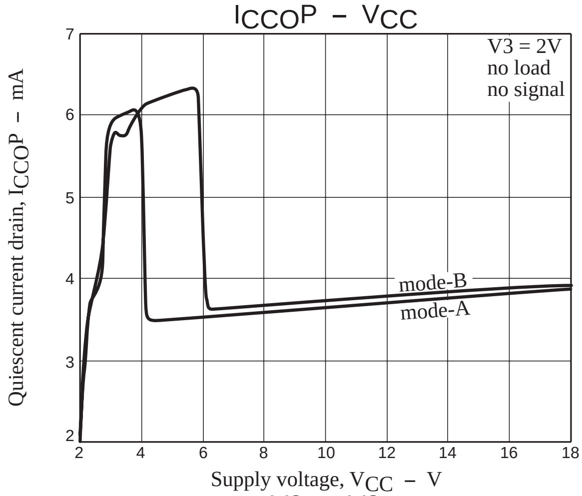
Off time – Crf



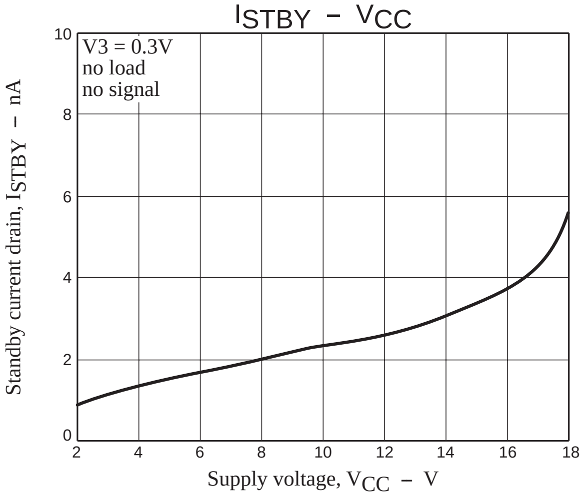
P_O max – Rrf



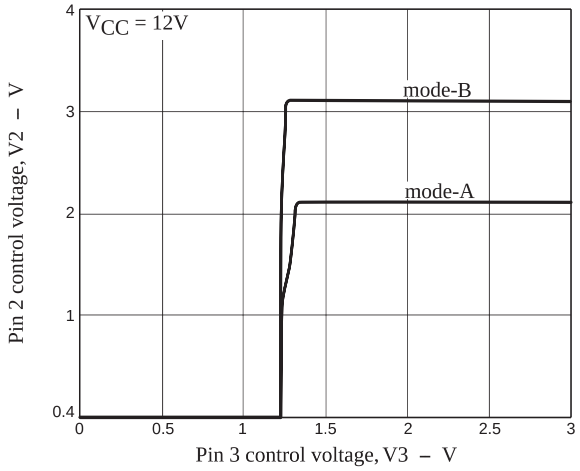
$I_{CCO}P$ – V_{CC}



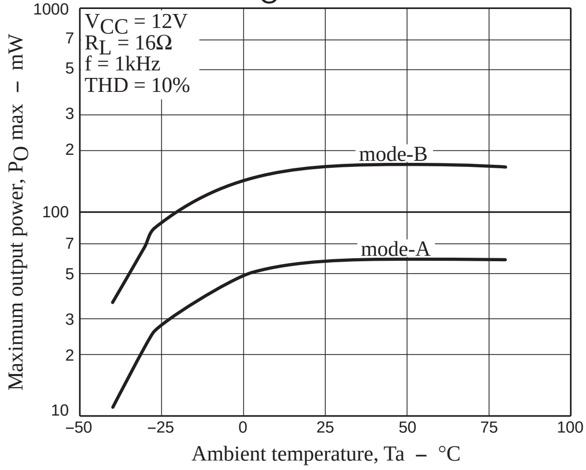
I_{STBY} – V_{CC}



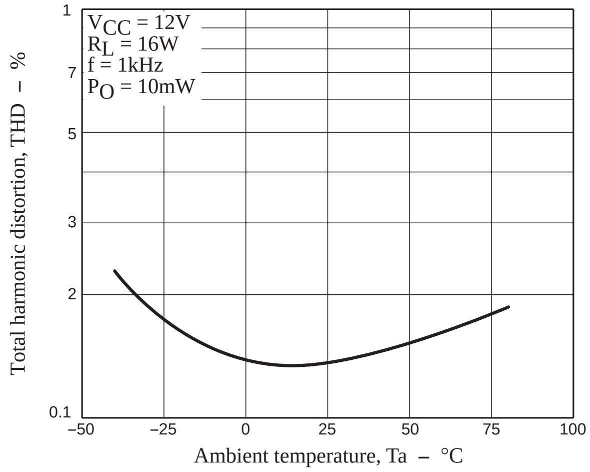
V2 – V3



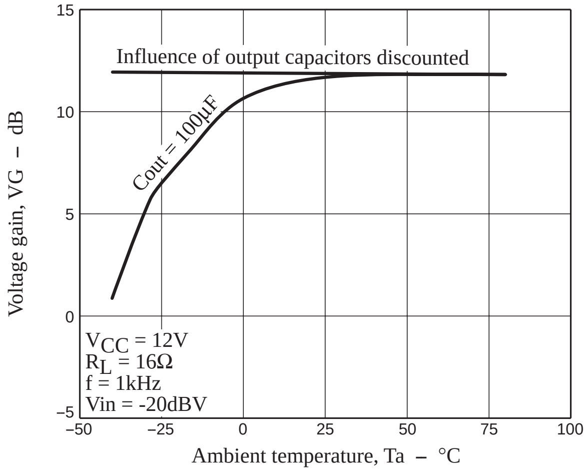
P_O max – Ta



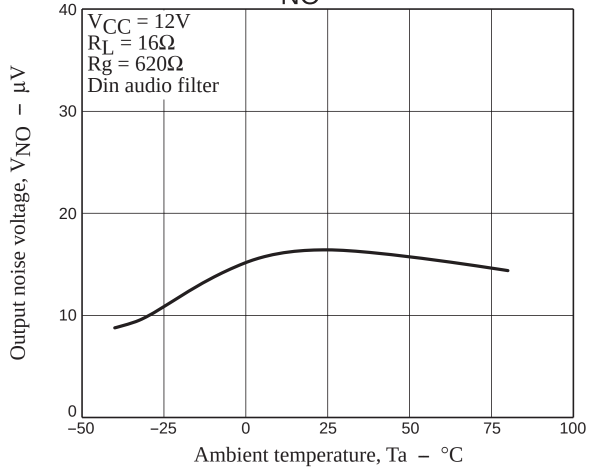
THD – Ta



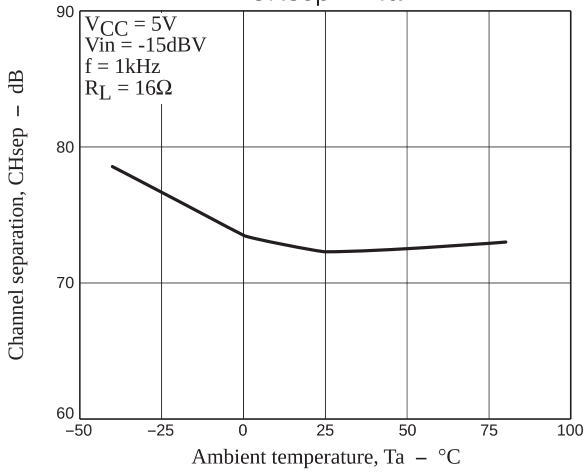
VG – Ta



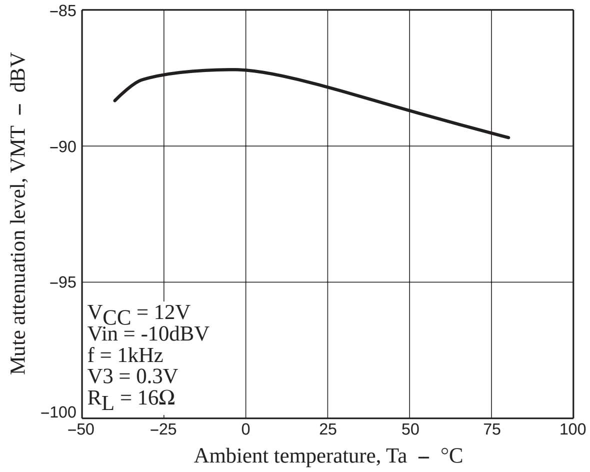
V_{NO} – Ta



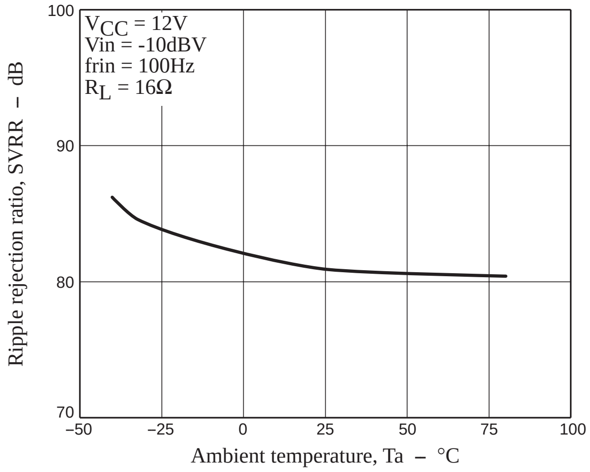
CHsep – Ta



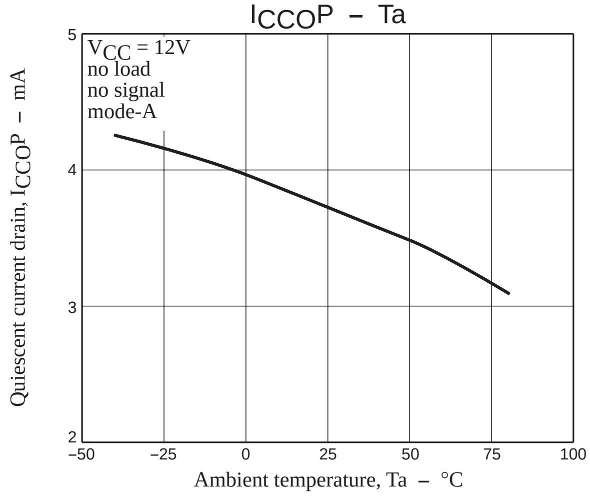
VMT – Ta

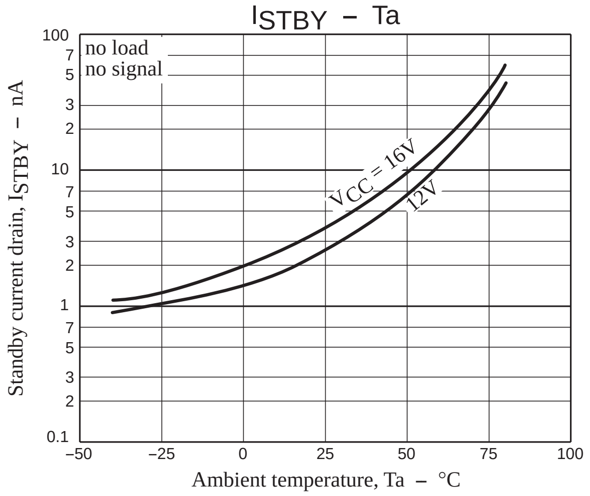


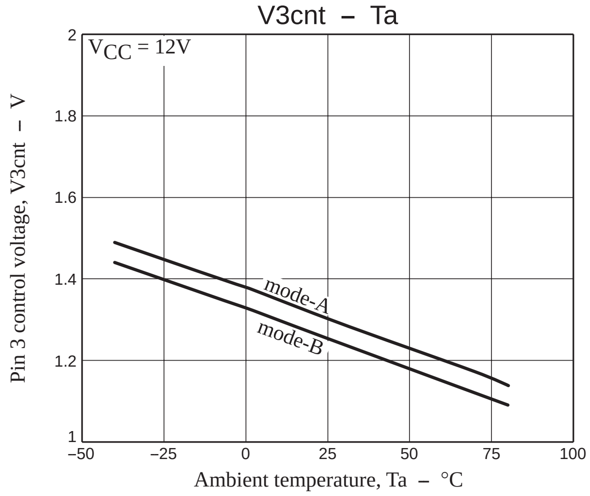
SVRR – Ta



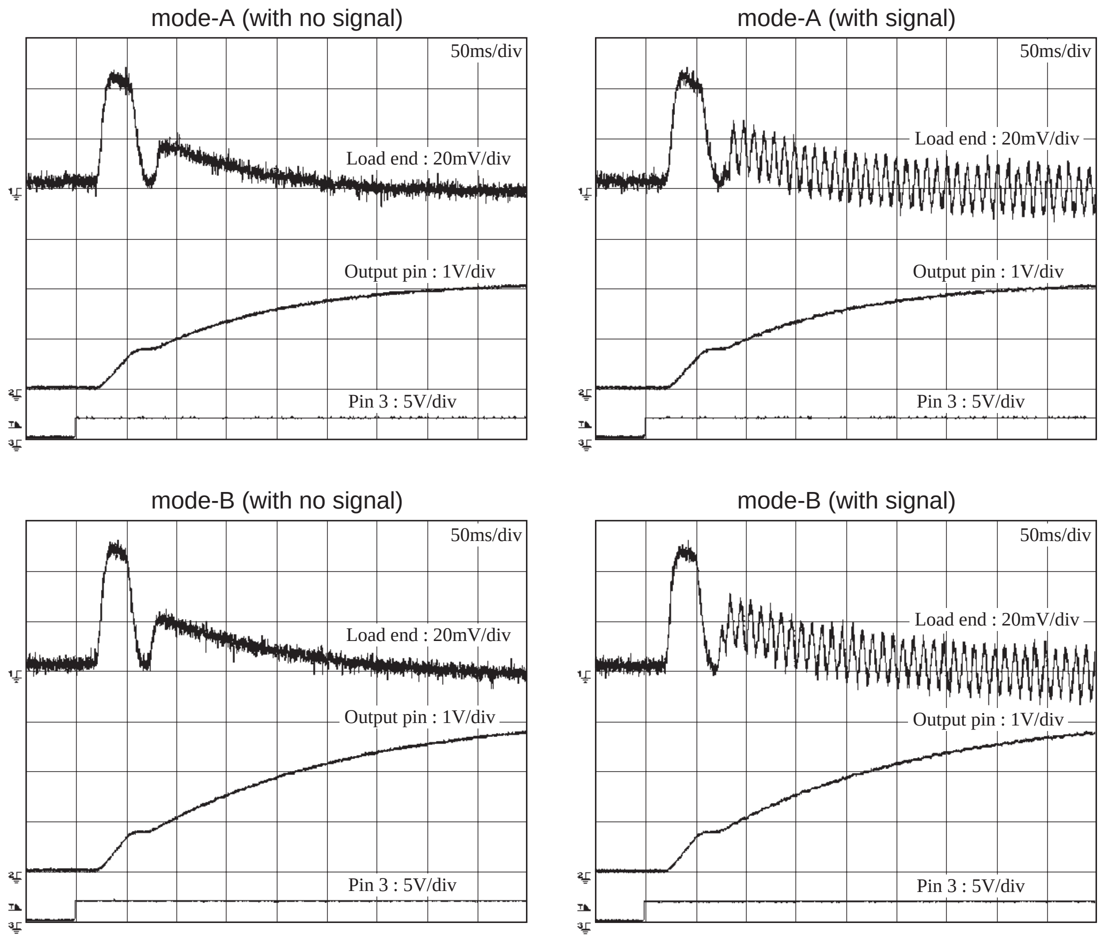
$I_{CCO}P$ – Ta





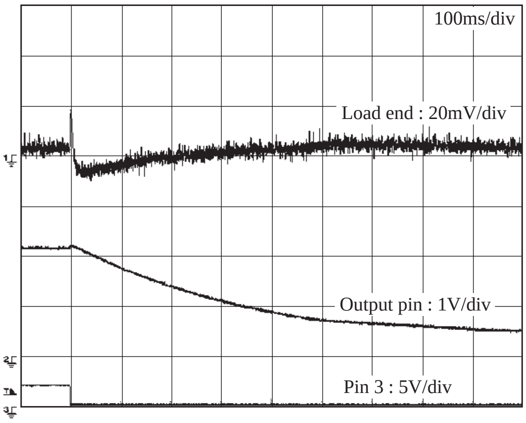


•**Transient response characteristics** (Rising characteristics)

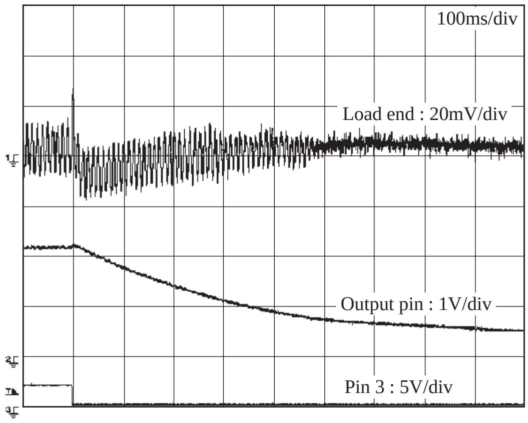


•Transient response characteristics (Falling characteristics)

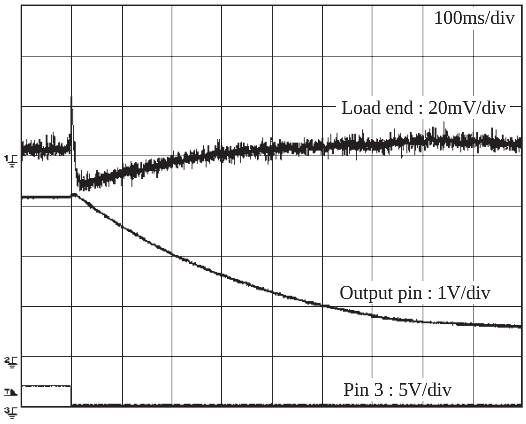
mode-A (with no signal)



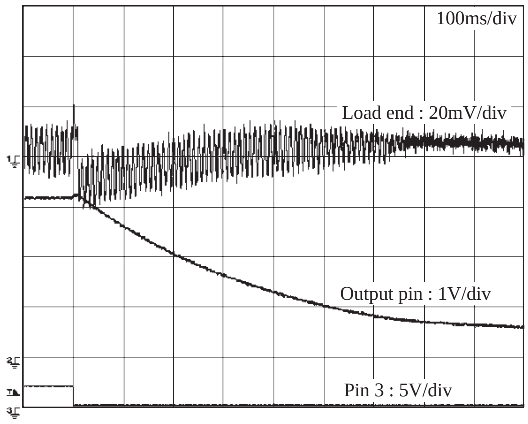
mode-A (with signal)



mode-B (with no signal)



mode-B (with signal)



This catalog provides information as of October, 2009. Specifications and information herein are subject to change without notice.