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Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- $\pm 450\text{mA}$ Load Current
- 1.2V Typical Total V_{sat} at 450mA
- Programmable Over-Current Control
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Range Bandwidth Control
- Inhibit Input and UVLO
- 3V to 15V Operation
- 12mA Quiescent Supply Current

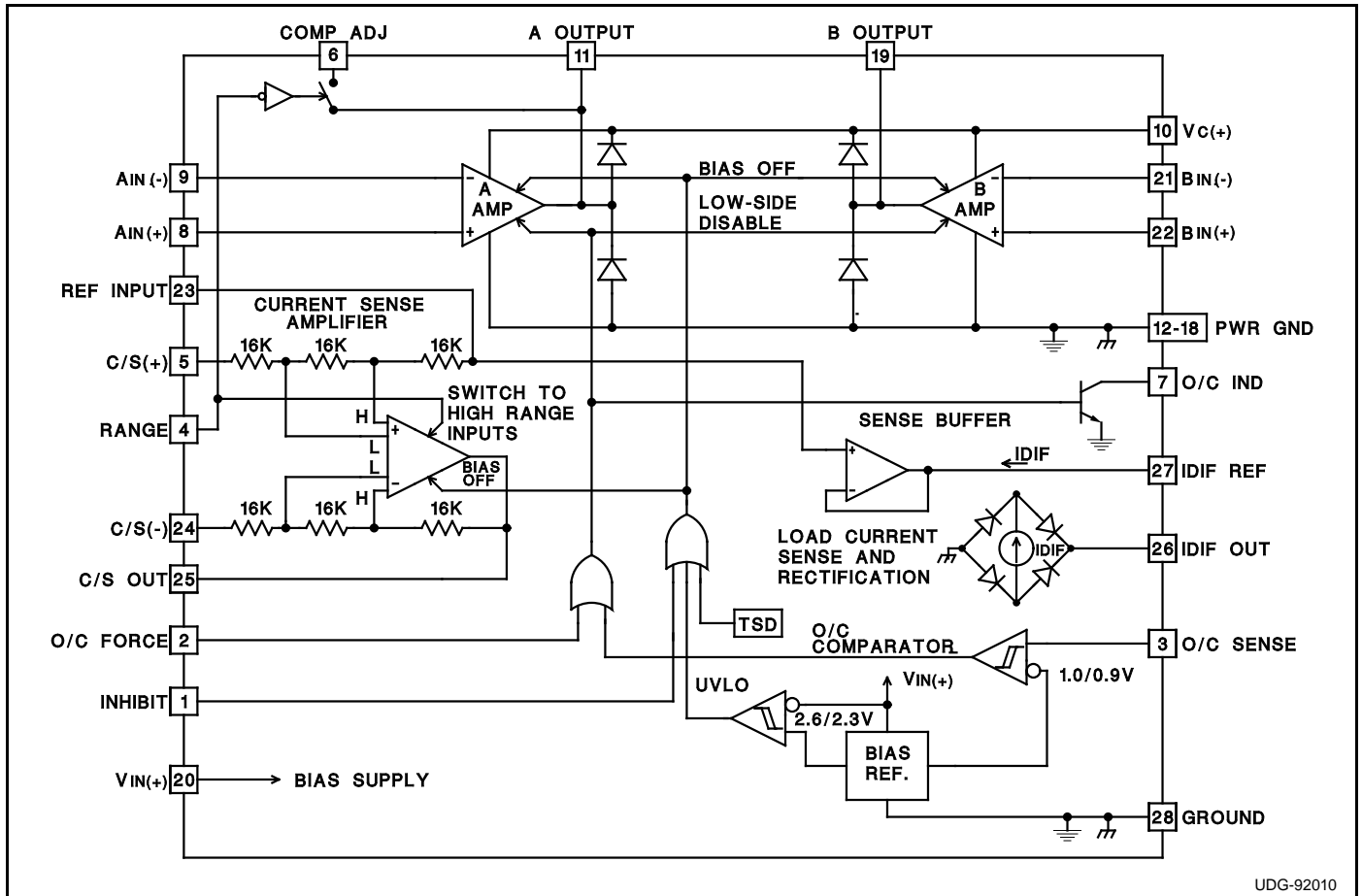
DESCRIPTION

The UC3178 full-bridge power amplifier, rated for continuous output current of 0.45 Amperes, is intended for use in demanding servo applications. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3178 is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited, the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a load current sensing and rectification function that can be configured with the device's over-current comparator to provide tight control on the maximum commanded load current. The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

This device is packaged a power PLCC, "QP" package which maintains a standard 28-pin outline, but with 7 pins along one edge directly tied to the die substrate for improved thermal performance.

BLOCK DIAGRAM



UDG-92010

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (VIN(+), VC(+))	20V
O/C Sense, Logic Inputs, and REF Input	
Maximum forced voltage	-0.3V to 10V
Maximum forced current	±10mA
A & B Amplifier Inputs	-0.3V to (VIN(+)+ 1.0V)
O/C Indicate Open Collector Output Voltage	20V
A and B Output Currents(continuous)	
Source	Internally Limited
Sink	0.6A
Output Diode Current (pulsed)*	0.5A
O/C Ind Output Current(continuous)	20mA
Operating Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C

*Notes: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.

THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)

Thermal Resistance Junction to Leads, θ_{jl}	15°C/W
Thermal Resistance Junction to Ambient, θ_{ja}	30-40°C/W

Note: The above numbers for θ_{jl} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{ja} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAM

PLCC - 28 (Top View) QP Package		PACKAGE PIN FUNCTION	
FUNCTION	PIN	FUNCTION	PIN
Inhibit	1	Vc(+) Supply	10
O/C Force	2	A Output	11
O/C Sense	3	Pwr Gnd	12
Range	4	Pwr Gnd	13
C/S(+)	5	Pwr Gnd	14
Comp Adj	6	Pwr Gnd	15
O/C Ind	7	Pwr Gnd	16
AIN(+)	8	Pwr Gnd	17
AIN(-)	9	Pwr Gnd	18
B Output	19	VIN(+)	20
Vc(+) Supply	10	BIN(-)	21
A Output	11	BIN(+)	22
Pwr Gnd	12	REF Input	23
Pwr Gnd	13	C/S(-)	24
Pwr Gnd	14	C/S Out	25
Pwr Gnd	15	IDIF Out	26
Pwr Gnd	16	IDIF REF	27
Pwr Gnd	17	Ground	28
Pwr Gnd	18		

ELECTRICAL CHARACTERISTICS: Unless otherwise stated specifications hold for TA = 0°C to 70°C, VC(+) = VIN(+) = 12V, REF Input = VIN(+)/2, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN (+)Supply Current			12	16	mA
VC(+) Supply Current	IOUT = OA		1.2	2.0	mA
Total Supply Current	Supplies = 5V, IOUT = OA		12	16	mA
	Supplies = 12V, IOUT = OA		13	18	mA
VIN(+) UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysteresis			300		mV
Over-Current (O/C) Comparator					
Input Bias Current	V input = 0.8V	-1.0	-0.1		µA
Thresholds	low to high	0.97	1.0	1.03	V
Threshold Hysteresis		85	100	115	mV
O/C IND Vsat	IOUT = 5mA, V input low		0.2	0.45	V
O/C IND Leakage	VOUT = 20V			5.0	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, VCM = 6V			4.0	mV
	B Amplifier, VCM = 6V			12.0	mV
Input Bias Current	VCM = 6V	-500	-50		µA
CMRR	VCM = 0.5 to 13V, Supplies = 15V	70	90		dB
PSRR	VIN(+) = 4 to 15V, VCM = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, VOUT = 1V, IOUT = 300mA to VOUT = 10.5V, IOUT = -300mA	3.0	15.0		V/mV

ELECTRICAL CHARACTERISTICS (cont.):

Unless otherwise stated specifications hold for $T_A = 0^\circ\text{C}$ to 70°C , $V_C(+) = V_{IN}(+) = 12\text{V}$,
 REF Input = $V_{IN}(+)/2$, O/C Input & Inhibit Input = 0V .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Amplifiers A & B (cont.)					
Gain Bandwidth Product	A Amplifier		2.0		MHz
	B Amplifier		1.0		MHz
Slew Rate			1.0		V/ μs
High-Side Current Limit		0.45	0.65		A
Output Saturation Voltage	High-Side, $I_{OUT} = -100\text{mA}$		0.75		V
	High-Side, $I_{OUT} = -300\text{mA}$		0.85		V
	High-Side, $I_{OUT} = -450\text{mA}$		0.9		V
	Low-Side, $I_{OUT} = 100\text{mA}$		0.2		V
	Low-Side, $I_{OUT} = 300\text{mA}$		0.25		V
	Low-Side, $I_{OUT} = 450\text{mA}$		0.30		V
	Total V_{sat} , $I_{OUT} = 100\text{mA}$		0.95	1.2	V
	Total V_{sat} , $I_{OUT} = 300\text{mA}$		1.05	1.4	V
Total V_{sat} , $I_{OUT} = 450\text{mA}$		1.25	1.6	V	
High-Side Diode, V_f	$I_D = 450\text{mA}$		1.30		V
Current Sense Amplifier					
Input Offset Voltage	$V_{CM} = 6\text{V}$, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change with Common Mode Input	$V_{CM} = -1\text{V}$ to 13V , Supplies = 12V , Low Range Mode			2000	$\mu\text{V/V}$
	$V_{CM} = -1\text{V}$ to 13V , Supplies = 12V , High Range Mode			4000	$\mu\text{V/V}$
Voltage Gain	$V_{DIFF} = +1.0$ to -1.0V , $V_{cm} = 6\text{V}$, High Range Mode	0.485	0.50	0.515	V/V
	$V_{DIFF} = +1.0$ to -1.0V , $V_{cm} = 6\text{V}$, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, $I_{OUT} = 1\text{mA}$		0.1	0.3	V
	High-Side, $I_{OUT} = -1\text{mA}$, Referenced to = $V_{IN}(+)$		0.1	0.3	V
Input Bias Current at Ref. Input	(REF Input - C/S(+))/48kohms, $T_j = 25^\circ\text{C}$	15	21	27	$\mu\text{A/V}$
Load Current Sense and Rectification					
Sense Buffer Offset Voltage	REF Input to IDIF REF, $I_{OUT} = \pm 1\text{mA}$			10	mV
Sense Buffer CMRR	$I_{OUT} = \pm 1\text{mA}$, REF Input = 2V to 10V	70	90		dB
IDIF REF to IDIF Out Current Ratio	IDIF = $\pm 100\mu\text{A}$, IDIF Out = 1V	0.95	1.0	1.05	A/A
	IDIF = $\pm 1\text{mA}$, IDIF Out = 1V	0.94	1.0	1.06	A/A
IDIF Out Supply Sensitivity	IDIF Out = $\pm 1\text{mA}$, $V_{IN}(+) = 4\text{V}$ to 15V , REF Input = 2V		1.0	5.0	$\mu\text{A/V}$
IDIF Out Common Mode Sensitivity (Δ IDIF Out/ Δ REF Input)	$I_{OUT} = \pm 1\text{mA}$, REF Input = 2V to 10V , IDIF Out = 1V		1.0	5.0	$\mu\text{A/V}$
Auxiliary Functions					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		μA
O/C Force Input Threshold		0.6	1.1	1.7	V
O/C Force Input Current	O/C Force Input = 1.7V		50	100	μA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	μA
COMP ADJ Pin Saturation Voltage	Range Input = 0V , Pin Current = $\pm 500\mu\text{A}$, Referenced to A_{OUT}		0.02	0.1	V
COMP ADJ Leakage Current	Range Input = 1.7V , Supplies = 12V $A_{OUT} - V_{Comp Adj} = \pm 6\text{V}$			5.0	μA
Total Supply Current When Inhibited	$V_{IN}(+)$ and $V_C(+)$ currents		1.0	1.5	mA
Thermal Shutdown Temperature			165		$^\circ\text{C}$

PIN DESCRIPTIONS:

A & B OUT: Outputs for the A & B power amplifiers, providing differential drive to the load during normal operation. During a UVLO, Inhibit, or O/C condition both of these outputs will be in a high, source only state. High-side diodes are included to catch inductive load currents flowing into these pins, inductive kicks on the low-side are caught by the high-side output transistors.

AIN(+): Non-inverting input to the A amplifier. Normally tied to the REF Input when the current sense amplifier is used.

AIN(-): Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

BIN(+): Non-inverting input to the B amplifier. This pin normally sets the reference point for the differential voltage swing at the load.

BIN(-): Inverting input to the B amplifier. Used to program the gain of the B amplifier.

COMP ADJ: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

C/S(+): The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

$$(REF\ Input / 2) - 0.3V.$$

C/S(-): The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, O/C comparator, and other low-level circuitry.

IDIF OUT: Current source output pin. The value of the output current is nominally equal to the magnitude of the current through the IDIF REF pin.

IDIF REF: Output of the IDIF sense buffer. Voltage on this pin will track the applied voltage on the REF Input pin. Current through this pin is full wave rectified and appears as a current sourced from the IDIF OUT pin.

Inhibit : A high impedance logic input that disables the A and B power amplifiers, the IDIF sense buffer, and the Current Sense amplifier. This input has an internal pull-up that will inhibit the device if the input is left open.

O/C Force: Logic input that forces the O/C condition.

O/C IND: Open collector output that indicates, with an active low state, an O/C condition.

O/C Sense: Input to the Over Current Comparator. When this input is above its 1V threshold the low-side devices of both the A & B power amplifiers will be disabled forcing a high, source only, state at both outputs.

PWR GND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

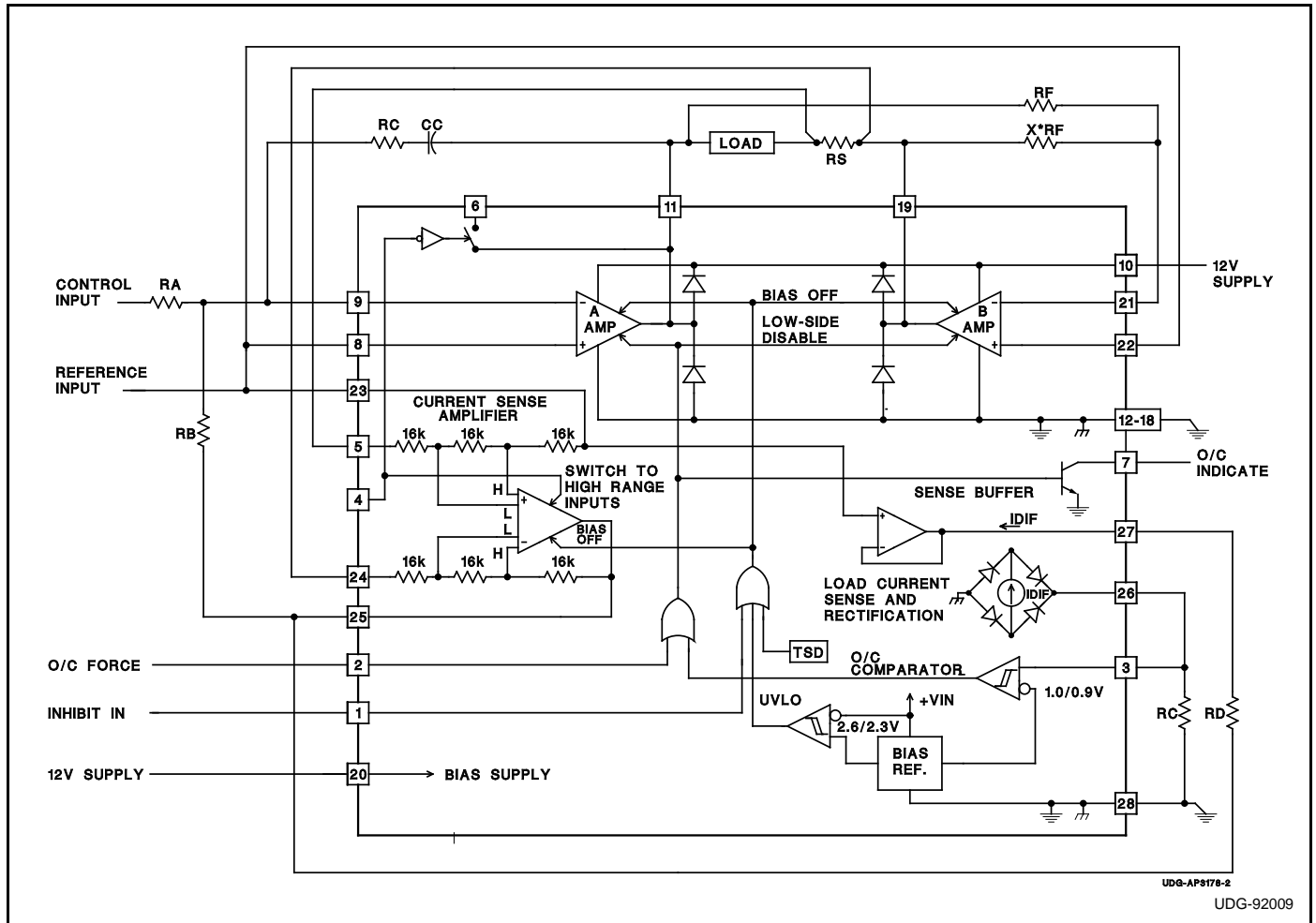
Range: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REF Input: Sets the Reference level at the C/S Output, and is normally tied to the system reference level for inputs to the power amplifier.

VIN(+): Provides bias supply to the device. The High-Side drive to the power stages on both the A and B amplifiers is referenced to this pin. The High-side saturation voltages, and UVLO are specified and measured with respect to this supply pin.

Vc(+): This supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are to be activated. This pin can operate approximately 400mV below the VIN(+) supply without affecting the voltage available to the load.

TYPICAL APPLICATION



Power amplifier transconductance

$$G_o = \frac{I_l}{V_s} = \frac{R_B}{R_A} \cdot \frac{1}{A_{V_{CS}} \cdot R_S}$$

Peak commanded load current

$$I_{MAX} = V_{O/C} \cdot \frac{R_D}{R_S \cdot A_{V_{CS}} \cdot R_E}$$

where:

- I_l is the load current
- V_s is the input command voltage
- $A_{V_{CS}}$ is the current sense amplifier gain
 - = 2.0 in low range mode
 - = 0.5 in high range mode
- $V_{O/C}$ is the 1.0V over-current comparator threshold

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UC3178QP	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

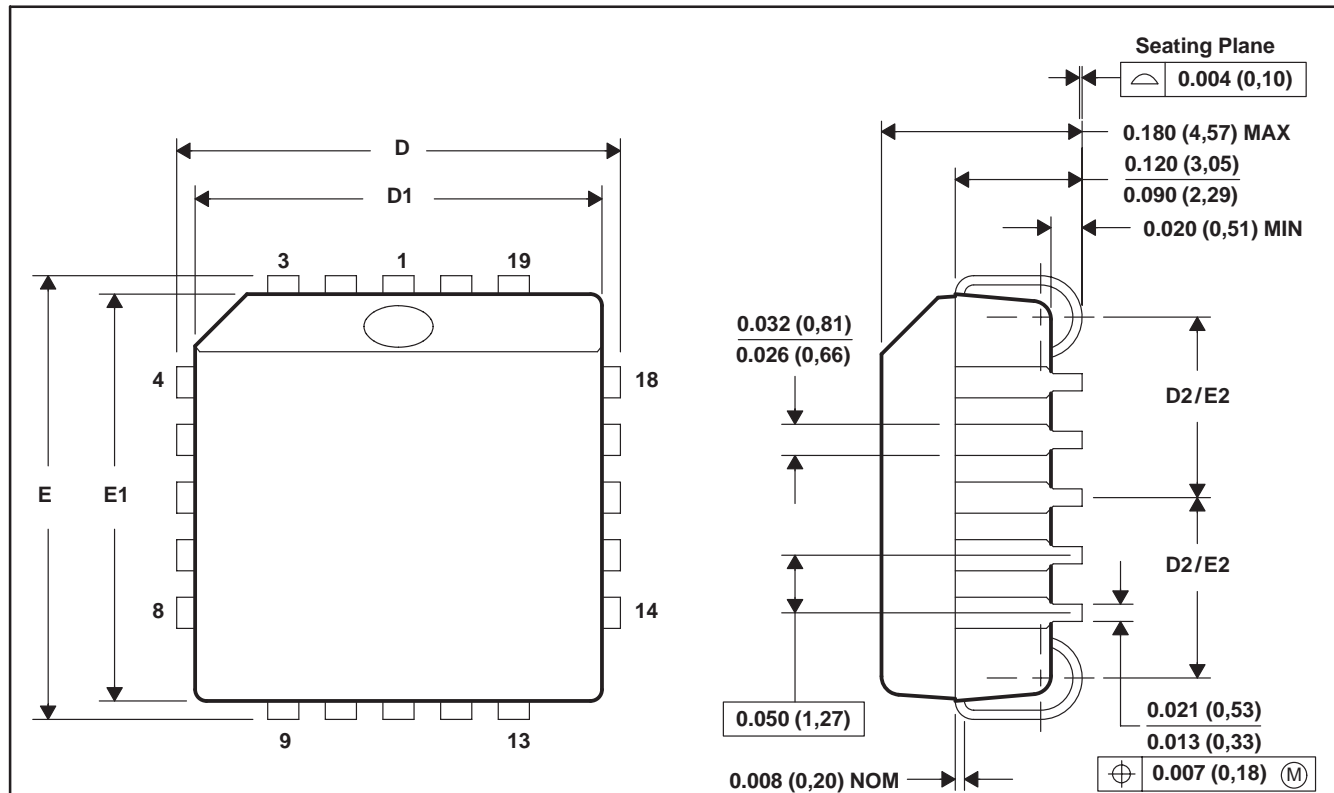
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FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

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 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-018

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