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### FEATURES

- Low Input Offset Voltage: 75  $\mu\text{V}$  Max**
- Low Offset Voltage Drift, Over  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ :**  
0.5  $\mu\text{V}/^\circ\text{C}$  Max
- Low Supply Current (Per Amplifier): 725  $\mu\text{A}$  Max**
- High Open-Loop Gain: 5000 V/mV Min**
- Low Input Bias Current: 2 nA Max**
- Low Noise Voltage Density: 11 nV/ $\sqrt{\text{Hz}}$  at 1 kHz**
- Stable with Large Capacitive Loads: 10 nF Typ**
- Pin Compatible to OP221, MC1458, and LT1013 with Improved Performance**
- Available in Die Form**

### GENERAL DESCRIPTION

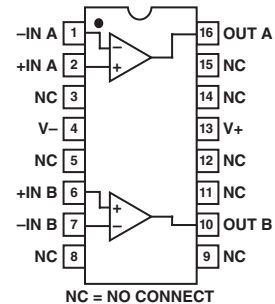
The OP200 is the first monolithic dual operational amplifier to offer OP77 type precision performance. Available in the industry-standard 8-lead pinout, the OP200 combines precision performance with the space and cost savings offered by a dual amplifier.

The OP200 features an extremely low input offset voltage of less than 75  $\mu\text{V}$  with a drift below 0.5  $\mu\text{V}/^\circ\text{C}$ , guaranteed over the full military temperature range. Open-loop gain of the OP200 exceeds 5,000,000 into a 10 k $\Omega$  load; input bias current is under 2 nA; CMR is over 120 dB and PSRR below 1.8  $\mu\text{V}/\text{V}$ . On-chip Zener zap trimming is used to achieve the extremely low input offset voltage of the OP200 and eliminates the need for offset pulling.

Power consumption of the OP200 is very low, with each amplifier drawing less than 725  $\mu\text{A}$  of supply current. The total current drawn by the dual OP200 is less than one-half that of a single OP07, yet the OP200 offers significant improvements over this industry-standard op amp. The voltage noise density of the OP200, 11 nV/ $\sqrt{\text{Hz}}$  at 1 kHz, is half that of most competitive devices.

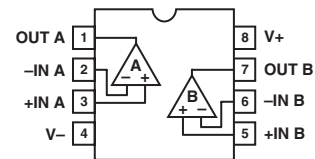
### PIN CONNECTIONS

#### 16-Lead SOIC (S-Suffix)



#### 8-Lead PDIP (P-Suffix)

#### 8-Lead CERDIP (Z-Suffix)



The OP200 is pin compatible with the OP221, LM158, MC1458/1558, and LT1013.

The OP200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP400.

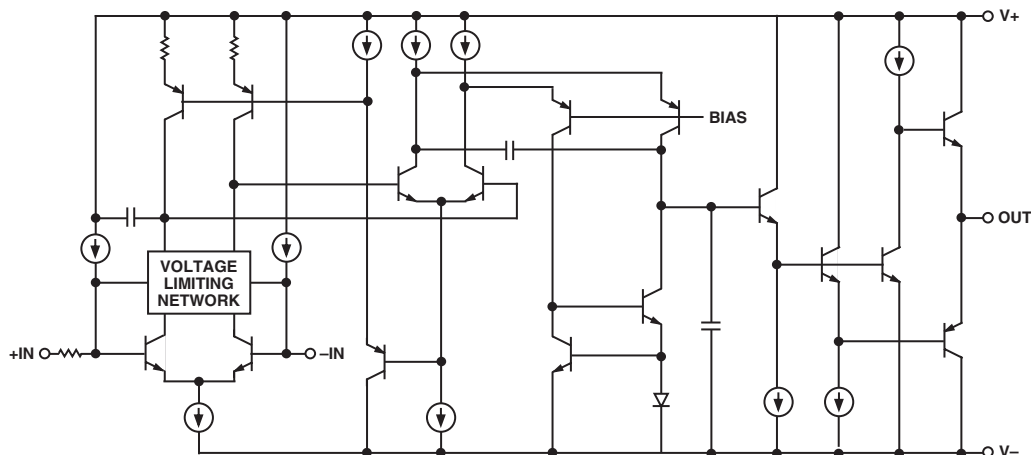


Figure 1. Simplified Schematic (One of two amplifiers is shown.)

### REV. B

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# OP200—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ( $V_S = \pm 15\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A/E			OP200G			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			25	75		80	200	$\mu\text{V}$
Long-Term Input Voltage Stability				0.1			0.1		$\mu\text{V}/\text{mo}$
Input Offset Current	$I_{OS}$	$V_{CM} = 0\text{ V}$		0.05	1.0		0.05	3.5	nA
Input Bias Current	$I_B$	$V_{CM} = 0\text{ V}$		0.1	2.0		0.1	5.0	nA
Input Noise Voltage	$e_{n\text{ p-p}}$	0.1 Hz to 10 Hz		0.5			0.5		$\mu\text{V}_{\text{p-p}}$
Input Noise Voltage Density*	$e_n$	$f_O = 10\text{ Hz}$ $f_O = 1000\text{ Hz}$		22 11	36 18		22 11		$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current	$i_{n\text{ p-p}}$	0.1 Hz to 10 Hz		15			15		$\text{pA}_{\text{p-p}}$
Input Noise Current Density	$i_n$	$f_O = 10\text{ Hz}$		0.4			0.4		$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance Differential Mode	$R_{IN}$			10			10		$\text{M}\Omega$
Input Resistance Common Mode	$R_{INCM}$			125			125		$\text{G}\Omega$
Large Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10\text{ V}$ $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	5000 2000	12000 3700		3000 1500	7000 3200		M/mV

\*Sample tested.

Specifications subject to change without notice.

**ELECTRICAL CHARACTERISTICS** ( $V_S = 15\text{ V}$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  for OP200A, unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A			Unit
			Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			45	125	$\mu\text{V}$
Average Input Offset Voltage Drift	$TCV_{OS}$			0.2	0.5	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$	$V_{CM} = 0\text{ V}$		0.15	2.5	nA
Input Bias Current	$I_B$	$V_{CM} = 0\text{ V}$		0.9	5.0	nA
Large Signal Voltage Gain	$A_{VO}$	$V_O = 10\text{ V}$ $R_L = 10\ \Omega$ $R_L = 2\text{ k}\Omega$	3000	9000		$\text{V}/\text{mV}$
			1000	2700		$\text{V}/\text{mV}$
Input Voltage Range*	IVR		$\pm 12$	$\pm 12.5$		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12\text{ V}$	115	130		dB
Power Supply Rejection Ratio	PSRR	$V_S = +3\text{ V to } +18\text{ V}$		0.2	3.2	$\mu\text{V}/\text{V}$
Output Voltage Swing	$V_O$	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	$\pm 12$	$\pm 12.4$		V
			$\pm 11$	$\pm 12$		V
Supply Current Per Amplifier	$I_{SY}$	No Load		600	775	$\mu\text{A}$
Capacitive Load Stability		$A_V = 1$		8		nF

\*Guaranteed by CMR test.

Specifications subject to change without notice.

**ELECTRICAL CHARACTERISTICS** ( $V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	OP200A/E			OP200G			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Voltage Range <sup>1</sup>	IVR		$\pm 12$	$\pm 13$		$\pm 12$	$\pm 13$		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12\text{ V}$	120	135		110	130		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V}$ to $\pm 18\text{ V}$		0.4	1.8		0.6	5.6	$\mu\text{V}/\text{V}$
Output Voltage Swing	$V_O$	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	$\pm 12$	$\pm 12.6$		$\pm 12$	$\pm 12.6$		V
			$\pm 11$	$\pm 12.2$		$\pm 11$	$\pm 12.2$		V
Supply Current Per Amplifier	$I_{SY}$	No Load		570	725		570	725	$\mu\text{A}$
Slew Rate	SR		0.1	0.15		0.1	0.15		$\text{V}/\mu\text{S}$
Gain Bandwidth Product	GBWP	$A_V = 1$		500			500		kHz
Channel Separation <sup>2</sup>	CS	$V_O = 20\text{ V p-p}$ $f_O = 10\text{ Hz}$	123	145		123	145		dB
Input Capacitance	$C_{IN}$			3.2			3.2		pF
Capacitive Load Stability		$A_V = 1$ No Oscillations		10			10		nF

NOTES

<sup>1</sup>Guaranteed by CMR test.

<sup>2</sup>Guaranteed but not 100% tested.

Specifications subject to change without notice.

# OP200—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ( $V_S = \pm 15\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	OP200E			OP200G			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{OS}$			35	100		110	300	$\mu\text{V}$
Average Input Offset Voltage Drift	$\text{TCV}_{OS}$			0.2	0.5		0.6	2.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	$I_{OS}$	$V_{CM} = 0\text{ V}$		0.08	2.5		0.1	6.0	nA
Input Bias Current	$I_B$	$V_{CM} = 0\text{ V}$		0.3	5.0		0.5	10.0	nA
Large-Signal Voltage Gain	$A_{VO}$	$V_O = \pm 10\text{ V}$ $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	3000 1500	10000 3200		2000 1000	5000 2500		V/mV V/mV
Input Voltage Range*	IVR		$\pm 12$	$\pm 12.5$		$\pm 12$	$\pm 12.5$		V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12\text{ V}$	115	130		105	130		dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3\text{ V}$ to $\pm 18\text{ V}$		0.15	3.2		0.3	10.0	$\mu\text{V}/\text{V}$
Output Voltage Swing	$V_O$	$R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$	$\pm 12$ $\pm 11$	$\pm 12.4$ $\pm 12$		$\pm 12$ $\pm 11$	$\pm 12.4$ $\pm 12.2$		V V
Supply Current Per Amplifier	$I_{SY}$	No Load		600	775		600	775	$\mu\text{A}$
Capacitive Load Stability		$A_V = 1$ No Oscillations		10 10			10 10		nF nF

\*Guaranteed by CMR test.

Specifications subject to change without notice.

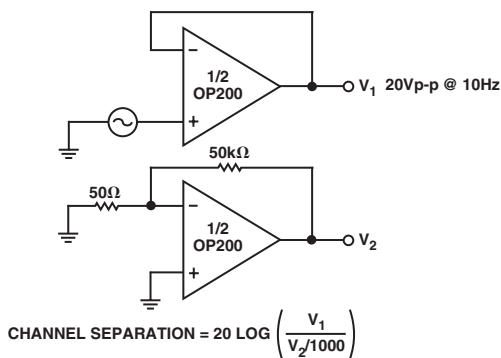


Figure 2. Channel Separation Test Circuit

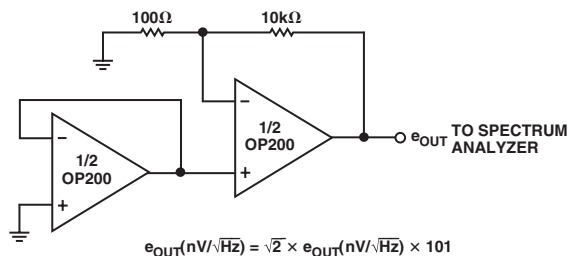


Figure 3. Noise Test Schematic

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	±20 V
Differential Input Voltage	±30 V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, S, Z-Package	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature (T <sub>J</sub> )	-65°C to +150°C
Operating Temperature Range	
OP200A	-55°C to +125°C
OP200E	-40°C to +85°C
OP200G	-40°C to +85°C

Package Type	θ <sub>JA</sub> <sup>2</sup>	θ <sub>JC</sub>	Unit
8-Lead Cerdip (Z)	148	16	°C/W
8-Lead Plastic DIP (P)	96	37	°C/W
16-Lead SOIC (S)	92	27	°C/W

**NOTES**

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

<sup>2</sup>θ<sub>JA</sub> is specified for worst-case mounting conditions, i.e., θ<sub>JA</sub> is specified for device in socket for Cerdip and PDIP packages; θ<sub>JA</sub> is specified for device soldered to printed circuit board for SOIC package.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP200 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**ORDERING GUIDE**

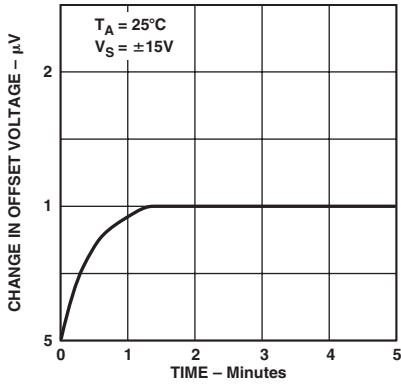
T <sub>A</sub> = 25°C V <sub>OS</sub> Max (μV)	Package		Operating Temperature Range
	CERDIP 8-Lead	Plastic	
75	OP200AZ		MIL
75	OP200EZ		XIND
200		OP200GP	XIND
200		OP200GS	XIND
200		OP200GS-REEL	XIND

For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at [www.dsccl.dla.mil/programs/milspec/default.asp](http://www.dsccl.dla.mil/programs/milspec/default.asp)

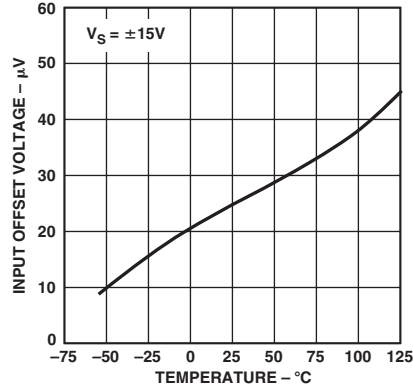
SMD Part Number	ADI Equivalent
5962-8859301M2A	OP200ARCMDA
5962-8859301MPA	OP200AZMDA



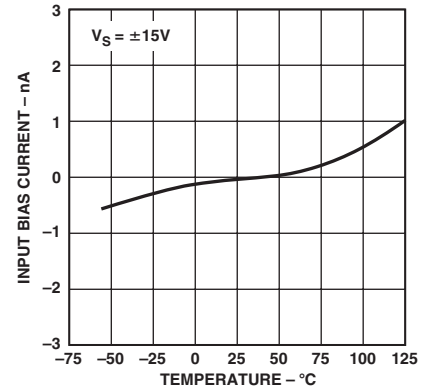
# OP200—Typical Performance Characteristics



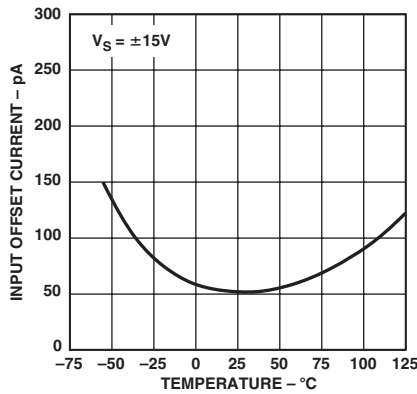
TPC 1. Warm-Up Drift



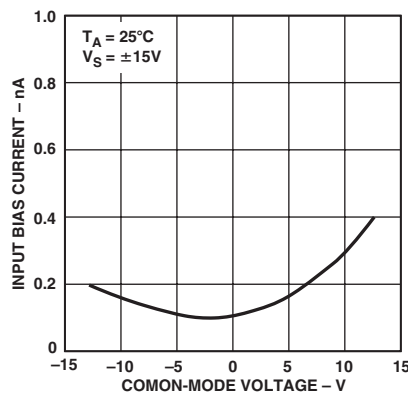
TPC 2. Input Offset Voltage vs. Temperature



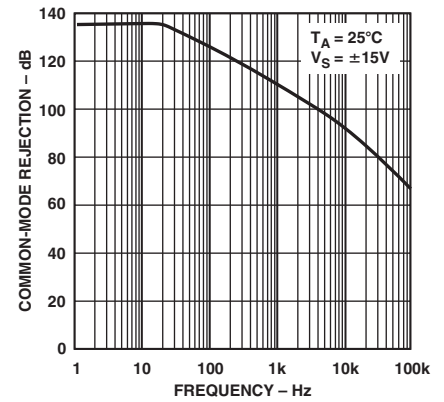
TPC 3. Input Bias Current vs. Temperature



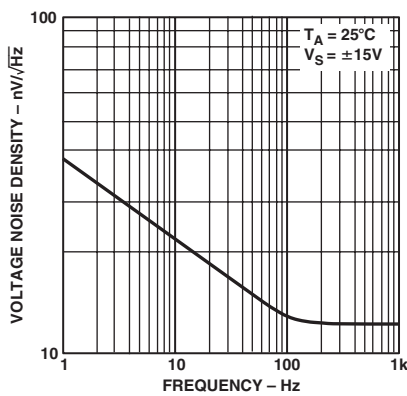
TPC 4. Input Offset Current vs. Temperature



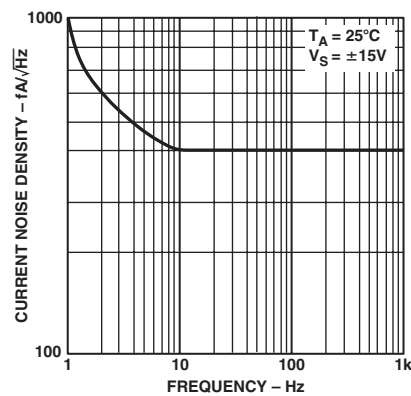
TPC 5. Input Bias Current vs. Common-Mode Voltage



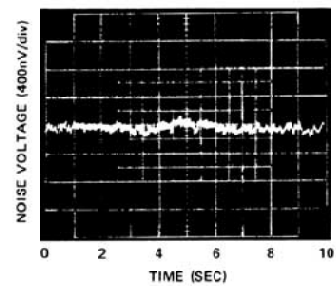
TPC 6. Common-Mode Rejection vs. Frequency



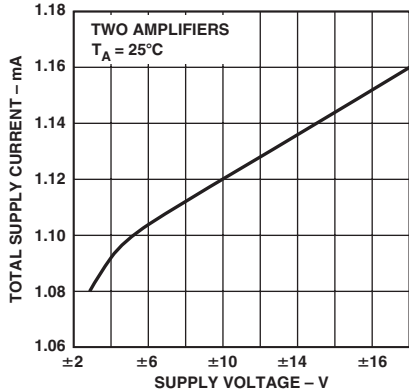
TPC 7. Voltage Noise Density vs. Frequency



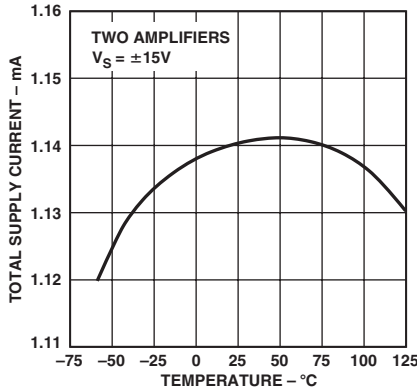
TPC 8. Current Noise Density vs. Frequency



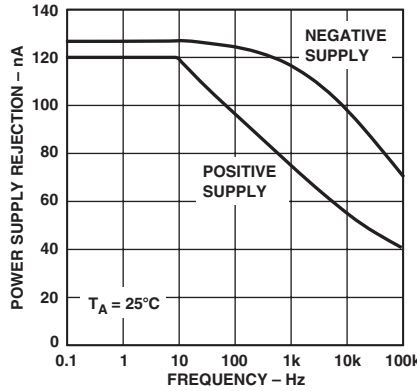
TPC 9. 0.1 to 10 Hz Noise



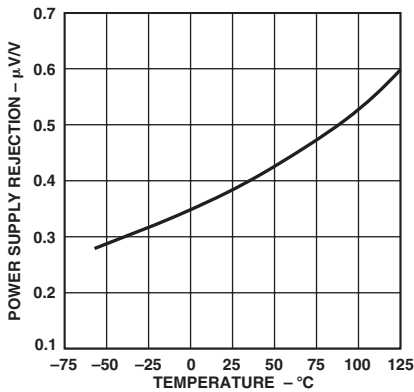
TPC 10. Total Supply Current vs. Supply Voltage



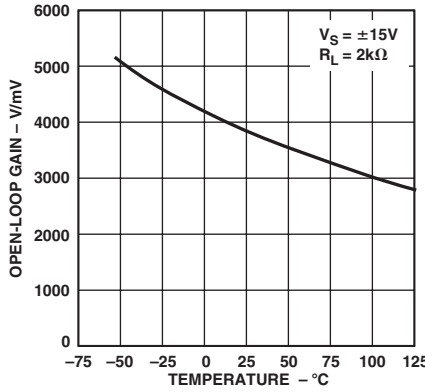
TPC 11. Total Supply Current vs. Temperature



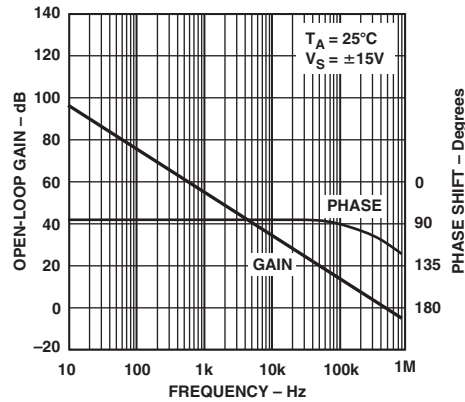
TPC 12. Power Supply Rejection vs. Frequency



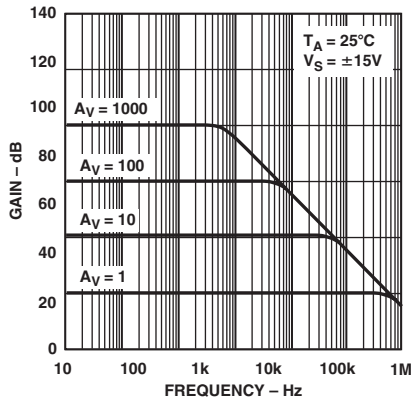
TPC 13. Power Supply Rejection vs. Temperature



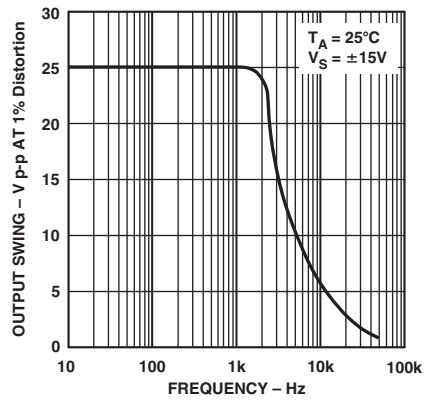
TPC 14. Open-Loop Gain vs. Temperature



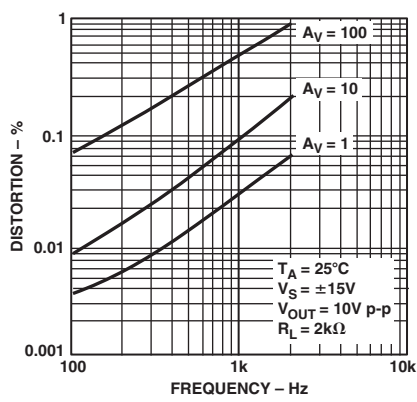
TPC 15. Open-Loop Gain and Phase Shift vs. Frequency



TPC 16. Closed-Loop Gain vs. Frequency



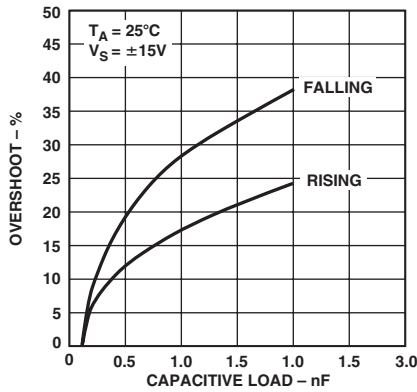
TPC 17. Maximum Output Swing vs. Frequency



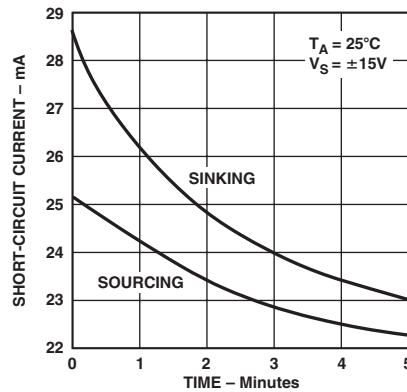
TPC 18. Total Harmonic Distortion vs. Frequency



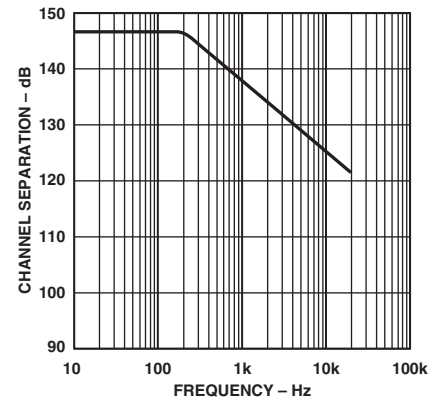
# OP200



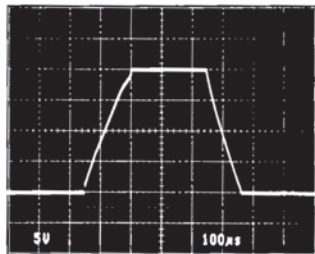
TPC 19. Overshoot vs. Capacitive Load



TPC 20. Short-Circuit Current vs. Time

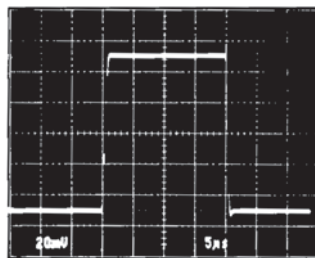


TPC 21. Channel Separation vs. Frequency



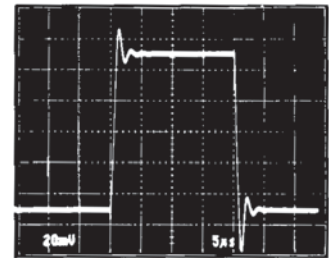
TA = 25°C  
VS = ±15V  
AV = +1

TPC 22. Large Signal Transient Response



TA = 25°C  
VS = ±15V  
AV = +1

TPC 23. Small Signal Transient Response



TA = 25°C  
VS = ±15V  
AV = +1

TPC 24. Small Signal Transient Response  $C_{LOAD} = 1 \text{ nF}$

## APPLICATIONS INFORMATION

The OP200 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP200.

## APPLICATIONS

### Dual Low-Power Instrumentation Amplifier

A dual instrumentation amplifier that consumes less than 33 mW of power per channel is shown in Figure 4. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115 dB (gain = 1000). Offset voltage drift is typically  $0.2 \mu\text{V}/^\circ\text{C}$  over the military temperature range, which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low power instrumentation amplifier is a function of gain and is shown below:

Gain	Bandwidth
5	150 kHz
10	67 kHz
100	7.5 kHz
1000	500 Hz

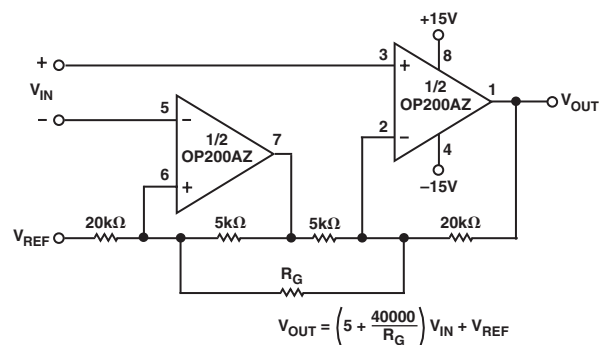


Figure 4. Dual Low Power Instrumentation Amplifier  
The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from  $-10 \text{ V}$  to  $+10 \text{ V}$  if required.

**Precision Absolute Value Amplifier**

The circuit in Figure 5 is a precision absolute value amplifier with an input impedance of 10 MΩ. The high gain and low TCV<sub>OS</sub> of the OP200 ensure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP200 exceeds 120 dB, yielding an error of less than 2 ppm.

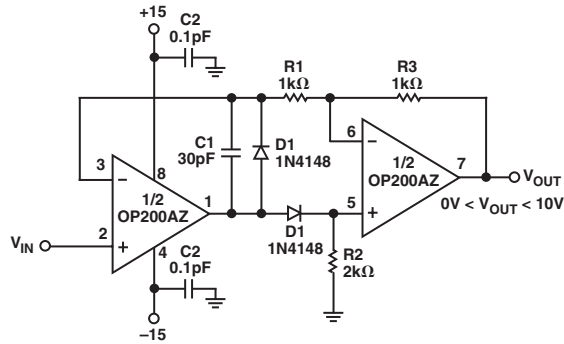


Figure 5. Precision Absolute Value Amplifier

**Precision Current Pump**

Maximum output current of the precision current pump shown in Figure 6 is ±10 mA. Voltage compliance is ±10 V with ±15 V supplies. Output impedance of the current transmitter exceeds 3 MΩ with linearity better than 16 bits.

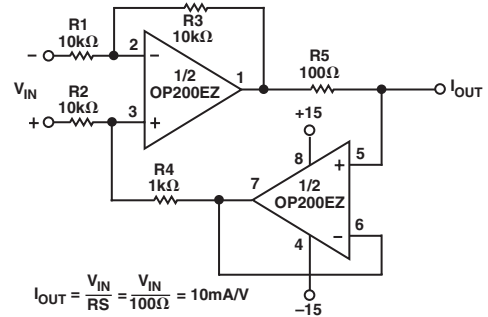


Figure 6. Precision Current Pump

**Dual 12-Bit Voltage Output DAC**

The dual output DAC shown in Figure 7 is capable of providing untrimmed 12-bit accurate operation over the entire military temperature range. Offset voltage, bias current, and gain errors of the OP200 contribute less than 1/10 of an LSB error at 12 bits over the military temperature range.

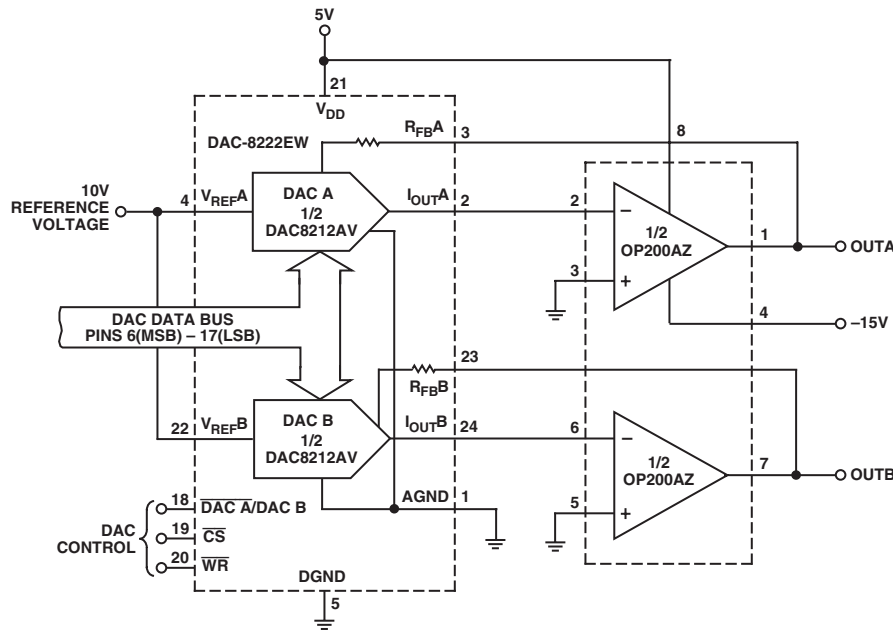


Figure 7. Dual 12-Bit Voltage Output DAC

# OP200

## Dual Precision Voltage Reference

A dual OP200 and a REF43, a 2.5 V reference, can be used to build a  $\pm 2.5$  V precision voltage reference. Maximum output current from each reference is  $\pm 10$  mA with load regulation under  $25 \mu\text{V}/\text{mA}$ . Line regulation is better than  $15 \mu\text{V}/\text{V}$  and output voltage drift is under  $20 \mu\text{V}/^\circ\text{C}$ . Output voltage noise from 0.1 Hz to 10 Hz is typically  $75 \mu\text{V}$  p-p. R1 and D1 ensure correct start-up.

## Programmable High Resolution Window Comparator

The programmable window comparator shown in Figure 9 is easily capable of 12-bit accuracy over the full military temperature range. A dual CMOS 12-bit DAC, the DAC8212, is used in the voltage switching mode to set the upper and lower thresholds (DAC A and DAC B, respectively).

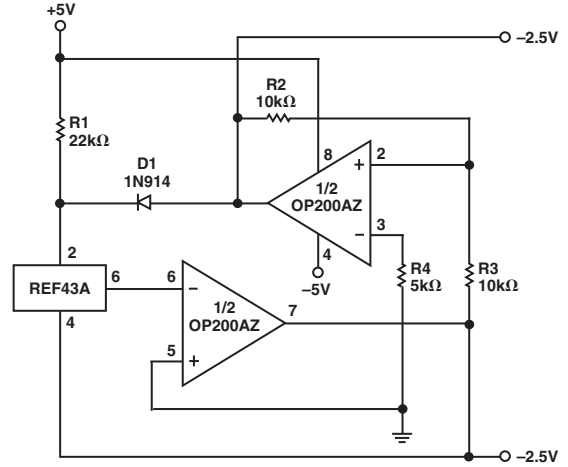


Figure 8. Dual Precision Voltage Reference

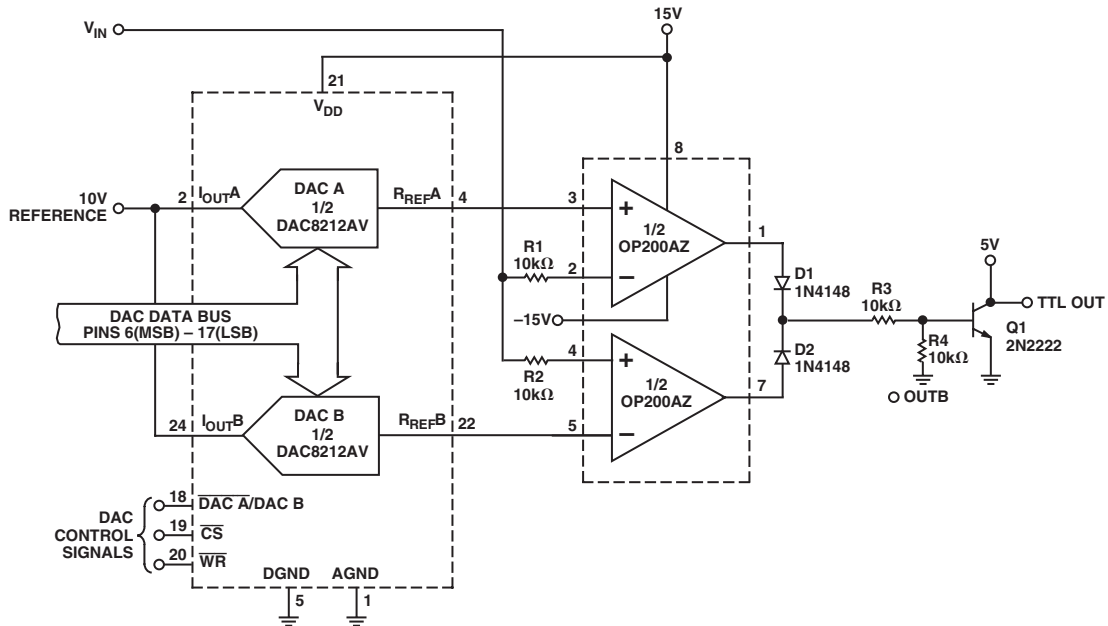
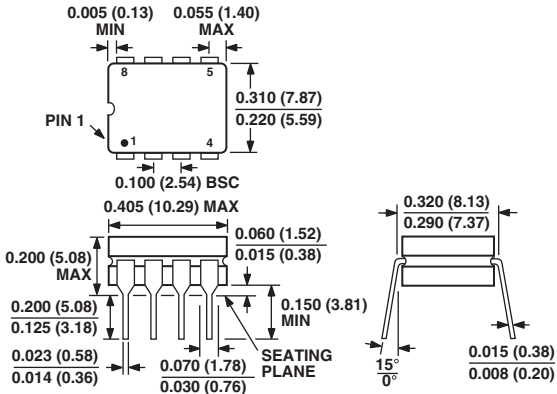


Figure 9. Programmable High Resolution Window Comparator

OUTLINE DIMENSIONS

8-Lead Ceramic Dual In-Line Package [CERDIP]  
(Q-8)  
Z-Suffix

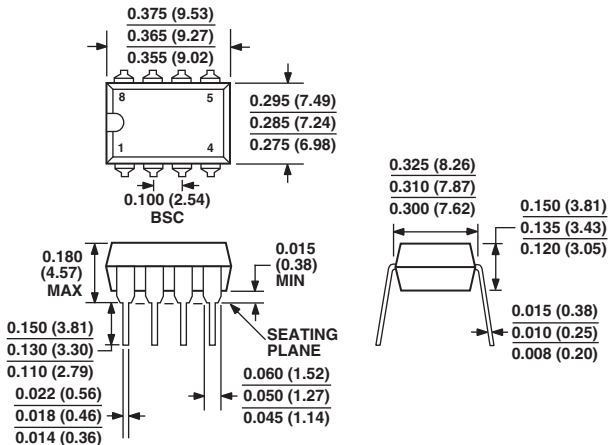
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual In-Line Package [PDIP]  
(N-8)  
P-Suffix

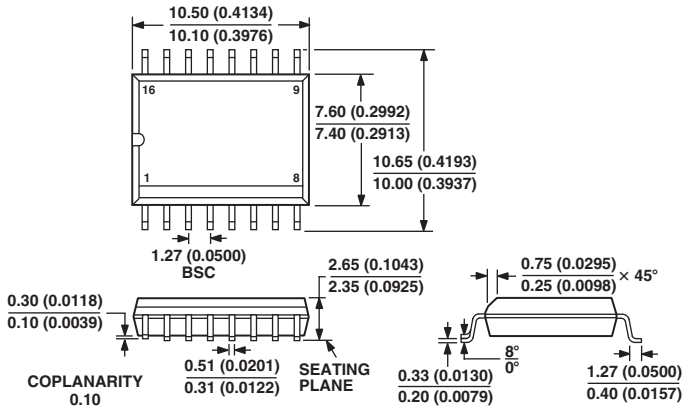
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Standard Small Outline Package [SOIC]  
Wide Body  
(RW-16)  
S-Suffix

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

# OP200

## Revision History

Location	Page
<b>2/04—Data Sheet changed from REV. A to REV. B.</b>	
OP200F deleted	Universal
Changes to ORDERING GUIDE	5
Changes to Figure 4	8
Updated OUTLINE DIMENSIONS	11
<b>4/02—Data Sheet changed from REV. 0 to REV. A.</b>	
Edits to FEATURES	1
Edits to GENERAL DESCRIPTION	1
Edits to ORDERING INFORMATION	1
Edits to PIN CONNECTIONS	1
Edits to ABSOLUTE MAXIMUM RATINGS	2
Edits to PACKAGE TYPE	2

C00322-0-2/04(B)