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S1D13517 External SDRAM LCD Controller

March 2009

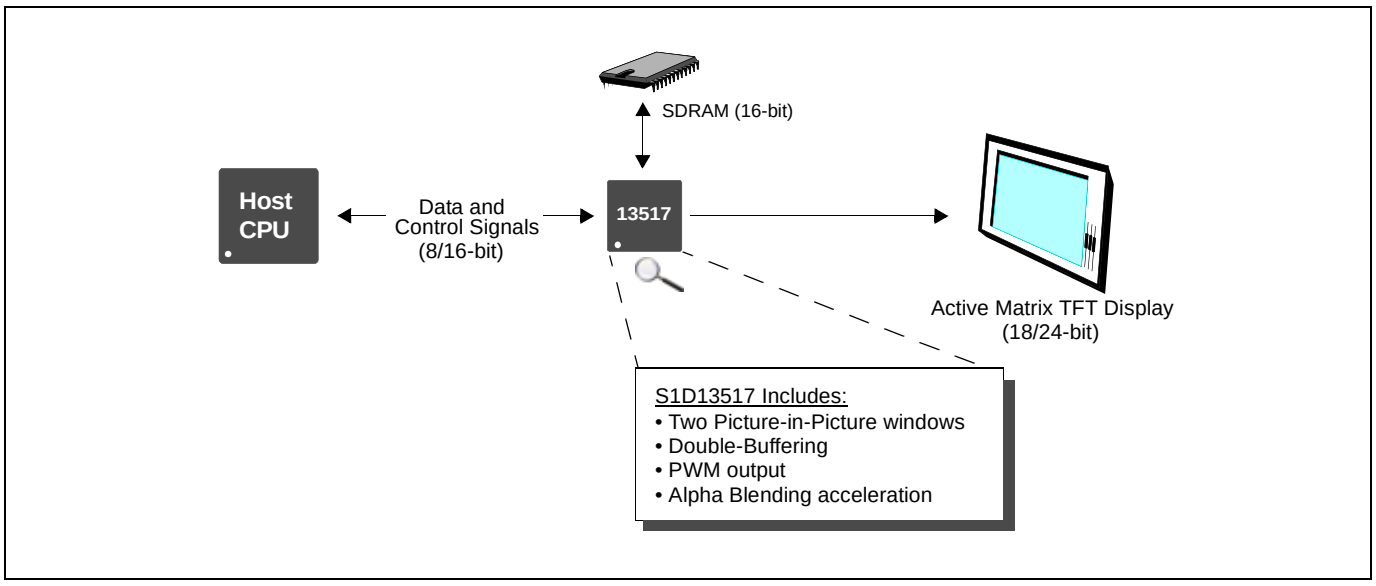
The S1D13517 is a color LCD graphics controller which uses an external SDRAM display buffer. The S1D13517 supports an 8/16-bit indirect host interface while providing high performance bandwidth to external SDRAM, allowing for fast screen updates.

The S1D13517 supports displays up to 960x540 (QHD) @ 24 bpp or 800x600 (SVGA)@ 24bpp, controlling a main the window and up to two Picture-in-Picture windows. Additionally, the S1D13517 is designed with a 2D Graphics Engine with Alpha Blending. The S1D13517 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates.

FEATURES

- Easy to use, Easy to connect
- External 16M-bit, 64M-bit or 128M-bit SDRAM
- High performance SDRAM controller
- 8/16-bit asynchronous indirect parallel interface (used for display or register data)
- Input data formats: RGB 8:8:8, RGB 5:6:5
- Active Matrix TFT interface: 18/24-bit interface
- Supports resolutions up to 960x540 or 800x600
- Software Power Save mode
- Main Display Window with two Picture-in-Picture windows
- 180° hardware rotation and mirror of display image
- Double-Buffer available to prevent image tearing during streaming input
- PWM output for LCD backlight control
- Internal programmable PLL
- SS (Spread spectrum) clock available
- General Purpose Output pins

SYSTEM BLOCK DIAGRAM



■ DESCRIPTION

Frame Buffer

- External 16M-bit, 64M-bit or 128M-bit SDRAM memory support
  - Maximum 90MHz SDRAM clock
  - 16-bit bus width
  - Maximum 16-Buffer separation available

Host Interface

- 8/16-bit asynchronous parallel interface (used for display or register data)
  - Indirect addressing Intel80 interface
  - Burst and rectangular write available for memory

Input Data Format

- RGB 8:8:8, RGB 5:6:5

Display Support

- Active Matrix TFT
  - 18/24-bit interface
- Supports resolution up to 960x560 (QHD)
  - HVGA, VGA, WVGA, SVGA

Power

- COREVDD 2.5 volts, PLLVDD 2.5 volts and IOVDD 3.3 volts

Display Features

- 24 bit-per-pixel (bpp) color depths
- Display window
- Two Picture-in-Picture windows
- 2D graphics engine (Alpha blending, Copy)
- 180° hardware rotation and mirror of display image.
- Double-Buffer available to prevent image tearing during streaming input
- Software Multi-Buffer available for simple animation
- TE (Tearing Effect) output

Clock Source

- Internal programmable PLL (Maximum 180MHz)
- Spread Spectrum clock available for PCLK and SDCLK (note: frequency: 31MHz to 80MHz)
- LCD pixel clock (Maximum PCLK = 45MHz)
- SDRAM clock (Maximum SDCLK = 90MHz

Miscellaneous

- PWM output for LCD backlight control
- Software Power Save mode
- General Purpose Output pins are available (GPO[3:0])
- QFP15 128-pin package (16mm x 16mm x 1.7mm)

CONTACT YOUR SALES REPRESENTATIVE FOR COMPREHENSIVE DESIGN TOOLS

- S1D13517 Technical Documentation
- CPU Independent Software Utilities
- S1D13517 Evaluation Boards
- Royalty Free source level driver code

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