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SYNC SEPARATOR WITH VARIABLE FILTER

DEVICE DESCRIPTION

The ZXFV4583 provides the ability to separate out video synchronization signals for a wide variety of TV and CRT display systems, standard and non-standard.

Flexibility arises from the use of just three external resistors to adapt to each application. One resistor controls a fully integrated internal color carrier filter with variable bandwidth. This filter avoids disturbance from the color carrier, permitting accurate threshold slicing for timing extraction.

A second resistor controls the voltage threshold for loss of signal detection after a time-out interval. The third resistor controls the timing functions.

DC restoration for displays is facilitated by the Back Porch synch output, which can be used to drive an external circuit to clamp the blanking voltage to a fixed level.

ORDERING INFORMATION

Part Number	Container	Increment
ZXFV4583N16TA	Reel 7″	500
ZXFV4583N16TC	Reel 13″	2500

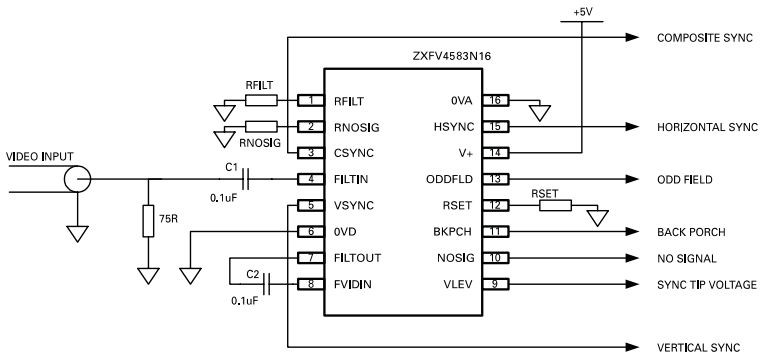
FEATURES AND BENEFITS

- PAL, NTSC, SECAM
- Variable filter for optimal accuracy
- Sync outputs: composite, horizontal, vertical, back porch, odd/even
- No-signal detector
- On chip sample / hold capacitors
- +5V single supply
- Default vertical output where there are no serration pulses
- Pin and layout compatible with part EL4583 in SO16N surface mount package

APPLICATIONS

- Digital image capture
- Video input systems requiring separation of picture timing
- Video distribution
- CCTV surveillance
- Digital multimedia
- Timing for black level clamp

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	-0.5V to +7V
Inputs to ground*	-0.5V to V_{CC} +0.5V
Operating temperature range	-40°C to 85°C
Storage	-65°C to +150°C
Operating ambient junction temperature	T_{JMAX}150°C**

**The thermal resistance from the semiconductor die to ambient is typically 120°C/W when the SO16 package is mounted on a PCB in free air. The power dissipation of the device when loaded must be designed to keep the device junction temperature below $T_{JMAX.}$

*During power-up and power-down, these voltage ratings require that signals be applied only when the power supply is connected.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, R_{SET} = 681kΩ, R_{FILT} = 22kΩ, R_{NOSIG} = 82kΩ, T_{amb} = 25°C unless otherwise stated.

Test level: P = 100% production test
C = Characterized only

PARAMETER	CONDITIONS	TEST	MIN	TYP	MAX	UNIT
DC Characteristics						
Supply current		P	2	4.5	6.5	mA
Clamp voltage at FILTIN	Pin 4 unloaded	P	1.2	1.35	1.5	V
Discharge current at FILTIN	Pin 4, Vin = 2V pk-pk	C		1		µA
Discharge current at FILTIN	Pin 4, no signal	C	3	6	12	µA
Clamp charge current at FILTIN	Pin 4, Vin = 1V pk-pk	P	2	3	4	mA
Clamp voltage at FVIDIN	Pin 8 unloaded	P	1.2	1.35	1.5	V
Discharge current at FVIDIN	Pin 8, Vin = 2V pk-pk	C		1		µA
Discharge current at FVIDIN	Pin 8, no signal	C	3	6	12	µA
Clamp charge current at FVIDIN	Pin 8, Vin = 1V pk-pk	P	2	3	4	mA
R_{SET} voltage, pin 12		P	1.5	1.75	2	V
R_{FILT} voltage, pin 1		P	0.35	0.5	0.65	V
RNOSIG current, pin 2		P	1.5	2.5	3.5	µA
Logic output low voltage, V_{OL}	I_{OL} = 1.6mA	P		0.35	0.8	V

ELECTRICAL CHARACTERISTICS (Cont.)

V_{CC} = 5V, R_{SET} = 681kΩ, R_{FILT} = 22kΩ, R_{NOSIG} = 82kΩ, T_{amb} = 25°C unless otherwise stated.

PARAMETER	CONDITIONS	TEST	MIN	TYP	MAX	UNIT
AC Characteristics						
FILTIN function input voltage range	PAL/NTSC	P	0.5		2	V pk-pk
Filter voltage gain	FILTIN to FILOUT	P	4.9	5.7	6.5	dB
Filter attenuation	4.4MHz for PAL, 3.6MHz for NTSC	P P	15 10	19 14		dB dB
Slice level	Vin = 1V pk-pk	P	40	50	60	%
CSYNC prop. Delay, t_{CS}	Relative to pin 4 input	P		250	400	ns
VSYNC delay		C		250		ns
VSYNC pulse width, t_{VSYNC} (PAL)		C		165		µs
VSYNC pulse width, t_{VSYNC} (NTSC)		C		195		µs
VSYNC default delay, t_{VSD}		P	30	36	45	µs
HSYNC delay		P		250		ns
HSYNC pulse width, t_{HSYNC}		P	3.8	5	6.2	µs
BKPCH delay, t_{BD}	Relative to pin 4 input	P		250	400	ns
BKPCH pulse width, t_B		P	2.7	3.7	4.7	µs

Note: In order to avoid coupling between high speed logic output signals and analog inputs, the test circuit layout uses connections from the logic output pins routed away from the analog pins. In the application, similar care in the layout is required, keeping resistors R_{FILT}, R_{NOSIG} and R_{SET} close to their respective pins, in particular routing signal CSYNC away from pins 1, 2 and 12.

CONNECTIONS

PIN No.	PIN NAME	TYPE	FUNCTION
1	R_{FILT}	Resistor control	Controls the input color carrier filter characteristic. An external resistor R_{FILT} connected from this pin to 0V sets the bandwidth. Smaller R_{FILT} gives increased bandwidth. See the detailed operating description below.
2	R_{NOSIG}	Resistor control	Controls the no-signal detector level. An external resistor R_{NOSIG} connected from this pin to 0V sets the threshold voltage level, according to the equation $V_{PMIN} = 0.75\ R_{NOSIG} / R_{SET}$ where V_{PMIN} is the minimum detected sync pulse amplitude at pin 4 and R_{SET} is the resistor value at pin 12.
3	CSYNC	Logic out	Composite sync logic output. Includes all sync pulses derived from the input video.
4	FILTIN	Analog in	Input to color carrier filter. This is the main analog (unfiltered) composite video input used when color carrier filtering is required. A voltage clamp circuit and adaptive current source are also included at this node. See the detailed operating description. When the filter is not used, this pin must be left open circuit.
5	VSYNC	Logic out	Vertical sync output. This is an active low pulse commencing on the first vertical sync pulse trailing (rising) edge and ending near the second next equalizing pulse. See timing diagram.
6	OVD	Ground	Provides ground return path for internal logic output buffer circuits. Normally connected externally to a common PCB ground plane.
7	FILTOUT	Analog out	Analog output signal from color carrier filter. The filter voltage gain is nominally 2. This output is normally capacitor-coupled to pin 8.
8	FVIDIN	Analog in	Input for filtered analog video signal input. This is the direct input to the sample/hold and sync slicing comparator providing the logic timing edges. This input is normally coupled via an external capacitor from FILTOUT, pin 7. It may be used as the signal input where the color carrier filter is not required. Includes a clamp similar that of pin 4.
9	VLEV	Analog out	Analog output, a positive voltage typically equal to twice the (negative) peak sync pulse amplitude if the filter is used.
10	NOSIG	Logic out	Logic output, which goes high after a time-out delay when no signal is present. The threshold level is controlled at pin 2.
11	BKPCH	Logic out	Burst or Back Porch logic output, an active low monostable pulse triggered from rising composite sync pulse edges. The width is set by R_{SET} to overlap most of the steady part of the back porch, assuming the color carrier burst has been attenuated sufficiently by filtering. This pulse is then suitable for controlling an external black level clamping circuit. See the timing diagram.
12	R_{SET}	Resistor control	Controls the timing interval of the sample/hold circuit and the monostable interval for the sync outputs according to the application. An external resistor, R_{SET} connected from this pin to 0V establishes the timing parameter, to which these times are scaled together. See the detailed operating description.
13	ODDFLD	Logic out	Odd field logic output. High during an odd numbered field, low during even. This output is timed with the start of the VSYNC pulse.
14	V+	Power in	Power supply input, +5V.
15	HSYNC	Logic out	Horizontal sync logic output. Monostable output derived from CSYNC falling edges, it achieves a steady stream of 5µs pulses. The half line events during the field blanking interval are eliminated. See timing diagram.

DETAILED DESCRIPTION

Introduction

This device includes all the functions required to separate out the critical timing points of most types of video signal. A sample-and-hold process is used to establish accurately the 50% point of the sync pulse. The input is also filtered to avoid the effect of the color carrier. The filter is coupled externally. The following paragraphs give a simplified description of the signal processing.

Color carrier filter

This low-pass filter provides adjustable attenuation of the color carrier with low distortion of the remaining sync pulses so as to ensure accurate timing of the extracted logic outputs. The control is via an external resistor R_{FILT} connected from pin 1 to ground. R_{FILT}=22kΩ gives corner frequency of ~1.3MHz corresponding to ~12dB attenuation @ 3.58MHz.(Corner freq. Proportional to $1/R_{FILT}$, minimum value 18kΩ). A graph shows how the bandwidth varies with the resistor value.

Clamping circuits

Clamping circuits are use to limit the signal swing excursion after AC coupling at both the input to the filter, FILTIN and the timing extractor input, FVIDIN. In each case, the sync tip level is maintained at a value of nominally 1.35V.

Sync timing extraction circuits

The waveforms are depicted in Timing Diagrams, **Figure 1** for PAL (625 lines) and **Figure 2** for NTSC (525 lines). Sample-and-hold circuits are used to obtain time-delayed voltage values of the sync tip and the back porch. The sample gates are controlled by a comparator sensing the video input relative to a threshold at a fixed offset above the sync tip clamp level. The sampled voltages are combined in a potential divider to derive the mean voltage (50% amplitude), which is used as the sync pulse threshold. A second comparator then provides **CSYNC**, the logic version of the composite sync signal. This is delayed slightly as shown in **Figure 3**. The time delay comprises that of the input filter and also the smaller delay of the comparator and logic. The timing of the sample hold and other time parameters are all controlled together in unison by the external resistor R_{SET}. A 1% resistor tolerance is recommended. The sync tip voltage level from the sample-and-hold is buffered and provided as an analog output, **VLEV.**

The vertical sync output **VSYNC** is derived from the Field pulse group. Where there are short equalization pulses in the standard systems, these short pulses are ignored. Essentially, a pulse width discriminator circuit senses the first of the Field pulses, as they are wider than those of the rest of the sequence. The trailing edge of the first negative-going Frame Pulse (i.e. the rising edge of the first "serration" pulse) triggers the VSYNC output. In systems with a frame interval with no serration pulses, a vertical sync output is provided after a default delay as in **Figure 4**. Also provided is an **ODDFLD** logic output, which is high during an odd-numbered field and low during an even one.

The horizontal sync **HSYNC** is a monostable output derived from the leading (falling) edge of the composite sync. The pulse width is about 5 µs. Also, during the Field blanking sequence, the additional half-line pulses are removed by a timing circuit with a pulse interval discrimination function controlled by R_{SET}. R_{SET} is normally set to 681kΩ for standard PAL or NTSC timings. Consequently the scan rate is inversely proportional to R_{SET}.

The Back Porch monostable output **BKPCH** is initiated from the trailing edge of the composite sync. The pulse is active low and the width is set according to R_{SET}.

Loss-of-Signal detector

Loss of signal is indicated by a logic high level at the output **NOSIG**. The decision threshold is set by an external resistor R_{NOSIG} connected from pin 2 to ground. R_{NOSIG} =100kΩ gives a shut off threshold of ~250mV of sync amplitude at FVIDIN or ~130mV on FILTIN (Threshold proportional to R_{NOSIG}, minimum value 82kΩ) The table of connections above gives the equation used to determine a suitable resistor value. A waiting time of nominally 600 µs occurs before the loss of signal is flagged.

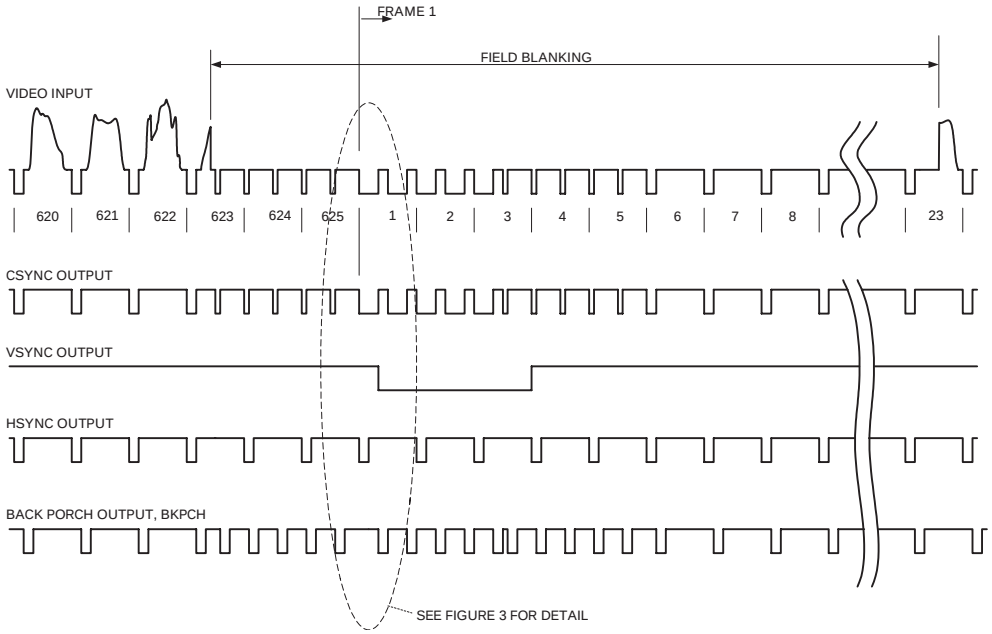


Figure 1: PAL 625 TIMING DIAGRAM

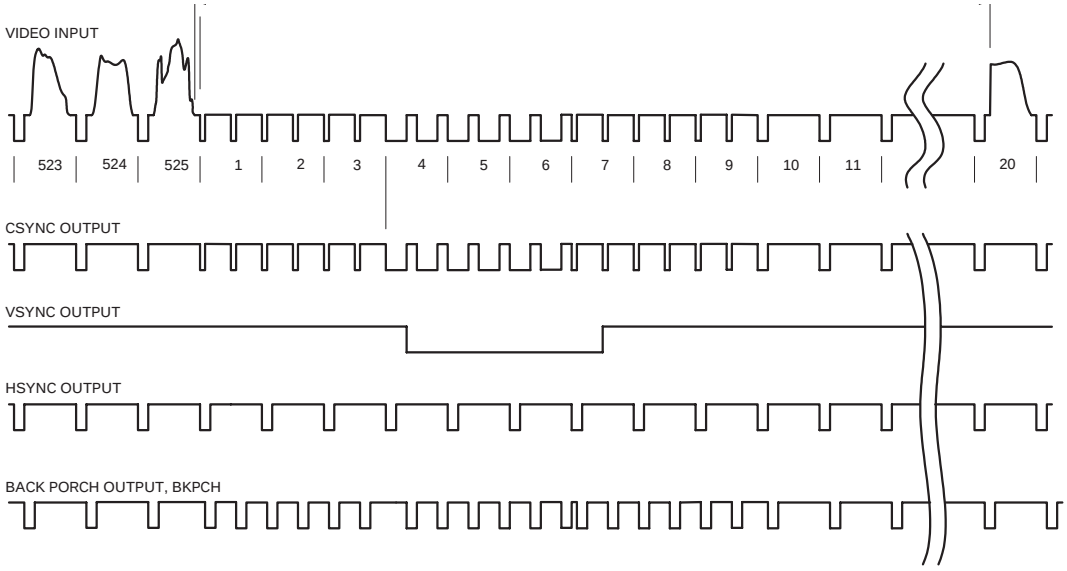


Figure 2: NTSC TIMING DIAGRAM

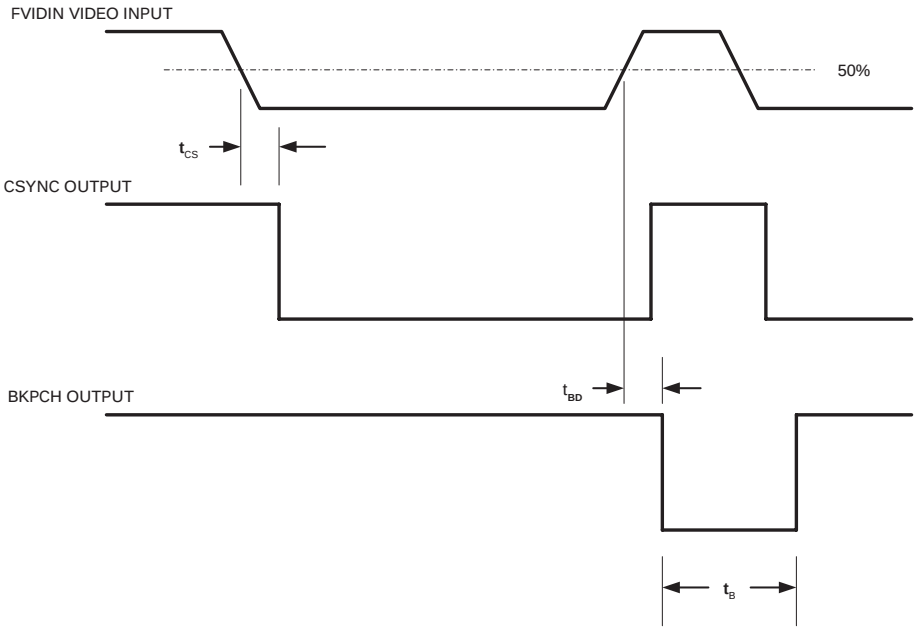


Figure 3: SYNC SLICING & OUTPUT DETAIL

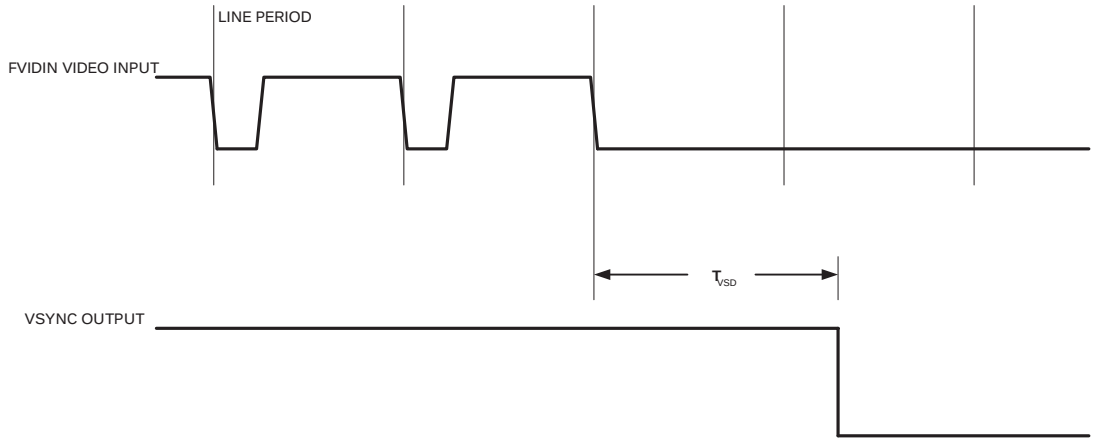
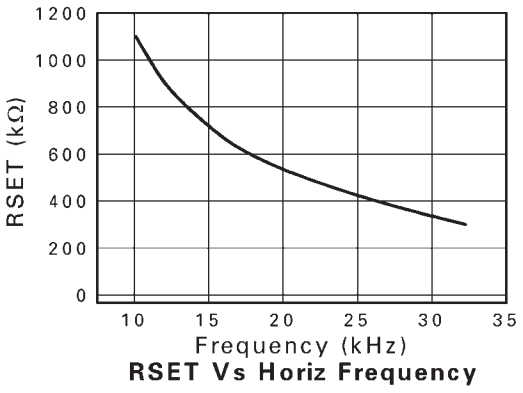
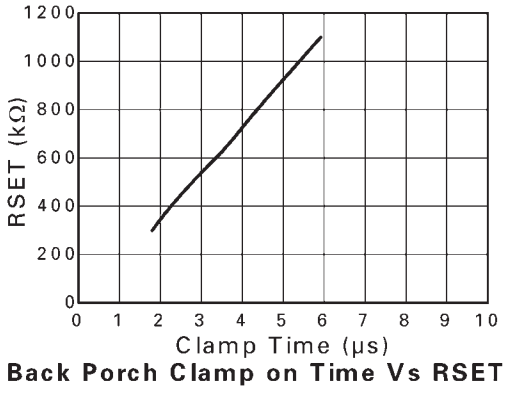


Figure 4: VERTICAL SYNC DEFAULT

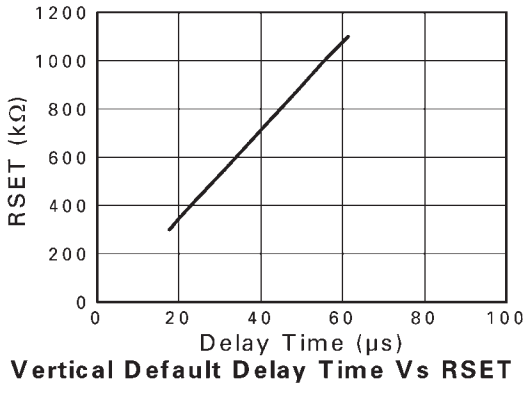
TYPICAL CHARACTERISTICS



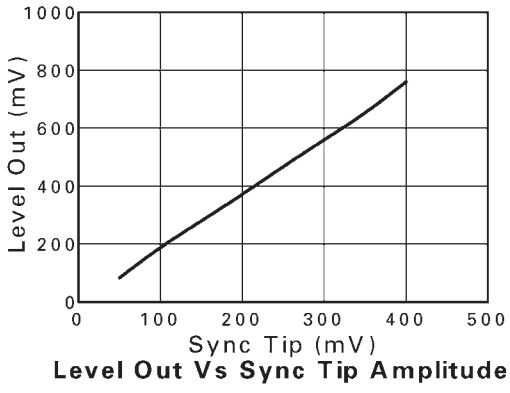
RSET Vs Horiz Frequency



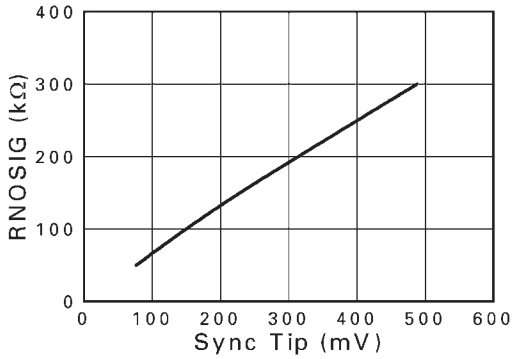
Back Porch Clamp on Time Vs RSET



Vertical Default Delay Time Vs RSET

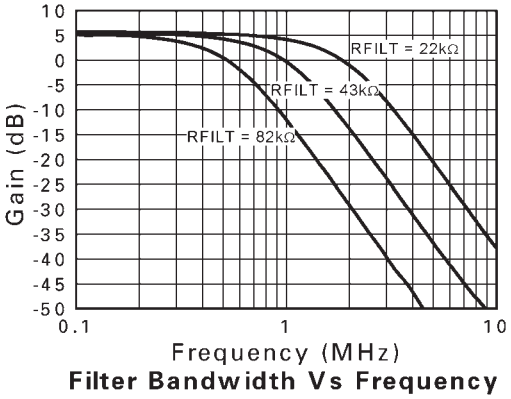


Level Out Vs Sync Tip Amplitude

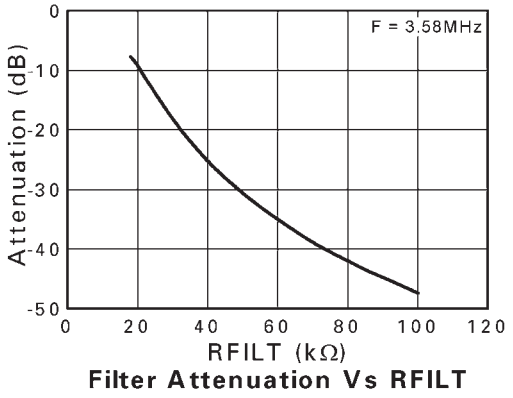


Minimum Signal Detect Vs RNOSIG

TYPICAL CHARACTERISTICS (Cont.)



Filter Bandwidth Vs Frequency



Filter Attenuation Vs RFILT

APPLICATIONS INFORMATION

General guidance

The ZXFV4583 is a high speed mixed analog/digital signal processing component requiring the appropriate care in the layout of the application printed circuit board. A continuous ground plane construction is preferred. Suitable power supply decoupling suggested includes a 100nF leadless ceramic capacitor close to the power supply connection at pin 14.

In order to avoid coupling between high speed logic output signals and analog inputs, the test circuit layout uses connections from the logic output pins routed away from the analog pins. In the application, similar care in the layout is required, keeping resistors, R_{FILT}, R_{NOSIG}, and R_{SET} close to their respective pins, in particular routing signal CSYNC away from pins 1, 2 and 12.

Evaluation circuit

An evaluation circuit is available, designed to provide demonstration of the ZXFV4583 function using 50 Ω test instruments. The schematic diagram is shown in Figure 5 and the printed circuit layout is shown in Figures 6, 7 and 8. The circuit includes the Zetex ZXFV4089 DC Restoration Circuit, which is described in the data sheet for that part. The ZXFV4089 uses the Back Porch output from the ZXFV4583 in order to control and stabilize the black level of a video waveform.

BNC connector sockets allow connection of the analog video and output to laboratory test instruments via 50 Ω BNC cables. The circuit can be adapted for 75 Ω use. The output circuit includes a resistor matching circuit to present a load of 150 Ω to the amplifier and simultaneously provide 50 Ω output impedance. The attenuation of this matching circuit is 15.45 dB. As the amplifier is configured for a voltage gain of 2, the overall gain in a 50 Ω system is:

6 - 15.45 = -9.45 dB.

The synchronized logic outputs are brought to a header for examination using oscilloscope probes. A set of jumper links allow the selection of operation with or without the built in color carrier filter. The selection is depicted on the board itself.

Parts List

QTY	CCTREF	VALUE	DESCRIPTION
Resistors, surface mount			
1	R1	51Ω	0805
1	R2	22kΩ	0805
1	R3	82kΩ	0805
1	R4	681kΩ	0805
2	R5, R12	2.2kΩ	0805
3	R6, R7, R8	1kΩ	0805
1	R9	130Ω	0805
1	R10	33Ω	0805
1	R11	24Ω	0805
Capacitors, surface mount			
5	C1, C2, C3, C5, C6	100nF	ceramic X7R 50V 0805
1	C4	1nF	ceramic NPO 50V 0805
1	C7	10nF	ceramic X7R 50V 0805
2	C8, C9	10μF	tantalum elec 16V size C
Integrated circuits			
1	U1	-	ZXFV4583N16 - Zetex
1	U2	-	ZXFV4089N8 - Zetex
Miscellaneous			
2	J1, J2	-	Socket BNC PCB straight flange e.g. Tyco B35N14H999X99
1	J3	-	Terminal block 3-way IMO 20.501/3SB
1	PL1	-	Header 8 way single row 2.54mm, Harwin M20-9990805
1	PL2	-	Header 8 way double row 2.54mm, Harwin M
3	TP1, TP2, TP3	-	Test terminal, W. Hughes 200-207
2	LK1, LK2	-	Jumper Link, Harwin M7567-05

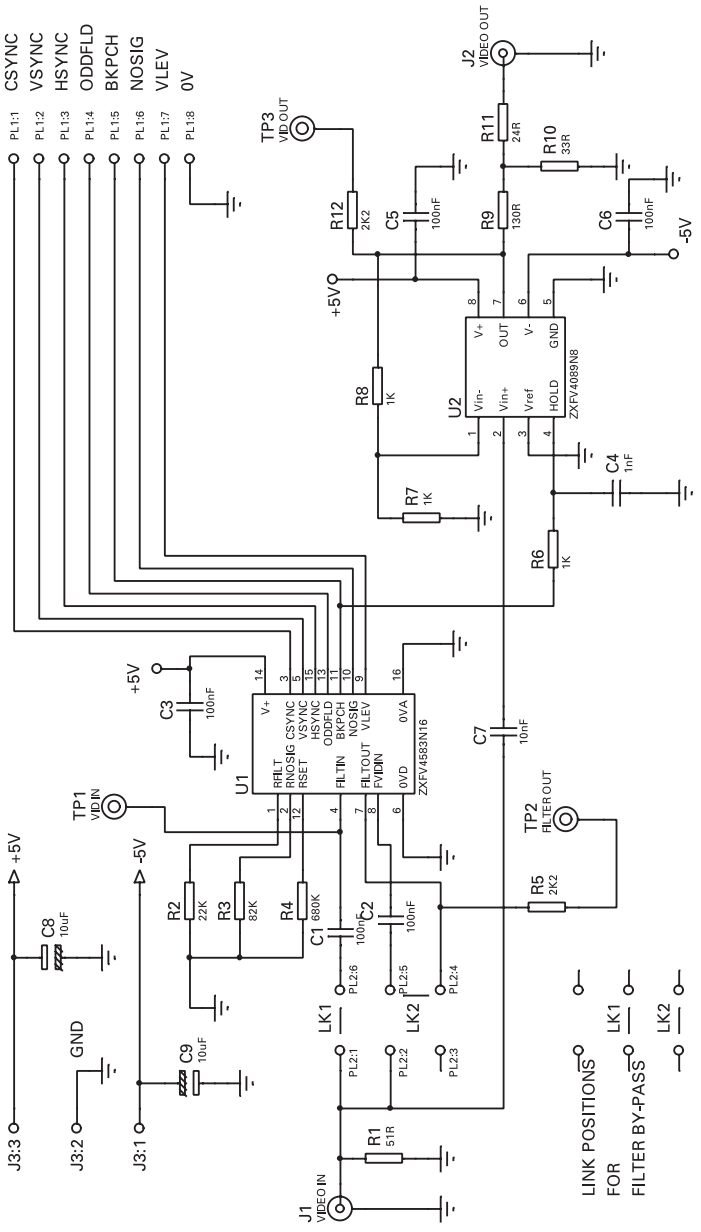


Figure 5: Evaluation circuit board schematic

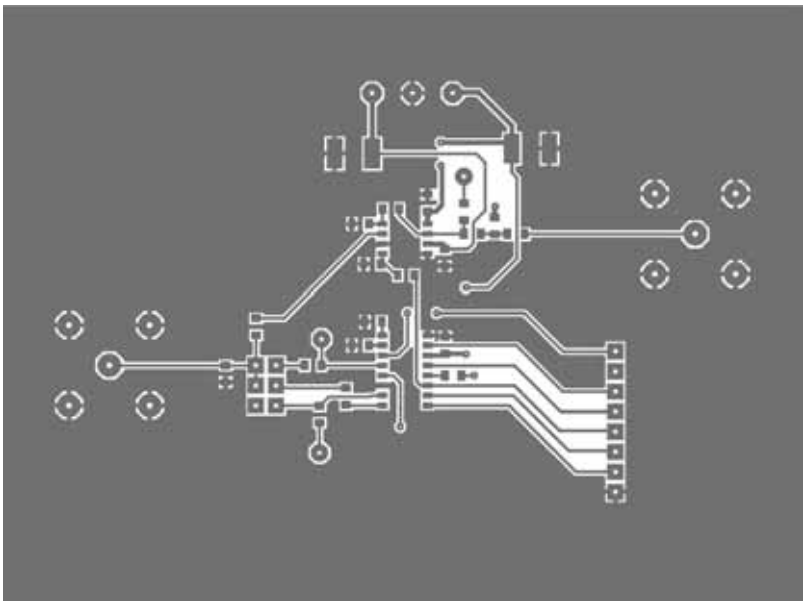


Figure 6: Evaluation circuit layout: Top side

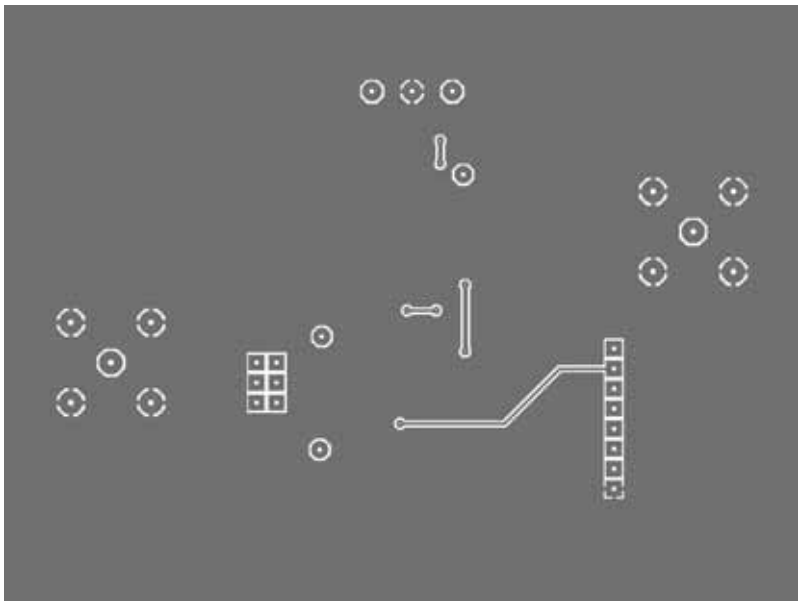


Figure 7: Evaluation circuit layout: Bottom side (viewed through board)

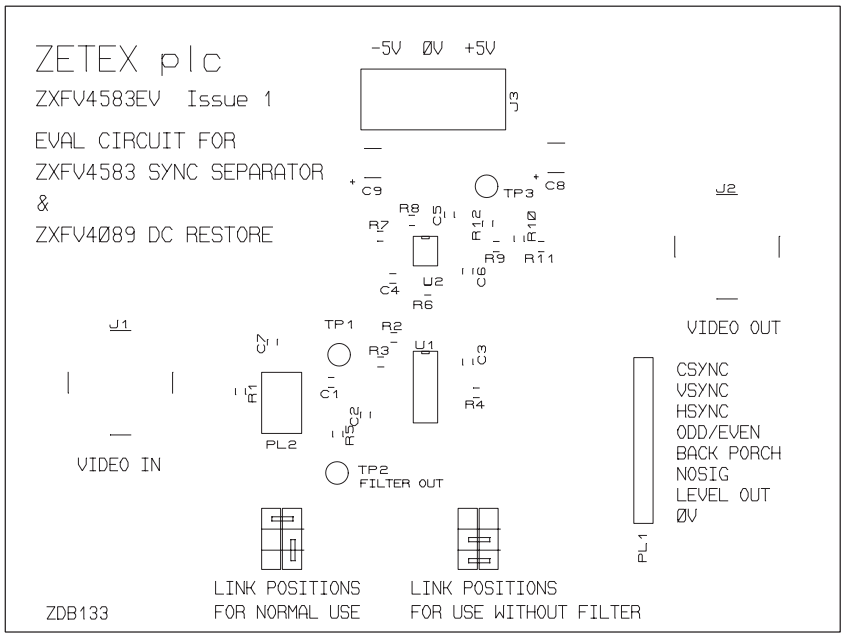
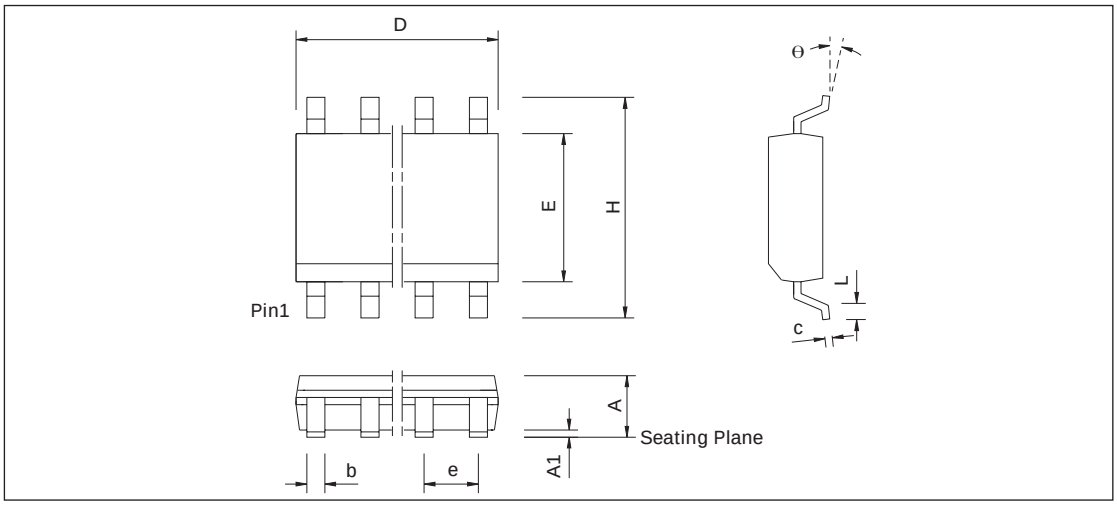


Figure 8: Evaluation circuit layout: Component layout

ZXFV4583

PACKAGE OUTLINE



DIM	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
D	9.80	10.00	0.386	0.394
E	3.80	4.00	0.150	0.157
e	1.27BSC		0.050BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Conforms to JEDEC MS-012AC Iss C (SO16N)

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