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GS4882, GS4982 Video Sync Separators with 50% Sync Slicing

Features

- precision 50% sync slicing
- internal color burst filter
- $\pm 5\text{ns}$ temperature stability
- superior noise immunity
- robust signal detection/output muting circuitry
- high performance dual mode input clamp
- 0.5V to 4.0Vpp input signal with +5V supply
- composite, vertical, back porch, odd/even outputs
- horizontal sync output available with GS4982
- +4.5V to +13.2V supply voltage range
- Pb-free and Green

Description

The GS4882 and GS4982 are precision sync separators for extracting timing information from NTSC, PAL, and SECAM video signals. The GS4882 generates noise immune and temperature stable composite sync, vertical sync, back porch and odd/even field signals. The GS4982 provides a horizontal sync output for those applications requiring horizontal sync extraction.

The GS4882 and GS4982 feature an internal color burst filter for minimization of spurious timing information and the reduction of external component count. The precision 50% sync slicing feature embodied in the device provides

for superior sync extraction in the presence of noise and varying sync pulse amplitudes. The high performance dual mode input clamp aids in maintaining the accuracy of the internally derived 50% sync slicing level to within $\pm 5\%$ as well in reducing system start-up/recovery time. In addition, a missing pulse detector enables the devices to quickly respond to impulse noise by temporarily turning on a Nosync Recovery Current connected to the dual mode input clamp. The input stage will operate with input signal amplitudes ranging from +0.5 to +4.0V peak to peak with a +5V supply voltage.

The GS4882 and GS4982 have robust signal detection and output muting circuitry. Should valid video be removed from the device input, the absence of video will be automatically detected and all outputs muted to a logic high state after a defined probation period. Upon the return of a valid video signal, device outputs are enabled after receiving 8 lines of video. An internal frequency to voltage converter also allows the device to differentiate between valid and invalid input signals by analyzing the horizontal scan rate of the input signal and comparing it against the expected input signal scan rate.

The GS4882 and GS4982 are available in standard 8-pin PDIP and SOIC packages, operate with a +4.5V to +13.2V supply voltage range and typically consume less than 6mA of current with a +5V supply voltage.

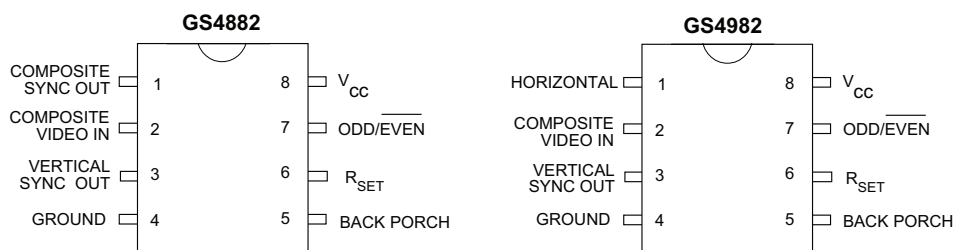


Figure A: Pin Connections

Revision History

Version	Date	Changes and/or Modifications
2	November 2009	Updated to latest Gennum template and changed from document number 52161 to 8505.
1	July 2004	Revisions made.
0	March 1996	New document.

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1. Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1-1 lists the absolute maximum ratings for the GS4882 and GS4982. Conditions exceeding the limits listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage Range	±13.5V
Operating Temperature Range	-0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 Sec)	260°C

1.2 Electrical Characteristics

Table 1-2 shows the electrical characteristics of the GS4882 and GS4982, where conditions are $V_{CC} = 5V$, $R_{SET} = 227k$, $T_A = 25^\circ C$, $C_L = 15pF$, unless otherwise specified.

Table 1-2: Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLIES	Supply Voltage	–	4.5	5.0	13.2	V
	Supply Current	Outputs at Logic 1	–	6	10	mA
VIDEO INPUT	Signal Level	$V_{CC} = 5V$	0.5	–	4.0	V
	Nosync Recovery Current	–	23	30	40	V
	Delay to Nosync Recovery	–	70	–	120	V
	Sync Tip Clamp Voltage	–	–	1.55	–	V
	Source Impedance	–	–	–	200	Ω
	Color Burst Filter	Attenuation at 3.58MHz	12	15	–	dB
	Sync Slice Level	Input Amplitude 0.5 to 2.0Vp-p	45	50	55	%
COMPOSITE SYNC OUTPUT (GS4882)	Delay from Video	$T_A = 25^\circ C$	150	200	250	ns
	Delay from Video	$T_A = 0^\circ C$ to $70^\circ C$	-5	–	+5	ns
	Temperature Stability					
BACK PORCH OUTPUT	Delay	From rising edge of sync	400	525	650	ns
	Pulse Width	–	2.0	2.5	3.2	μs

Table 1-2: Electrical Characteristics (Continued)

	Parameter	Conditions	Min	Typ	Max	Units
VERTICAL SYNC OUTPUT	Pulse Width	Serrations during vertical interval	197.7	197.7	197.7	μ s
HORIZONTAL OUTPUT (GS4982)	Delay from Video	–	340	420	510	ns
	Pulse Width	–	6.0	8.0	10.0	μ s
OUTPUT MUTE	Probation Period	–	1.2	2.5	5	ms
	Lock Time	–	–	8	–	lines
R _{SET} REFERENCE	R _{SET} Reference Voltage	–	1.14	1.24	1.34	V
LOGIC OUTPUTS	V _{OH}	I _{OH} = 40 μ A	4.2	4.6	–	V
		I _{OH} = 1.6mA	2.4	3.4	–	V
	V _{OL}	I _{OL} = -1.6mA	–	0.3	0.6	V

2. Circuit Description

The Block Diagrams for the GS4882 and GS4982 are shown in [Figure 2-6](#) and [Figure 2-7](#), with timing diagrams for the devices shown in [Figure 2-8](#).

When presented with a composite video input signal, the GS4882 outputs composite sync, vertical sync, back porch and odd/even field information. The GS4982 substitutes the composite sync output with a horizontal sync output, for those applications requiring horizontal sync extraction.

An external resistor, R_{SET} , connected to Pin 6 is used to set all timing currents in the device. For standard NTSC applications, R_{SET} should be set to $227k\Omega$. The value of R_{SET} for a standard NTSC application is different for the GS4882/GS4982 line of sync separators ($R_{SET} = 227k\Omega$) than it is for the GS1881/GS4881/GS4981 line of sync separators ($R_{SET} = 680k\Omega$). This change was made to improve jitter performance of the device.

2.1 Composite Video Input (Pin 2)

The GS4882 and GS4982 will operate with input signal amplitudes ranging from 0.5V to 4.0Vp-p. Composite video is AC coupled into the device via an external coupling capacitor connected to Pin 2.

Immediately upon entering the GS4882/GS4982, the video signal is passed to the device's dual mode input clamp in order to clamp the sync tip of the input video waveform to 1.55V. The GS4882/GS4982's dual mode input clamp, with both Hard Clamp and Soft Clamp capabilities, has been specifically designed for use in high performance sync separation. The dual mode input clamp aids in maintaining the accuracy of the internally derived 50% sync slicing level to within $\pm 5\%$ by utilizing the Soft Clamp during steady state operation. The device improves system start-up and impulse noise recovery time by utilizing the device's Hard Clamp and Nosync Recovery Current during initial start-up and when steady state operation has been disturbed by impulse noise.

During the clamping operation, the input video signal is passed through the device's internal color burst filter. The internal filter attenuates the color burst by typically $>15dB$. [Figure 2-1](#) shows the typical frequency response of the internal color burst filter.

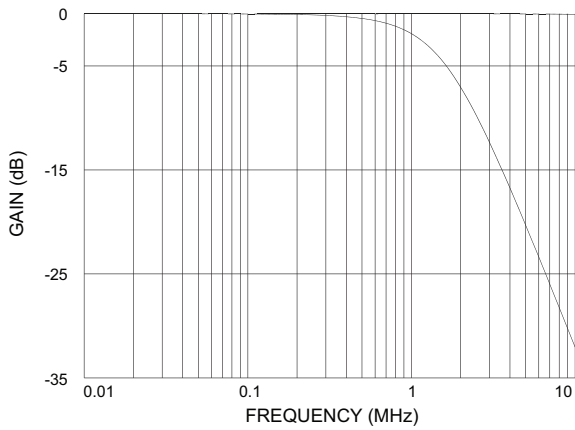


Figure 2-1: Frequency Response of Internal Color Burst Filter

2.2 Composite Sync Output (Pin 1 GS4882)

The filtered video signal is then fed to a comparator which compares it to an internally derived voltage corresponding to the 50% point of the sync pulse amplitude.

By slicing the composite video waveform at 50% of the sync pulse amplitude, variations in output pulse timing due to variations in input signal amplitude are minimized.

Figure 2-2 demonstrates the stability of output pulse timing achieved with 50% sync slicing.

With 50% Sync Slicing no Time Base Errors (TBEs) are introduced due to variations in sync pulse amplitude. Output pulses are always produced at $t_O + t_D$, where t_D represents the delay through the device.

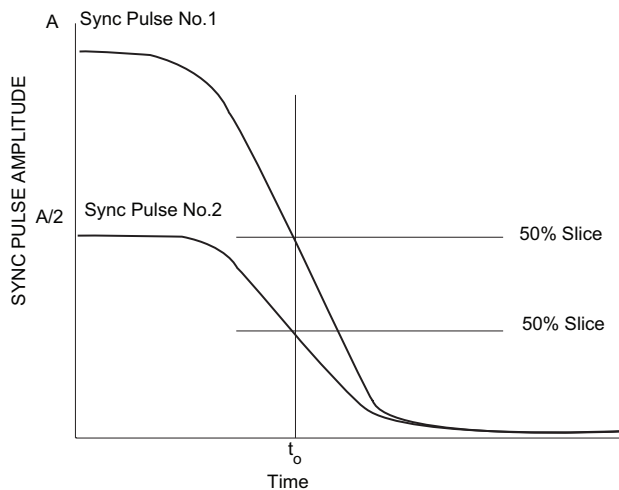


Figure 2-2: Stability of Output Pulse Timing with Variations in Sync Pulse Amplitude

The 50% point of sync is determined by using two identical resistors to divide the voltage between sync tip and back porch. The importance of precision sync tip clamping may be

appreciated here, since the sync tip voltage is used in deriving the 50% slicing level. The back porch voltage is derived through an internal integrate and hold circuit that is gated by the Back Porch output signal. By integrating over the entire back porch period, the accuracy and noise immunity of acquired back porch voltage is greatly improved when compared to systems using simple sample and hold techniques.

The output of the comparator is a reproduction of the input video signal with the active portion of video removed. This represents the composite sync waveform presented on Pin 1 of the GS4882.

The video path and composite sync slicing circuitry have been optimized and compensated to achieve superior temperature stability. Variations in composite sync output timing over the commercial temperature range are less than $\pm 5\text{ns}$.

2.3 Back Porch Output (Pin 5)

In an NTSC composite video signal, horizontal sync pulses are followed by the back porch interval. The GS4882 and GS4982 generate a negative going pulse on Pin 5 during this time. It is delayed typically 525ns from the rising edge of sync and has a typical width of 2.5 μs .

During the pre-equalizing, vertical sync and post equalizing periods, composite sync doubles in frequency. The GS4882 and GS4982 maintain the back porch output at the horizontal rate due to a Back Porch Enable (BPEN) signal, generated by the internal Windowing Circuit, which forces back porch to be output at the horizontal rate.

This gating circuit is also the reason for the excellent impulse noise immunity of the back porch output, as shown in [Figure 2-3](#).

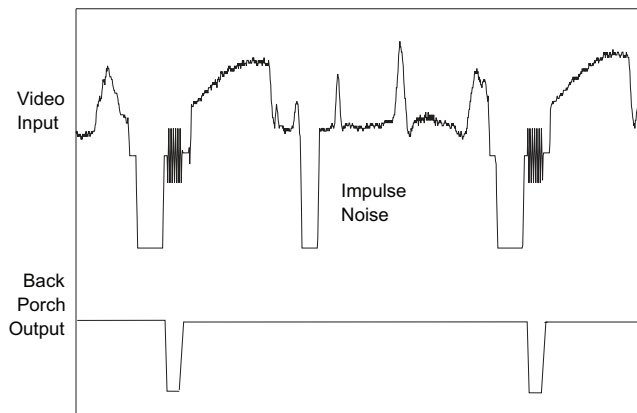


Figure 2-3: Noise Immunity of Back Porch Output

2.4 Vertical Sync Output (Pin 3)

The vertical sync interval is detected by integrating the composite sync pulses. The first broad pulse causes an internal capacitor to charge past a fixed threshold and raises an internal vertical flag. Once the vertical flag is raised, the positive edge of the next serration clocks out the vertical output. When the vertical sync interval ends, the first

post equalizing pulse is unable to charge the capacitor sufficiently, causing the vertical interval flag to go high. The rising edge of the second post-equalizing pulse then clocks out the high flag to end the vertical sync pulse. The vertical output is clocked in and out and therefore is a fixed width. Since the vertical detector is designed as a true integrator, it provides improved noise immunity.

2.5 Odd/Even Output (Pin 7)

NTSC, PAL and SECAM composite video standards are interlaced video schemes and therefore have odd and even fields. For odd fields, the first broad vertical sync pulse is coincident with the start of horizontal, while for even fields, the first broad vertical sync pulse starts in the middle of a horizontal line.

The GS4882 and GS4982 determine odd/even field information by comparing vertical sync with an internally generated horizontal sync. This output is clocked out by the falling edge of vertical sync. The odd/even output is low during even fields and high during odd fields.

This method of determining odd / even field information provides for superior noise immunity. Noise during the preequalizing pulses does not affect the output since the field decision is made at the beginning of the vertical interval. This noise immunity is shown in [Figure 2-4](#), in which an extra preequalizing pulse has been added to the video input with no negative effect on the odd/even field information.

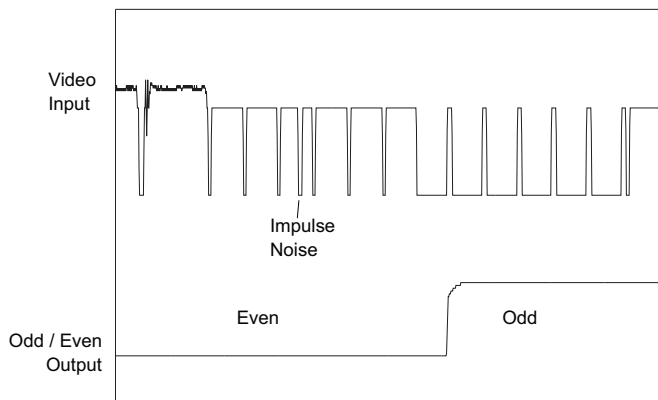


Figure 2-4: Noise Immunity of Odd/Even Output

2.6 Horizontal Output (Pin 1 on GS4982)

As mentioned previously, the odd/even field output of the device is generated by comparing vertical sync with an internal horizontal sync signal. This horizontal sync signal is a true horizontal signal (i.e. maintained during the vertical interval) and is output on Pin 1 of the GS4982. A delay of 420ns and a width of 8.0 μ s are typical for this signal. The internal Windowing Circuit which generates horizontal sync provides excellent impulse noise immunity as shown in [Figure 2-5](#).

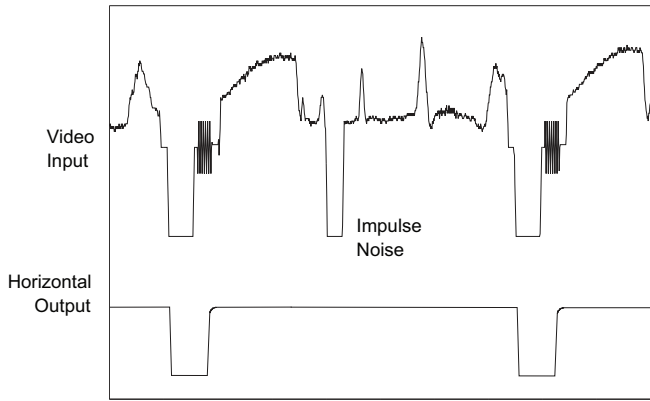


Figure 2-5: Noise Immunity of Horizontal Sync Output

2.7 Signal Detect and Output Mute

Internal to the GS4882 and GS4982 is a robust video signal detection circuit. This circuit provides a reliable control signal that will enable the sync separator outputs only when a valid video signal is present. When the input signal is not valid, the outputs are muted and stay in a logic high state.

The GS4882 and GS4982 differentiate between valid and invalid input signals by feeding the horizontal sync information into a frequency to voltage converter. The horizontal scan rate of the input signal is then compared to an expected input signal horizontal scan rate. With $R_{SET}=227k\Omega$ the sync separator will typically define a valid input signal as one with a horizontal frequency of $15.7 \pm 4kHz$.

Assuming that the sync separator is in steady state operation with a valid input signal, all outputs will be enabled. Removal of the input signal, or a significant change in the input signal frequency, will cause an internal probation timer to be triggered.

While on probation, the sync separator outputs remain enabled and separated sync is still produced. If a valid input signal is not returned to the system before the probation time expires (typically 2.5ms), all outputs will be muted to logic high state. Should a valid signal return during the probation period, and eight lines be received before the probation time expires, device outputs will remain enabled. Once device outputs are muted, the device must receive 8 valid lines of video at the correct horizontal frequency before the outputs are re-enabled.

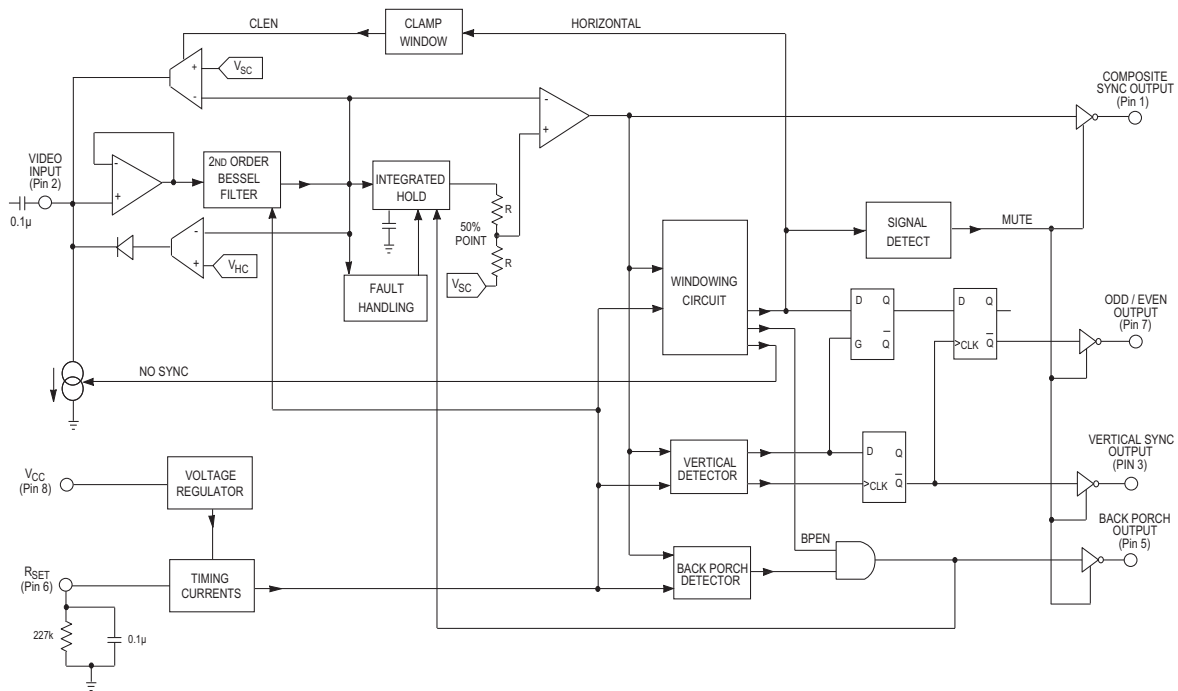


Figure 2-6: GS4882 Block Diagram

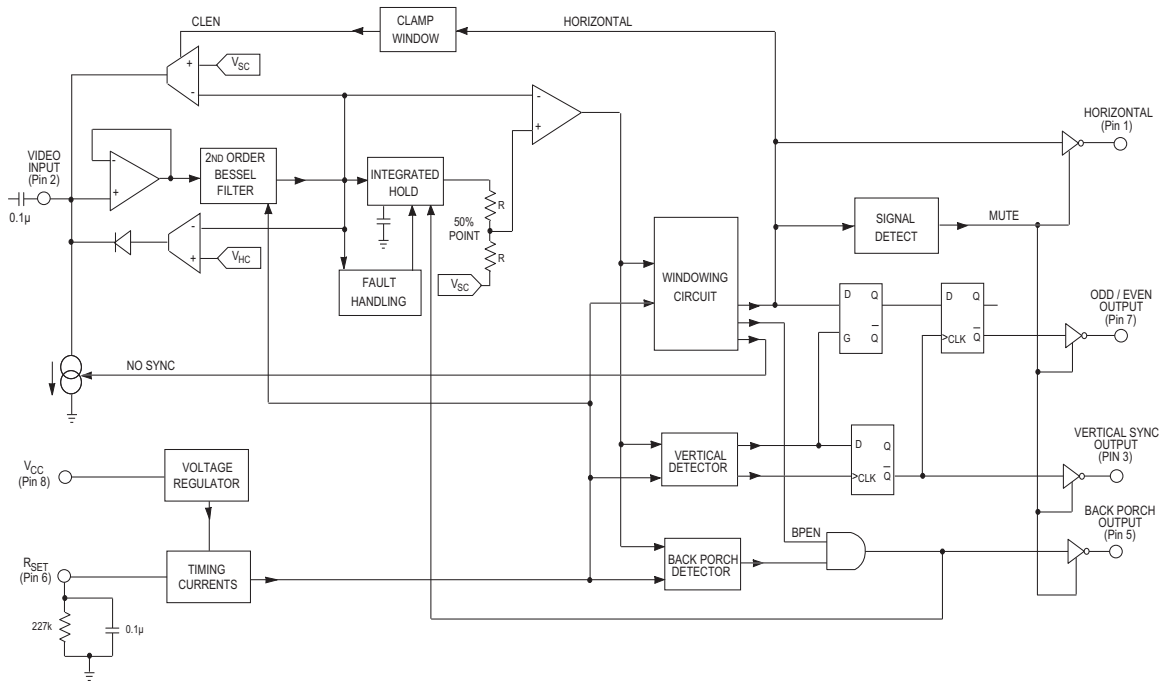


Figure 2-7: GS4982 Block Diagram

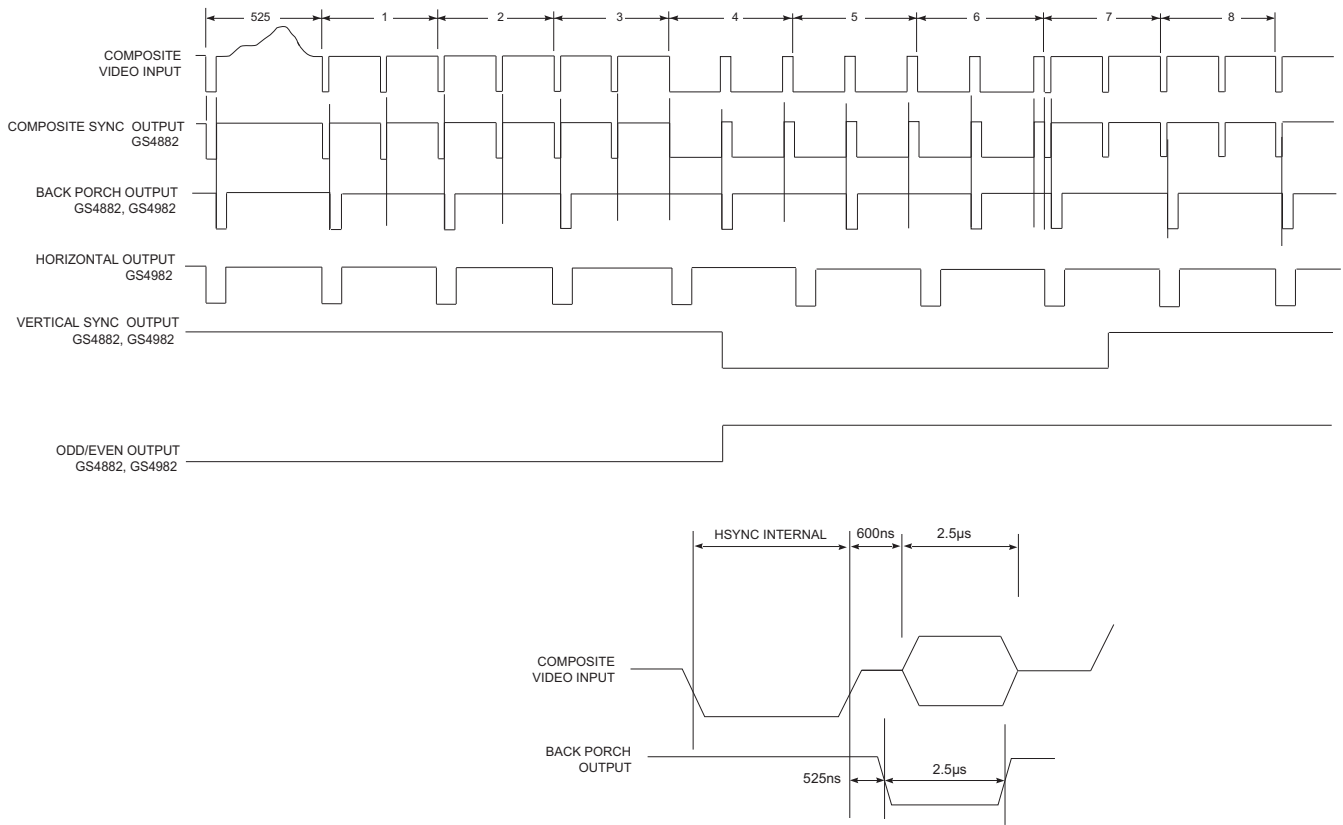
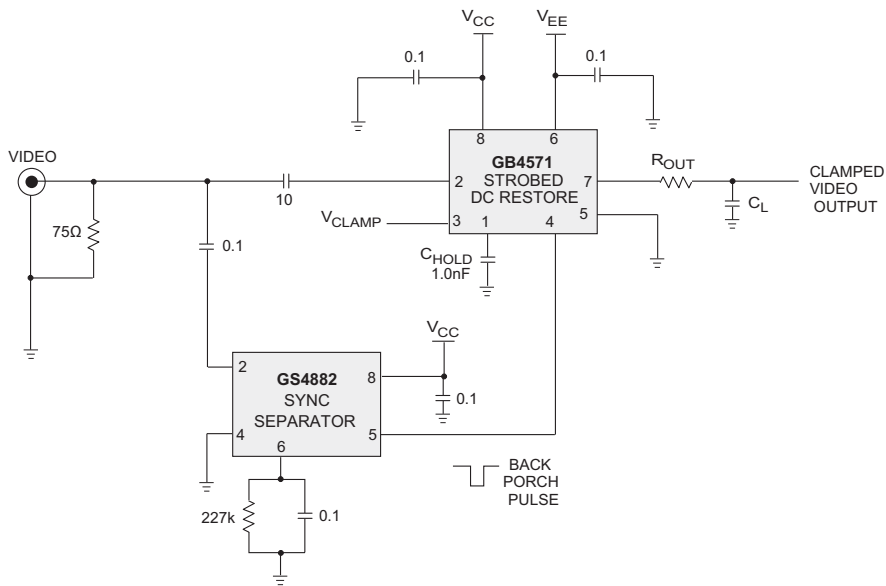


Figure 2-8: GS4882, GS4982 Video Sync Separator Timing Diagram



NOTE: All resistors in ohms, all capacitors in microfarads, unless otherwise stated.

Figure 2-9: Typical NTSC Application Diagram

3. Ordering Information

Table 3-1: GS4882 Ordering Information

Part Number	Package	Temperature Range	Pb-Free and Green
GS4882-CDA	8-Pin PDIP	0°C to 70°C	No
GS4882-CKA	8-Pin SOIC	0°C to 70°C	No
GS4882-CTA	8-Pin SOIC Tape	0°C to 70°C	No
GS4882-CKAE3	8-Pin SOIC	0°C to 70°C	Yes

Table 3-2: GS4982 Ordering Information

Part Number	Package	Temperature Range	Pb-Free and Green
GS4982-CDA	8-Pin PDIP	0°C to 70°C	No
GS4982-CKA	8-Pin SOIC	0°C to 70°C	No
GS4982-CTA	8-Pin SOIC Tape	0°C to 70°C	No
GS4982-CKAE3	8-Pin SOIC	0°C to 70°C	Yes

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