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TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC74LVX4245FS

## OCTAL DUAL SUPPLY BUS TRANSCEIVER

The TC74LVX4245 is a dual supply, advanced high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate CMOS technology.

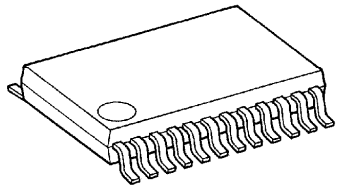
Designed for use as an interface between a 5V bus and a 3.3V bus in mixed 5V / 3.3V supply systems' it achieves high speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{OE}$) can be used to disable the device so that the buses are effectively isolated.

The A-port interfaces with the 5V bus, the B-port with the 3.3V bus.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



SSOP24-P-300-0.65A

Weight : 0.14g (Typ.)

### FEATURES

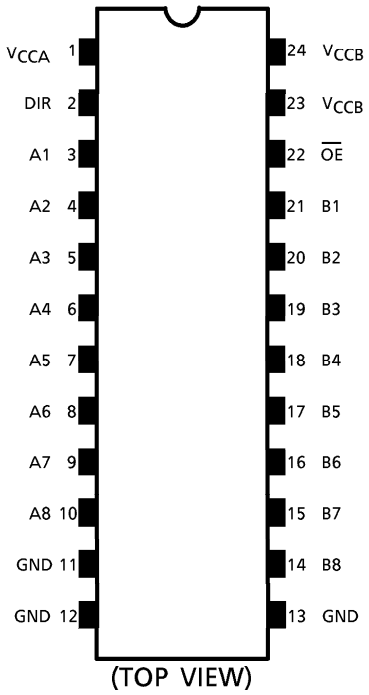
- Bidirectional interface between 5V and 3V buses
- High speed : $t_{pd}$ = 6.0ns (Typ.) ($V_{CCA}$ = 5.0V / $V_{CCB}$ = 3.3V)
- Low power dissipation : $I_{CC}$ = 8$\mu$A (Max.) (Ta = 25°C)
- Symmetrical output impedance : $I_{OUTA}$ = ± 24mA (Min.) $I_{OUTB}$ = ± 12mA (Min.) ($V_{CCA}$ = 4.5V / $V_{CCB}$ = 3.0V)
- Low noise : $V_{OLP}$ = 1.5V (Max.)
- Available in SSOP package

### APPLICATION NOTES

Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

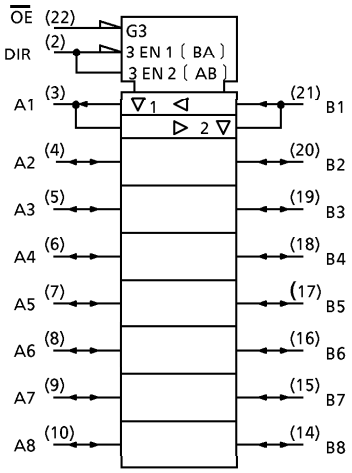
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

## PIN ASSIGNMENT



(TOP VIEW)

## IEC LOGIC SYMBOL



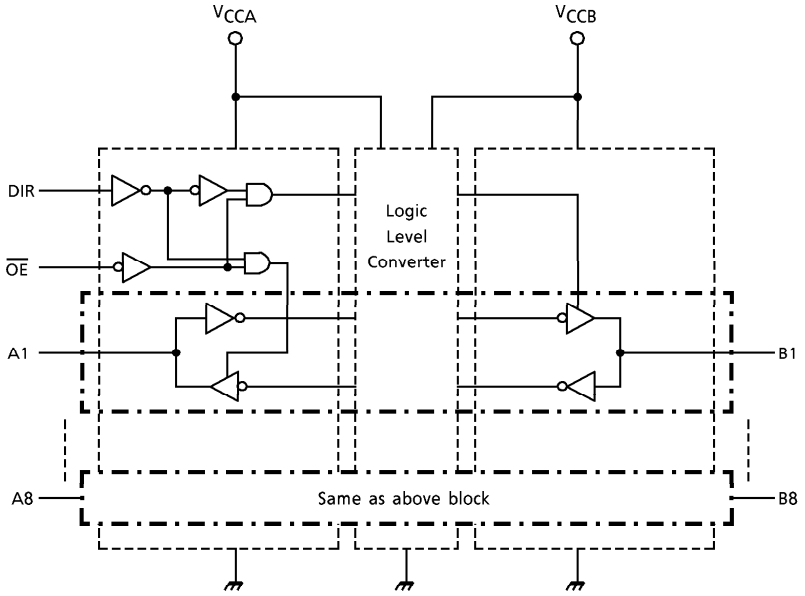

## TRUTH TABLE

| INPUTS | | OUTPUTS | FUNCTION | |
|---|---|---|---|---|
| $\overline{G}$ | DIR | | A-BUS | B-BUS |
| L | L | A = B | OUTPUT | INPUT |
| L | H | B = A | INPUT | OUTPUT |
| H | X | Z | High Impedance | |

X : Don't Care

Z : High Impedance

**BLOCK DIAGRAM**




**MAXIMUM RATINGS**

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage Range* | $V_{CCA}$ | −0.5~7.0 | V |
| | $V_{CCB}$ | −0.5~$V_{CCA}$ | |
| DC Input Voltage ($\overline{OE}$,DIR) | $V_{IN}$ | −0.5~$V_{CCA}$ + 0.5 | V |
| DC Bus I/O Voltage | $V_{I/OA}$ | −0.5~$V_{CCA}$ + 0.5 | V |
| | $V_{I/OB}$ | −0.5~$V_{CCB}$ + 0.5 | |
| Input Diode Current | $I_{IK}$ | −20 | mA |
| Output Diode Current | $I_{OK}$ | ±50 | mA |
| DC Output Current | $I_{OUTA}$ | ±50 | mA |
| | $I_{OUTB}$ | ±50 | |
| DC $V_{CC}$/Ground Current | $I_{CCA}$ | ±200 | mA |
| | $I_{CCB}$ | ±100 | |
| Power Dissipation | $P_D$ | 180 | mW |
| Storage Temperature | $T_{stg}$ | −65~150 | °C |

* : $V_{CCA} > V_{CCB}$, Don't use under the condition that $V_{CCB}$ is 0V.

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CCA}$ | 4.5~5.5 | V |
| | $V_{CCB}$ | 2.7~3.6 | |
| Input Voltage ($\overline{OE}$,DIR) | $V_{IN}$ | 0~$V_{CCA}$ | V |
| Bus I/O Voltage | $V_{I/OA}$ | 0~$V_{CCA}$ | V |
| | $V_{I/OB}$ | 0~$V_{CCB}$ | |
| Operating Temperature | $T_{opr}$ | −40~85 | °C |
| Input Rise And Fall Time | dt/dv | 0~8 ($V_{CCA}$ = 4.5~5.5V) | ns/V |
| | | 0~8 ($V_{CCB}$ = 2.7~3.6V) | |

**ELECTRICAL CHARACTERISTICS**

DC characteristics ($V_{CCA}$) $V_{CCB}$ = 2.7~3.6V

| PARAMETER | | SYM-BOL | TEST CONDITION | | $V_{CCA}$ (V) | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Input Voltage | "H" Level | $V_{IHA}$ | DIR, $\overline{G}$, An | | 4.5 ~ 5.5 | 2.0 | — | — | 2.0 | — | V |
| | "L" Level | $V_{ILA}$ | DIR, $\overline{G}$, An | | 4.5 ~ 5.5 | — | — | 0.8 | — | 0.8 | |
| Output Voltage | "H" Level | $V_{OHA}$ | $V_{INA}$ = $V_{IHA}$ or $V_{ILA}$ $V_{INB}$ = $V_{IHB}$ or $V_{ILB}$ | $I_{OH}$ = −100μA | 4.5 | 4.4 | 4.5 | — | 4.4 | — | V |
| | | | | $I_{OH}$ = −24mA | 4.5 | 3.86 | — | — | 3.76 | — | |
| | "L" Level | $V_{OLA}$ | $V_{INA}$ = $V_{IHA}$ or $V_{ILA}$ $V_{INB}$ = $V_{IHB}$ or $V_{ILB}$ | $I_{OL}$ = 100μA | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | $I_{OL}$ = 24mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| 3-State Output Off-State Current | | $I_{OZA}$ | $V_{INA}$ = $V_{IHA}$ or $V_{ILA}$ $V_{INB}$ = $V_{IHB}$ or $V_{ILB}$ $V_{I/OA}$ = $V_{CCA}$ or GND | | 5.5 | — | — | ±0.5 | — | ±5.0 | μA |
| Input Leakage Current | | $I_{INA}$ | $V_{IN}$ (DIR, $\overline{G}$) = $V_{CCA}$ or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent Supply Current | | $I_{CCA}$ | $V_{INA}$ = $V_{CCA}$ or GND $V_{INB}$ = $V_{CCB}$ or GND | | 5.5 | — | — | 8.0 | — | 80.0 | μA |
| | | $I_{CCTA}$ | PER INPUT : $V_{INA}$ = 3.4V OTHER INPUT : $V_{CCA}$ or GND | | 5.5 | — | — | 2.3 | — | 2.5 | mA |

DC characteristics ($V_{CCB}$) $V_{CCA}$ = 4.5~5.5V

| PARAMETER | | SYM-BOL | TEST CONDITION | | $V_{CCB}$ (V) | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Input Voltage | "H" Level | $V_{IHB}$ | Bn | | 2.7 | 2.0 | — | — | 2.0 | — | V |
| | | | | | 3.6 | 2.2 | — | — | 2.2 | — | |
| | "L" Level | $V_{ILB}$ | Bn | | 2.7 | — | — | 0.8 | — | 0.8 | |
| | | | | | 3.6 | — | — | 0.8 | — | 0.8 | |
| Output Voltage | "H" Level | $V_{OHB}$ | $V_{INA}$ = $V_{IHA}$ or $V_{ILA}$ | $I_{OH}$ = −100μA | 3.0 | 2.9 | 3.0 | — | 2.9 | — | V |
| | | | | $I_{OH}$ = −8mA | 2.7 | 2.26 | — | — | 2.20 | — | |
| | | | | $I_{OH}$ = −12mA | 3.0 | 2.48 | — | — | 2.40 | — | |
| | "L" Level | $V_{OLB}$ | $V_{INA}$ = $V_{IHA}$ or $V_{ILA}$ | $I_{OL}$ = 100μA | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | $I_{OL}$ = 8mA | 2.7 | — | — | 0.31 | — | 0.40 | |
| | | | | $I_{OL}$ = 12mA | 3.0 | — | — | 0.31 | — | 0.40 | |
| 3-State Output Off-State Current | | $I_{OZB}$ | $V_{INA}$ = $V_{IHA}$ or $V_{ILA}$<br>$V_{I/OB}$ = $V_{CCB}$ or GND | | 3.6 | — | — | ±0.5 | — | ±5.0 | μA |
| Quiescent Supply Current | | $I_{CCB}$ | $V_{INA}$ = $V_{CCA}$ or GND<br>$V_{INB}$ = $V_{CCB}$ or GND | | 3.6 | — | — | 5.0 | — | 50.0 | μA |
| | | $I_{CCTB}$ | PER INPUT : $V_{INB}$ = 3.0V<br>OTHER INPUT : $V_{CCB}$ or GND | | 3.6 | — | — | 0.35 | — | 0.50 | mA |

AC characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$, $V_{CCA} = 5.0 \pm 0.5V$)

| PARAMETER | SYMBOL | TEST CONDITION | | Ta = 25°C | | | Ta = −40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCB}$ (V) | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Propagation Delay Time (An⇒Bn) | $t_{pLH}$ $t_{pHL}$ | Input : An Output : Bn (DIR = "H") | 2.7 | — | 7.1 | 9.5 | 1.0 | 10.5 | ns |
| | | | 3.3 ± 0.3 | — | 6.5 | 8.6 | 1.0 | 9.5 | |
| 3-State Output Enable Time ($\overline{G}$⇒Bn) | $t_{pZL}$ $t_{pZH}$ | | 2.7 | — | 9.5 | 12.5 | 1.0 | 13.8 | ns |
| | | | 3.3 ± 0.3 | — | 8.6 | 11.4 | 1.0 | 12.5 | |
| 3-State Output Disable Time ($\overline{G}$⇒Bn) | $t_{pLZ}$ $t_{pHZ}$ | | 2.7 | — | 5.3 | 9.1 | 1.0 | 10.0 | ns |
| | | | 3.3 ± 0.3 | — | 5.3 | 9.1 | 1.0 | 10.0 | |
| Propagation Delay Time (Bn⇒An) | $t_{pLH}$ $t_{pHL}$ | Input : Bn Output : An (DIR = "L") | 2.7 | — | 7.0 | 9.5 | 1.0 | 10.5 | ns |
| | | | 3.3 ± 0.3 | — | 6.4 | 8.6 | 1.0 | 9.5 | |
| 3-State Output Enable Time ($\overline{G}$⇒An) | $t_{pZL}$ $t_{pZH}$ | | 2.7 | — | 8.5 | 11.6 | 1.0 | 12.7 | ns |
| | | | 3.3 ± 0.3 | — | 7.7 | 10.5 | 1.0 | 11.5 | |
| 3-State Output Disable Time ($\overline{G}$⇒An) | $t_{pLZ}$ $t_{pHZ}$ | | 2.7 | — | 5.1 | 6.8 | 1.0 | 7.5 | ns |
| | | | 3.3 ± 0.3 | — | 5.1 | 6.8 | 1.0 | 7.5 | |
| Output To Output Skew | $t_{osLH}$ $t_{osHL}$ | (Note 1) | 2.7 | — | — | 1.5 | — | 1.5 | ns |
| | | | 3.3 ± 0.3 | — | — | 1.5 | — | 1.5 | |
| Input Capacitance | $C_{INA}$ | DIR, $\overline{G}$ | 3.3 ± 0.3 | — | 5 | 10 | — | 10 | pF |
| Bus Input Capacitance | $C_{I/O}$ | An, Bn | 3.3 ± 0.3 | — | 13 | — | — | — | pF |
| Power Dissipation Capacitance (Note 2) | $C_{PDA}$ | A⇒B (DIR = "H") | 3.3 ± 0.3 | — | 17 | — | — | — | pF |
| | | B⇒A (DIR = "L") | 3.3 ± 0.3 | — | 25 | — | — | — | |
| | $C_{PDB}$ | A⇒B (DIR = "H") | 3.3 ± 0.3 | — | 4 | — | — | — | |
| | | B⇒A (DIR = "L") | 3.3 ± 0.3 | — | 4 | — | — | — | |

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

(Note 2) $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

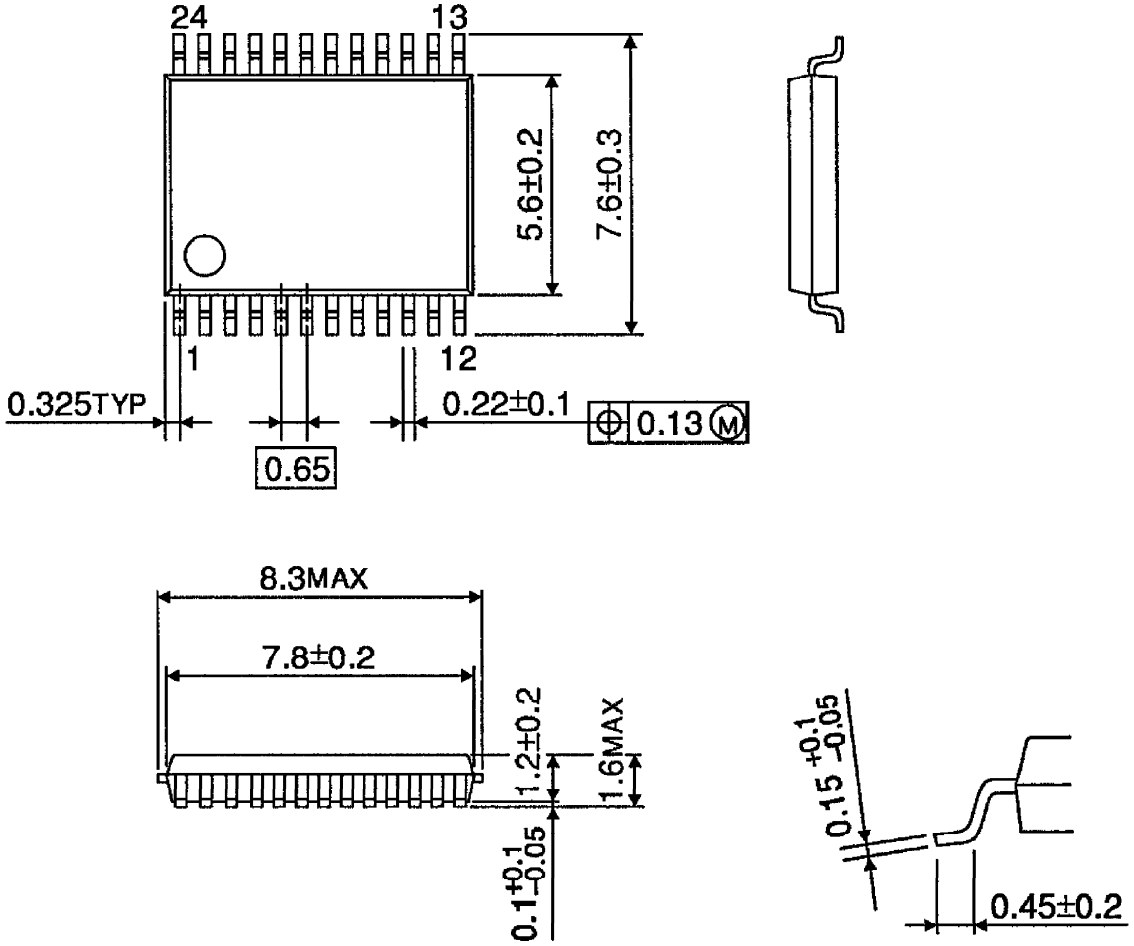
Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

| PARAMETER | SYMBOL | TEST CONDITION | $V_{CCA}$ (V) | $V_{CCB}$ (V) | TYP. | LIMIT | UNIT |
|---|---|---|---|---|---|---|---|
| Quiet Output Maximum Dynamic $V_{OL}$ (A) | $V_{OLPA}$ | Input : Bn Output : An (DIR = "L") | 5.0 | 3.3 | 1.0 | 1.5 | V |
| Quiet Output Mimimum Dynamic $V_{OL}$ (A) | $V_{OLVA}$ | | 5.0 | 3.3 | − 0.6 | − 1.2 | V |
| Quiet Output Maximum Dynamic $V_{OL}$ (B) | $V_{OLPB}$ | Input : An Output : Bn (DIR = "H") | 5.0 | 3.3 | 0.8 | 1.2 | V |
| Quiet Output Mimimum Dynamic $V_{OL}$ (B) | $V_{OLVB}$ | | 5.0 | 3.3 | − 0.5 | − 0.8 | V |
| Minimum High Level Dynamic Input Voltage | $V_{IHDA}$ | Input : An | 5.0 | 3.3 | — | 2.0 | V |
| Maximum Low Level Dynamic Input Voltage | $V_{ILDA}$ | Input : An | 5.0 | 3.3 | — | 0.8 | V |
| Minimum High Level Dynamic Input Voltage | $V_{IHDB}$ | Input : Bn | 5.0 | 3.3 | — | 2.0 | V |
| Maximum Low Level Dynamic Input Voltage | $V_{ILDB}$ | Input : Bn | 5.0 | 3.3 | — | 0.8 | V |

**OUTLINE DRAWING**

SSOP24-P-300-0.65A

Unit : mm







Weight : 0.14g (Typ.)