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FAIRCHILD SEMICONDUCTOR™

April 1988
Revised September 2000

74F174
Hex D-Type Flip-Flop with Master Reset

General Description

The 74F174 is a high-speed hex D-type flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

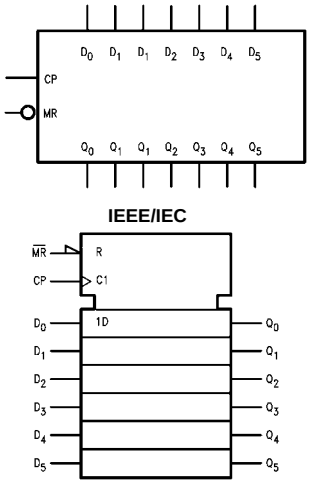
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- Guaranteed 4000V minimum ESD protection

Ordering Code:

Order Number	Package Number	Package Description
74F174SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F174PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

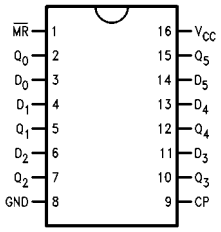
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



IEEE/IEC

Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_5	Data Inputs	1.0/1.0	20 μA/–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/–0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA
Q_0–Q_5	Outputs	50/33.3	–1 mA/20 mA

Functional Description

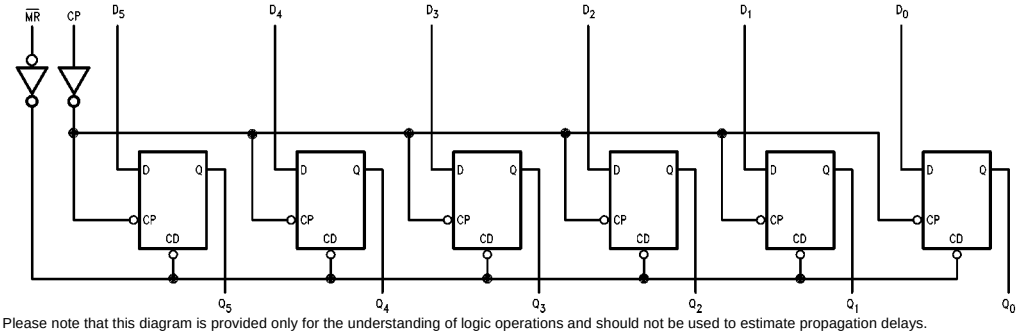
The 74F174 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 74F174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Outputs
$\overline{MR}$	CP	D_n	Q_n
L	X	X	L
H	⌐	H	H
H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		10% V_{CC}			0.5			I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			30	45	mA	Max	CP = ⌐ D_n = $\overline{MR}$ = HIGH
I_{CCL}	Power Supply Current			30	45	mA	Max	V_O = LOW

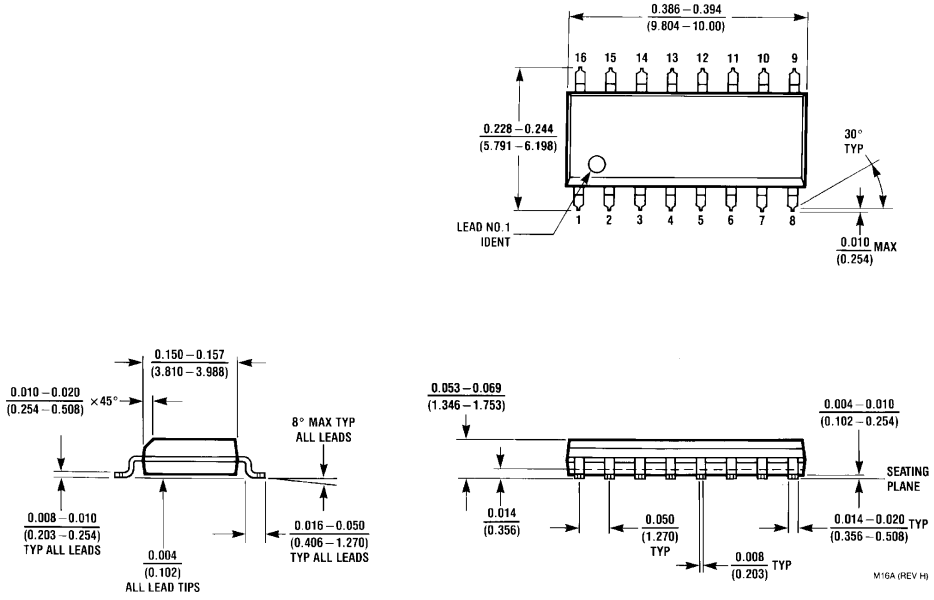
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	80			70		80		MHz
t_{PLH}	Propagation Delay	3.5	5.5	8.0	3.0	10.0	3.5	9.0	ns
t_{PHL}	CP to Q_n	4.0	7.0	10.0	4.0	12.0	4.0	11.0	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	10.0	14.0	5.0	16.0	5.0	15.0	ns

AC Operating Requirements

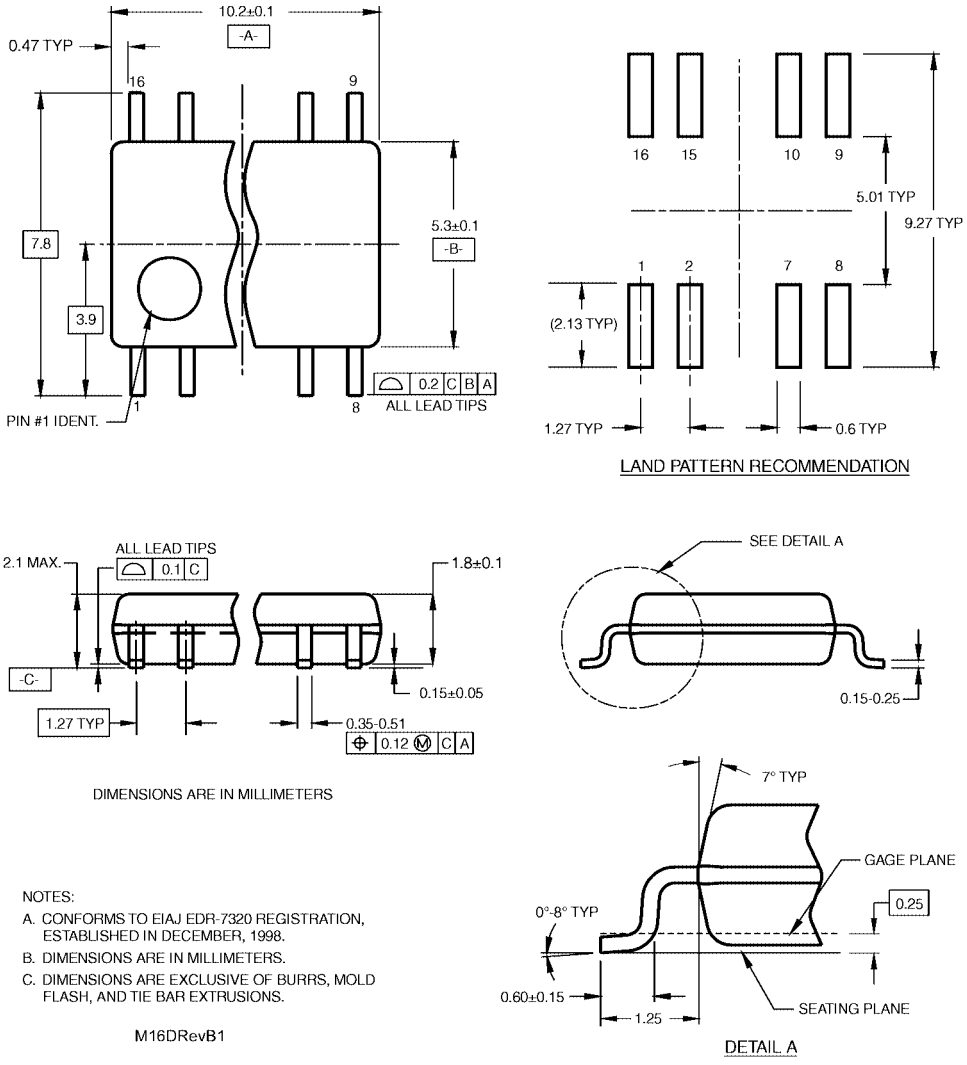
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.8		5.0		4.8		ns
$t_S(L)$	D_n to CP	4.0		5.0		4.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		2.0		0		
$t_H(L)$	D_n to CP	0		2.0		0		
$t_W(H)$	CP Pulse Width	4.0		5.0		4.0		ns
$t_W(L)$	HIGH or LOW	6.0		7.5		6.0		
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		6.5		5.0		ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP	5.0		6.0		5.0		

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

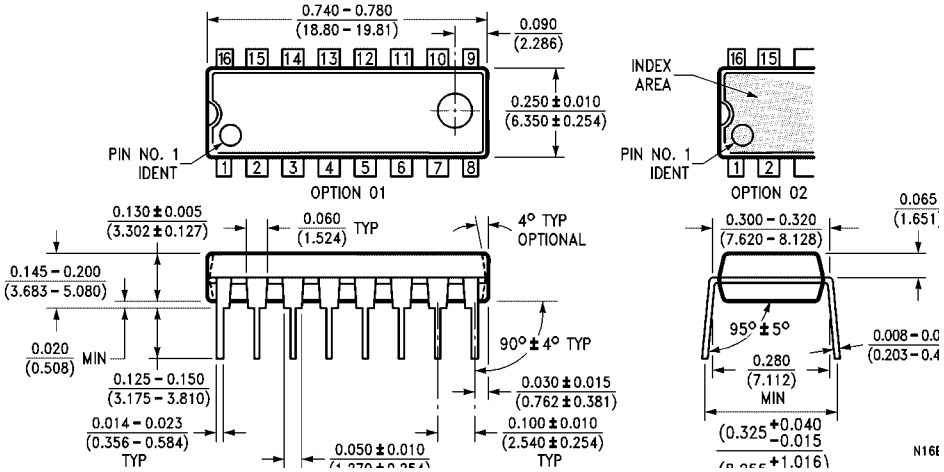
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E