

阅读申明

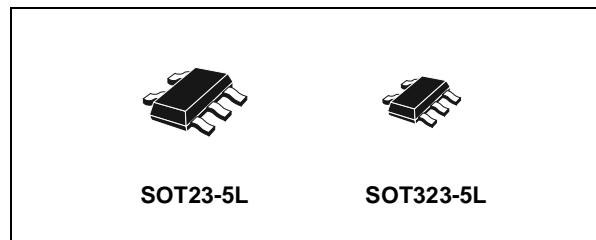
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SINGLE D-TYPE LATCH

- HIGH SPEED: $t_{PD} = 4.4ns$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 1\mu A$ (MAX.) at $T_A=25^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8mA$ (MIN) at $V_{CC} = 4.5V$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $5.5V$
- IMPROVED LATCH-UP IMMUNITY



ORDER CODES

PACKAGE	T & R
SOT23-5L	74V1G77STR
SOT323-5L	74V1G77CTR

DESCRIPTION

The 74V1G77 is an advanced high-speed CMOS SINGLE D-TYPE LATCH fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is designed to operate from 2V to 5.5V, making this device ideal for portable applications.

The single D-Type latch is controlled by a Latch Enable Input (LE).

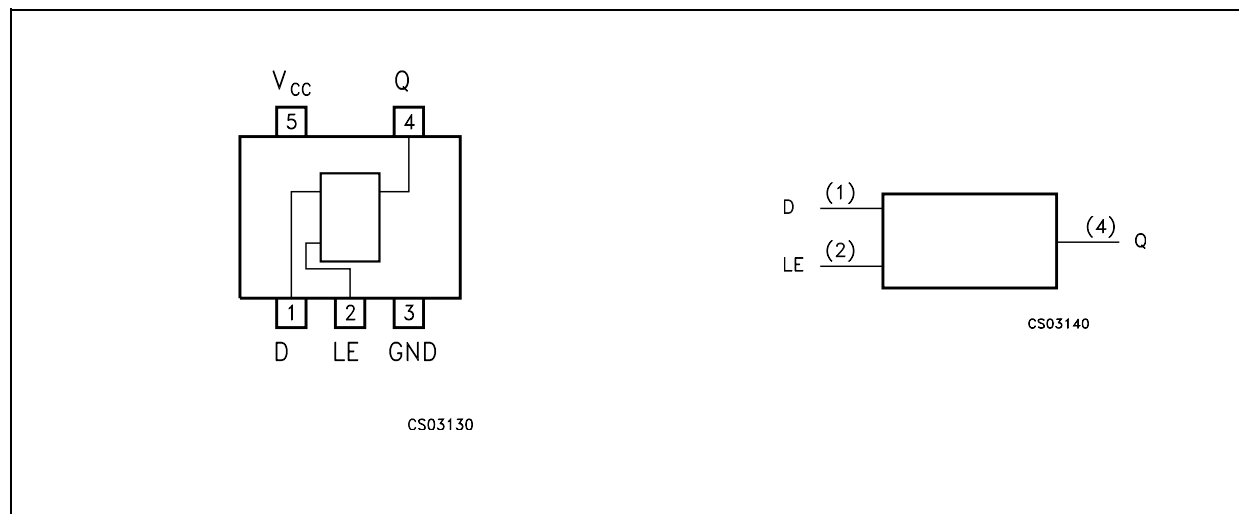
While the LE input is held at a high level, the Q output will follow the data input precisely. When

the LE input is taken low the Q output is latched precisely at the logic level of D input data.

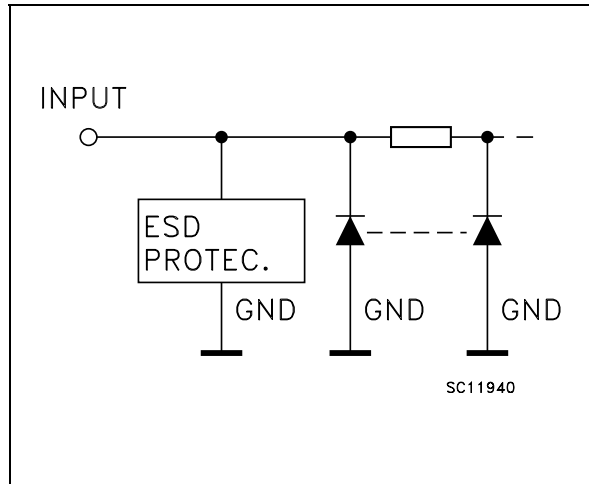
Power down protection is provided on inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V. It's available in the commercial and extended temperature range.

All inputs and output are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN N°	SYMBOL	NAME QND FUNCTION
1	D	Data Input
2	LE	Latch Enable Input
4	Q	Data Output
3	GND	Ground (0V)
5	V _{CC}	Positive Supply Voltage

TRUTH TABLE

D	LE	Q
L	L	No Change *
H	L	No Change *
L	H	Q _n
H	H	Q _n

(*) Q output is latched at the time when the le input is taken low logic level.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	260	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 5.5	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1) (V _{CC} = 3.3 ± 0.3V) (V _{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		0.7V _{CC}		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		0.3V _{CC}	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			1		10		20	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)	C _L (pF)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time LE to Q	3.3 ^(*)	15		6.2	9.0	1.0	10.5	1.0	11.5	ns
		3.3 ^(*)	50		6.8	10.0	1.0	11.5	1.0	13.0	
		5.0 ^(**)	15		4.4	6.5	1.0	7.5	1.0	8.5	
		5.0 ^(**)	50		4.8	7.0	1.0	8.0	1.0	9.0	
t _{PLH} t _{PHL}	Propagation Delay Time D to Q	3.3 ^(*)	15		7.2	10.0	1.0	11.5	1.0	13.0	ns
		3.3 ^(*)	50		7.9	11.0	1.0	12.5	1.0	14.0	
		5.0 ^(**)	15		4.4	6.5	1.0	7.5	1.0	8.5	
		5.0 ^(**)	50		4.8	7.0	1.0	8.0	1.0	9.0	
t _W	LE Pulse Width, HIGH	3.3 ^(*)			4.0			4.0		4.0	ns
		5.0 ^(**)			3.0			3.0		3.0	
t _S	Setup Time D to LE, HIGH or LOW	3.3 ^(*)			3.0			3.0		3.0	ns
		5.0 ^(**)			2.0			2.0		2.0	
t _H	Hold Time D to LE, HIGH or LOW	3.3 ^(*)			1.0			1.0		1.0	ns
		5.0 ^(**)			1.0			1.0		1.0	

(*) Voltage range is 3.3V ± 0.3V
 (**) Voltage range is 5.0V ± 0.5V

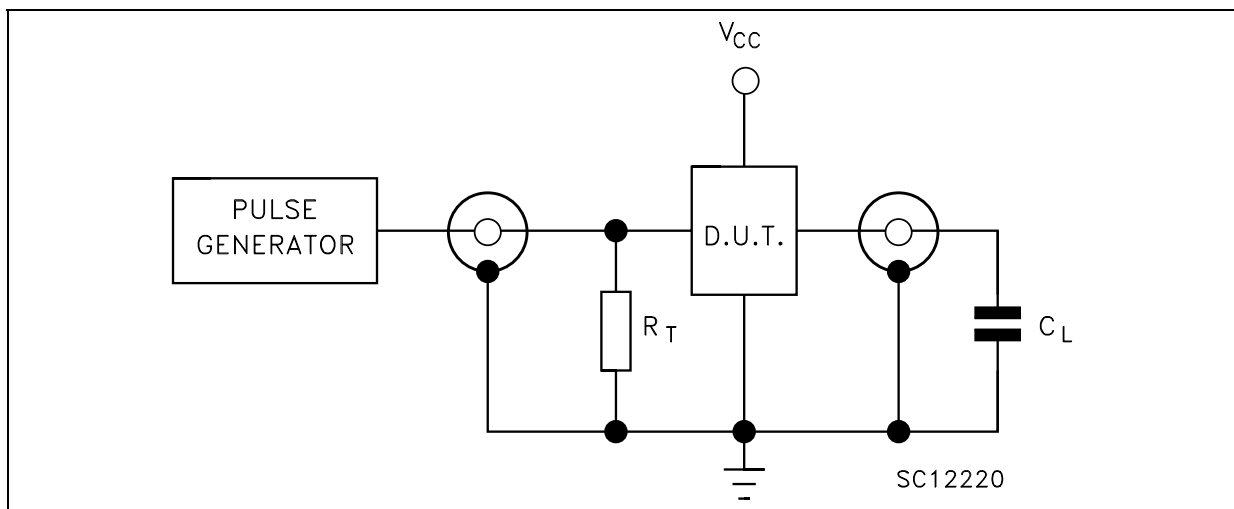


CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Value						Unit	
			T _A = 25°C			-40 to 85°C		-55 to 125°C		
			Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance			4	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)			8						pF

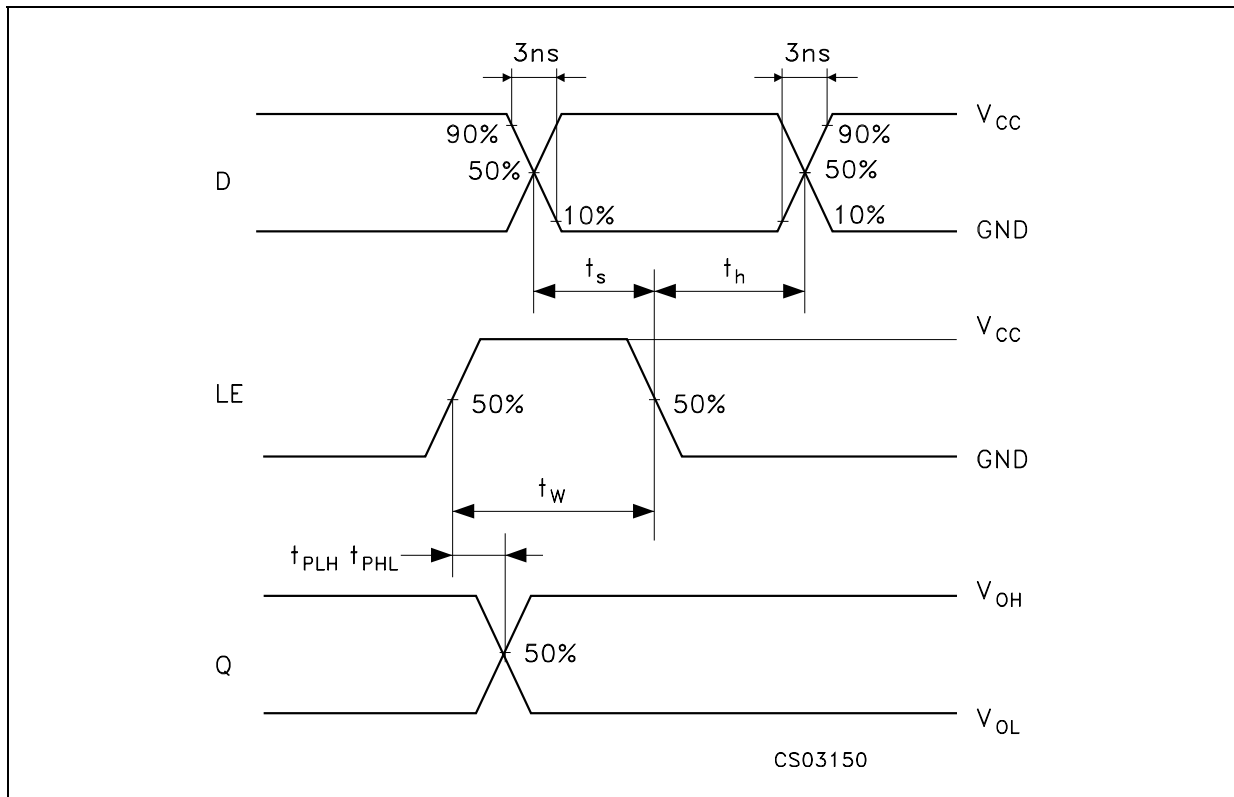
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

TEST CIRCUIT

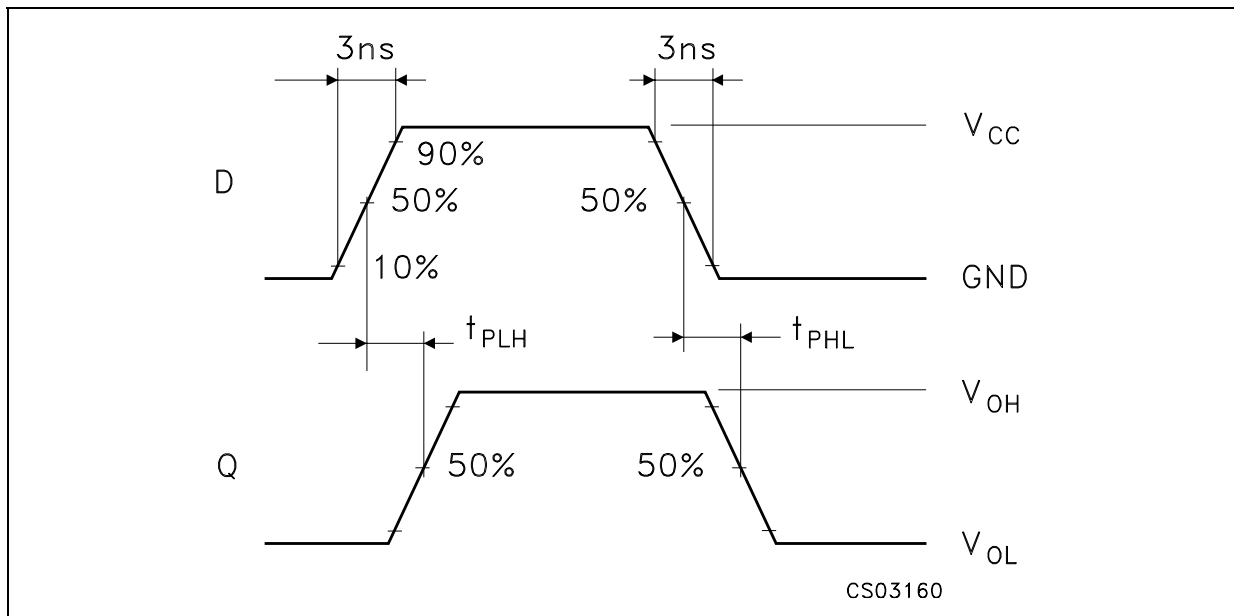


C_L = 15/50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)

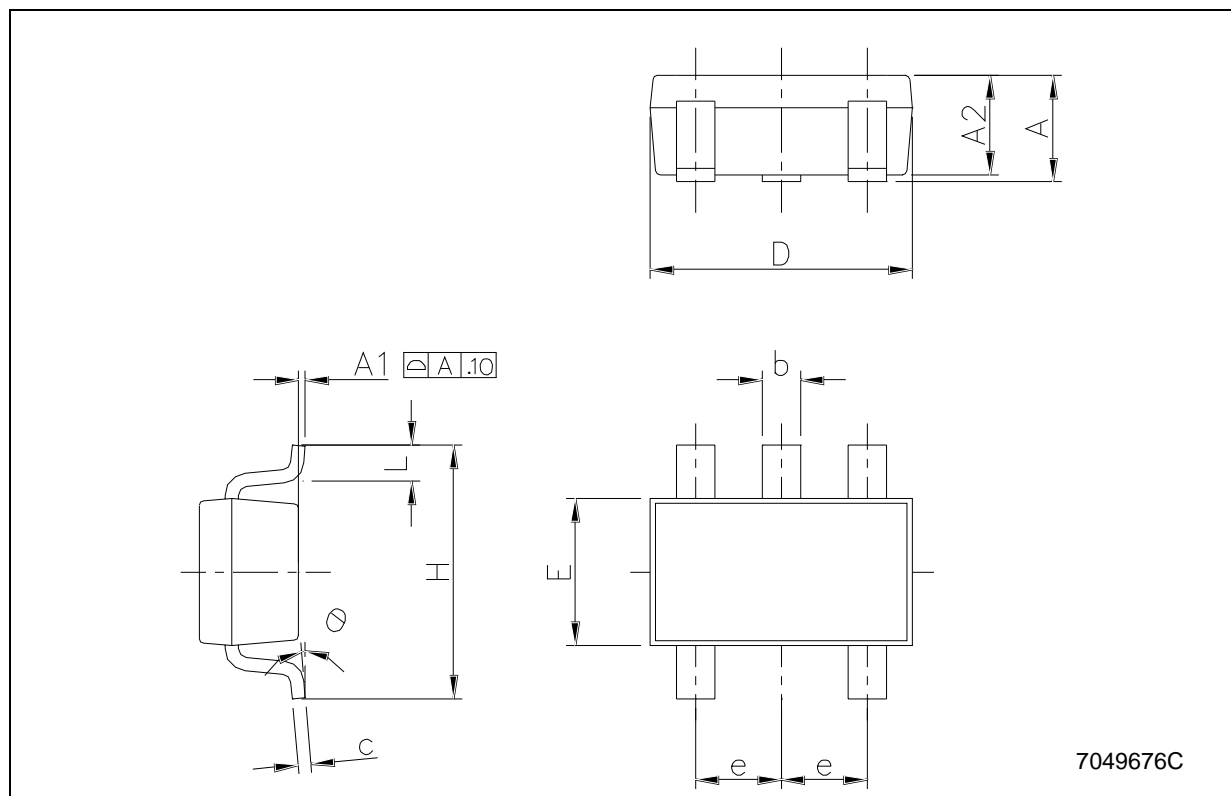


WAVEFORM 2: PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



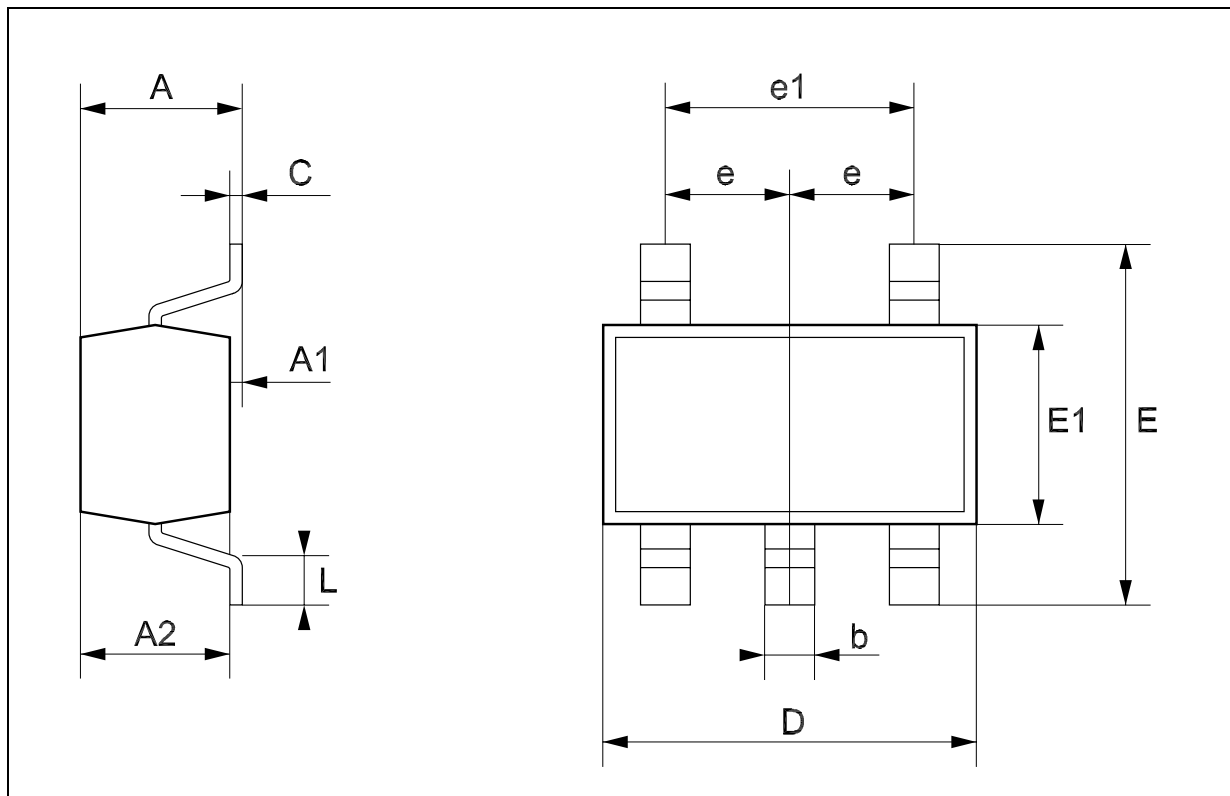
SOT23-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



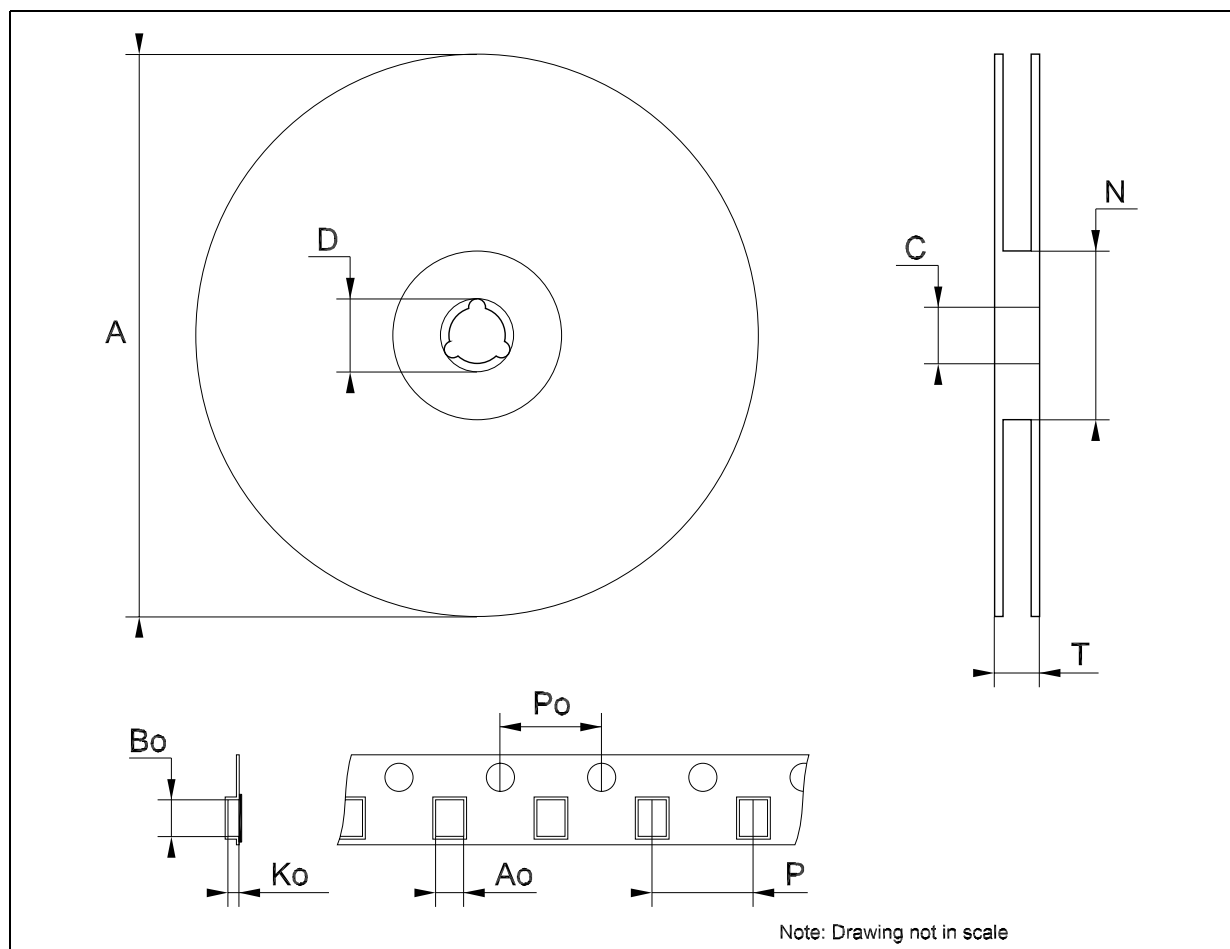
SOT323-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80		1.10	31.5		43.3
A1	0.00		0.10	0.0		3.9
A2	0.80		1.00	31.5		39.4
b	0.15		0.30	5.9		11.8
C	0.10		0.18	3.9		7.1
D	1.80		2.20	70.9		86.6
E	1.80		2.40	70.9		94.5
E1	1.15		1.35	45.3		53.1
e		0.65			25.6	
e1		1.3			51.2	
L	0.10		0.30	3.9		11.8



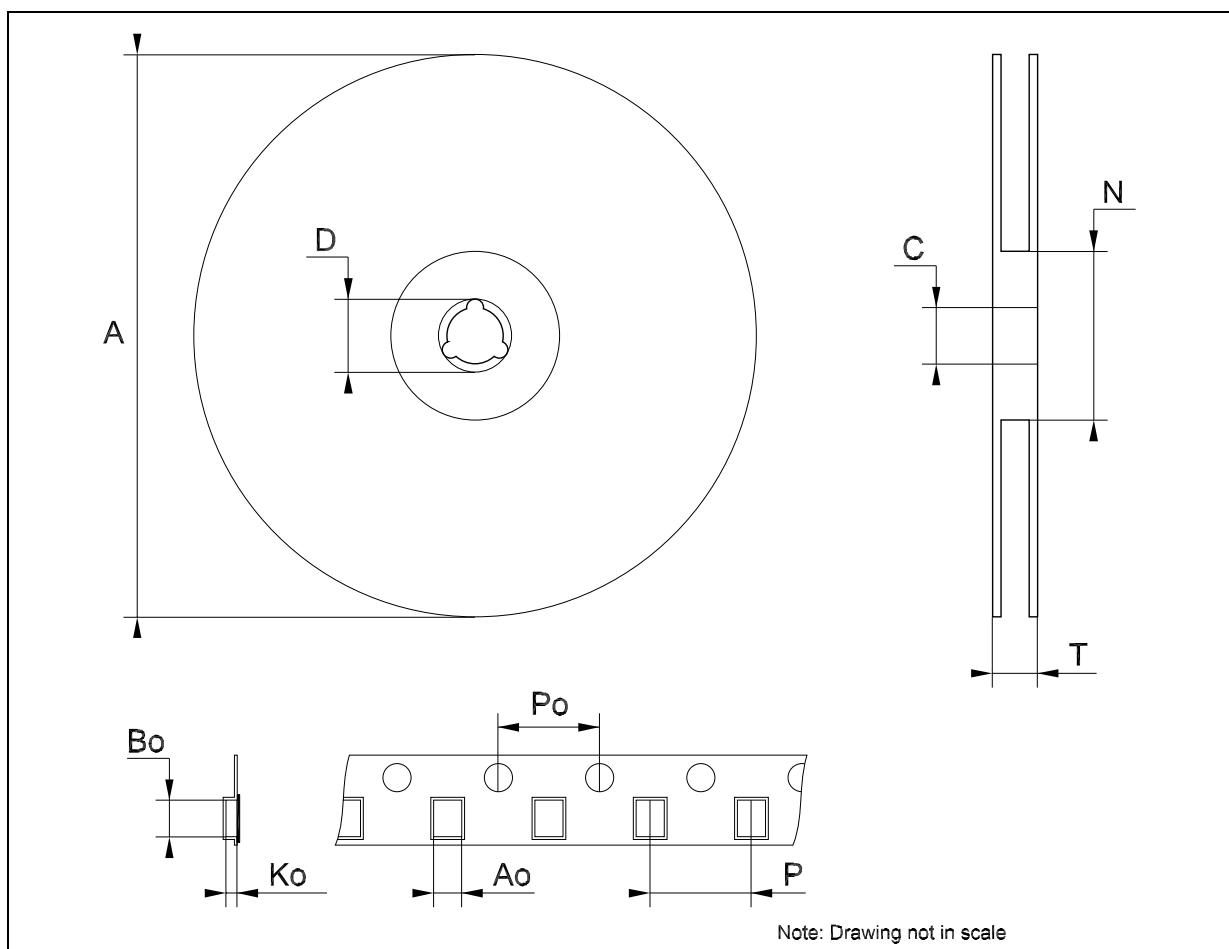
Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Tape & Reel SOT323-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	175	180	185	6.889	7.086	7.283
C	12.8	13	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	59.5	60	60.5		2.362	
T			14.4			0.567
Ao		2.25			0.088	
Bo		2.7			0.106	
Ko		1.2			0.047	
Po	3.9	4	4.1	0.153	0.157	0.161
P	3.8	4	4.2	0.149	0.157	0.165



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