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32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} max	Package Options	
		44 J-Lead Quad Plastic Chip Carrier	Dice in Waffle Pack Chip Carrier
HV9308	80V	HV9308PJ	HV9308X
HV9408	80V	HV9408PJ	HV9408X

Features

- ❏ Processed with HVCMOS® technology
- ❏ Low power level shifting
- ❏ Shift register speed 8MHz
- ❏ Latched data outputs
- ❏ 5V CMOS compatible inputs
- ❏ Forward and reverse shifting options
- ❏ Diode to V_{PP} allows efficient power recovery
- ❏ 44-lead ceramic surface mount package
- ❏ Hi-Rel processing available

General Description

The HV93 and HV94 are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. $HV_{OUT}1$ is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV94 shifts in the counterclockwise direction when viewed from the top of the package and the HV93 shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the LE (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the LE input is high. The data in the latch is retained when LE is low.

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]	-0.5V to +7V
Supply voltage, V_{PP}[2]	-0.5V to +90V
Logic input levels[2]	-0.5 to V_{DD} + 0.5V
Ground current[3]	1.5A
Continuous total power dissipation[4]	1200mW
Operating temperature range	-40°C to 85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes:

1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND_1.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

Electrical Characteristics (V_{PP} = 60V, V_{DD} = 5V, T_A =25°C)

DC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
I_{PP}	V_{PP} Supply Current		100	μA	HV_{OUT} outputs HIGH to LOW
I_{DDQ}	I_{DD} Supply Current (Quiescent)		100	μA	All inputs = V_{DD} or GND
I_{DD}	I_{DD} Supply Current (Operating)		15	mA	V_{DD} = V_{DD} max, f_{CLK} = 8 MHz
V_{OH} (Data)	Shift Register Output Voltage	V_{DD}-0.5		V	I_O = -100μA
V_{OL} (Data)	Shift Register Output Voltage		0.5	V	I_O = 100μA
I_{IH}	Current Leakage, any input		1.0	μA	Input = V_{DD}
I_{IL}	Current Leakage, any input		-1.0	μA	Input = GND
V_{OC}	HV_{OUT} Output Clamp Diode Voltage		-1.5	V	I_{OC} = -5mA
V_{OH}	HV_{OUT} Output when Sourcing	52		V	I_{OH} = -20mA, 0 to 70°C
V_{OL}	HV_{OUT} Output when Sinking		4.0	V	I_{OL} = 5mA, 0 to 70°C

AC Characteristics

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock Frequency		8.0	MHz	
t_{WL} or t_{WH}	Clock width, HIGH or LOW	62		ns	
t_{SU}	Setup time before CLK rises	25		ns	
t_H	Hold time after CLK rises	10		ns	
t_{DLH} (Data)	Data Output Delay after L to H CLK		110	ns	C_L = 15pF
t_{DHL} (Data)	Data Output Delay after H to L CLK		110	ns	C_L = 15pF
t_{DLE}	LE Delay after L to H CLK	50		ns	
t_{WLE}	Width of LE Pulse	50		ns	
t_{SLE}	LE Setup Time before L to H CLK	50		ns	
t_{ON}	Delay from LE to HV_{OUT}, L to H		500	ns	
t_{OFF}	Delay from LE to HV_{OUT}, H to L		500	ns	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic Voltage Supply		4.5	5.5	V
V_{PP}	High Voltage Supply		8.0	80	V
V_{IH}	Input HIGH Voltage		V_{DD}-0.5	V_{DD}	V
V_{IL}	Input LOW Voltage		0	0.5	V
f_{CLK}	Clock Frequency		0	8.0	MHz
T_A	Operating Free-Air Temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C

Notes:

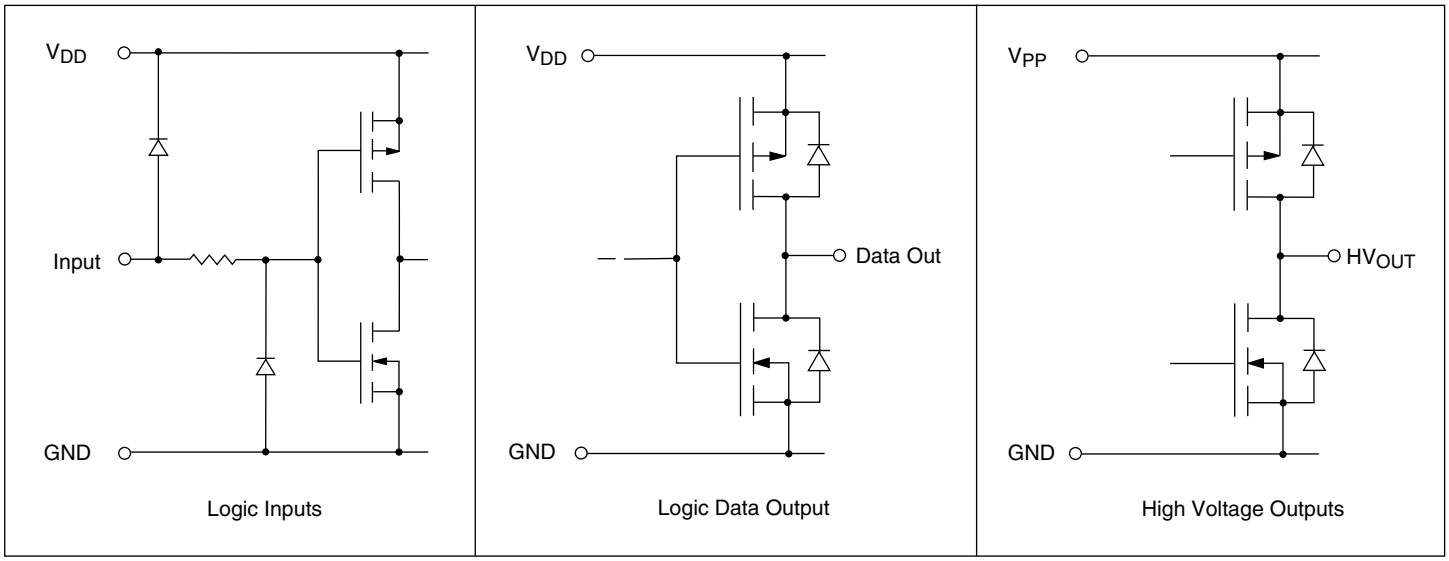
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

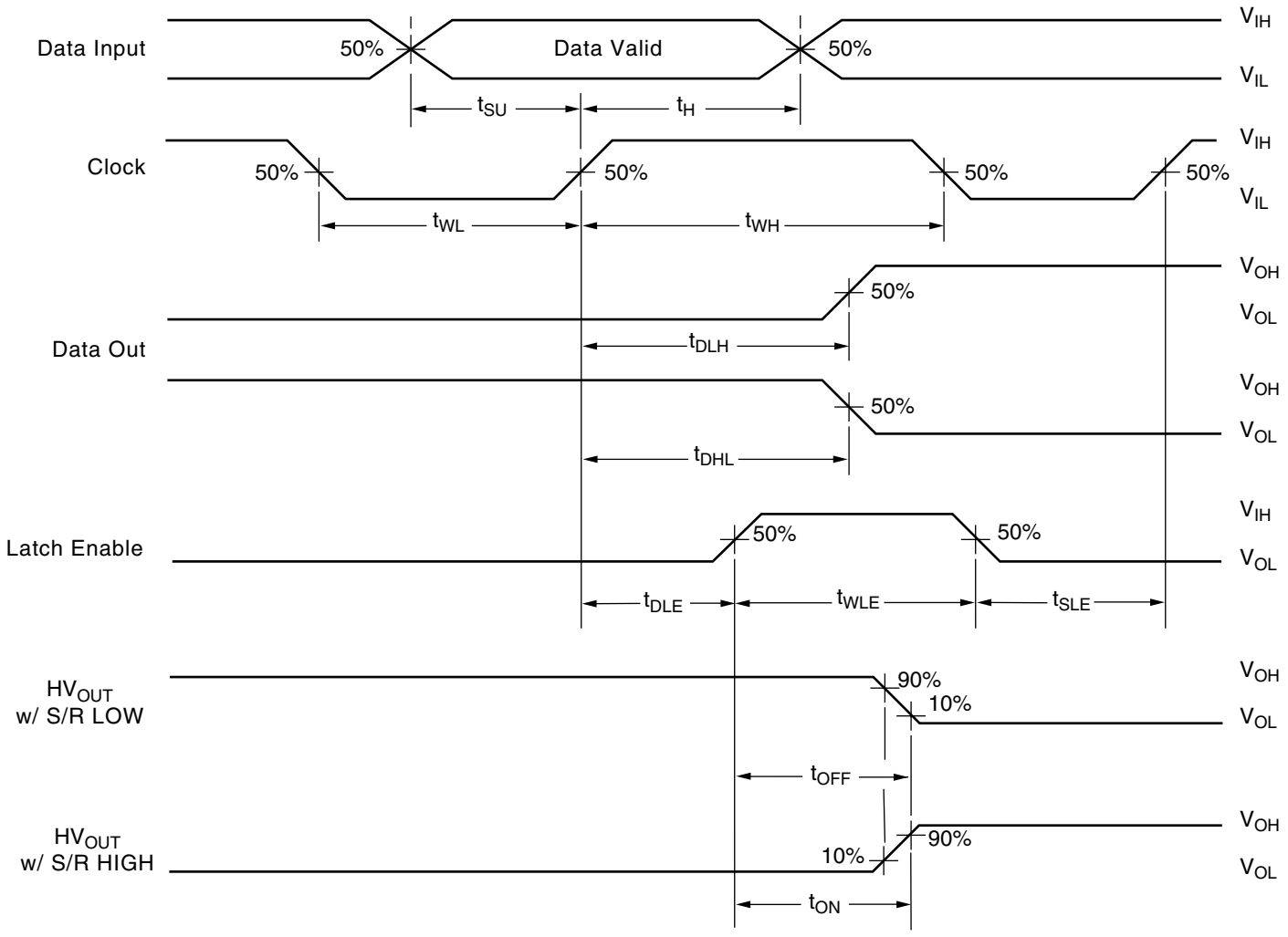
Power-down sequence should be the reverse of the above.

The V_{PP} should not drop below V_{DD} during operations.

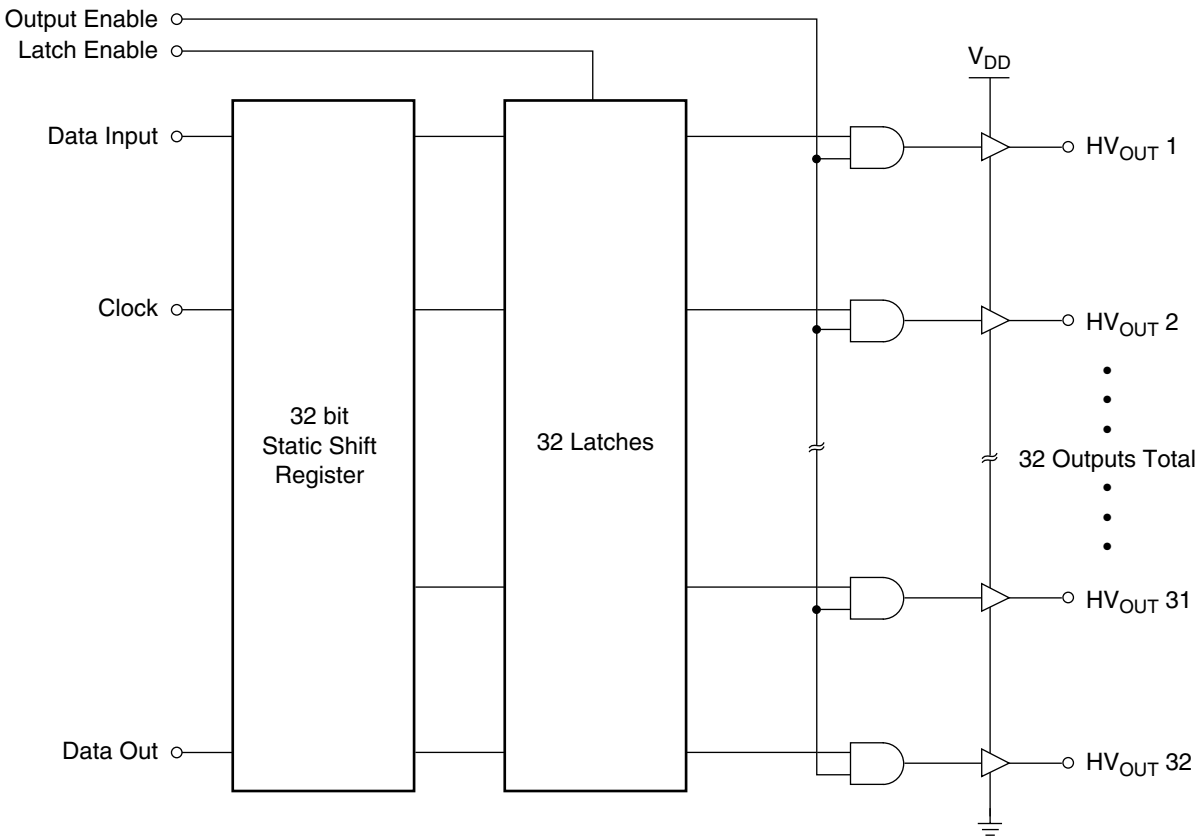
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Tables

Data Input	CLK*	Data Output
H	↑	H
L	↑	L
X	No ↑	No Change

* ↑ = LOW-to-HIGH level transition

Data Input	LE	OE	HV_{OUT} Output
X	X	L	All HV_{OUT} = LOW
X	L	H	Previous Latched Data
H	H	H	H
L	H	H	L

Pin Configuration

HV93

44 Pin J-Lead Package

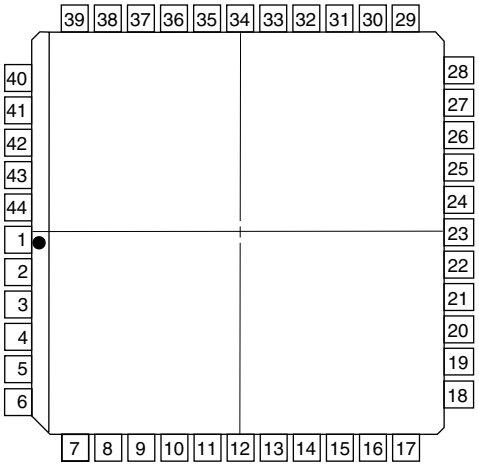
Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Output Enable
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HV_{OUT} 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	N/C	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

HV94

44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
3	HV_{OUT} 18	25	V_{DD}
4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Output Enable
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	N/C	43	HV_{OUT} 14
22	Clock	44	HV_{OUT} 15

Package Outline



top view

44-pin J-Lead Package

Supertex inc.

1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 744-0100 • FAX: (408) 222-4895
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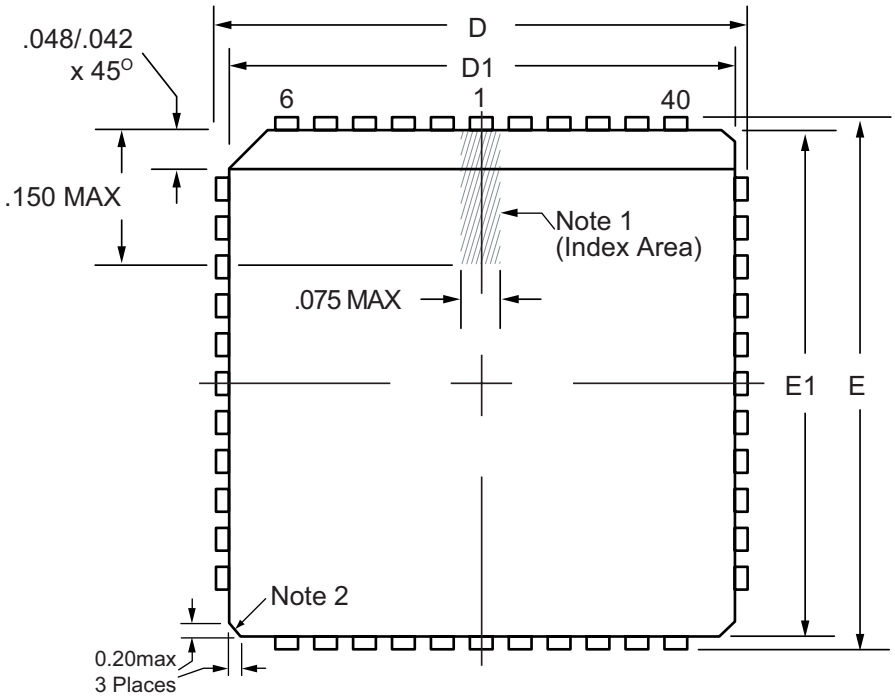
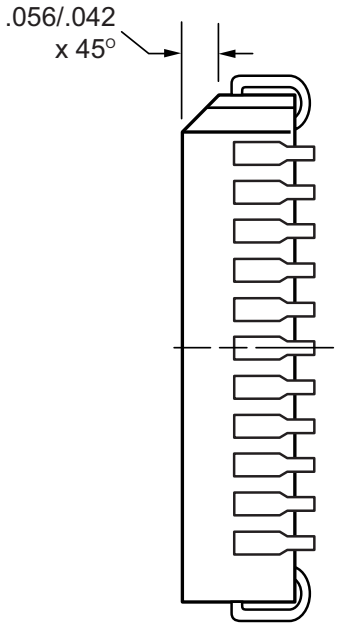
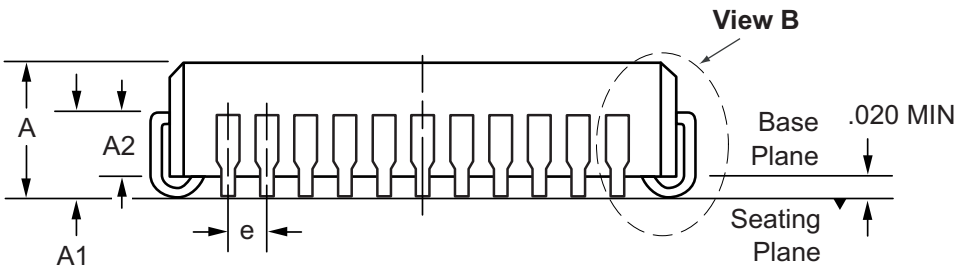
44-Lead PLCC Package Outline (PJ)



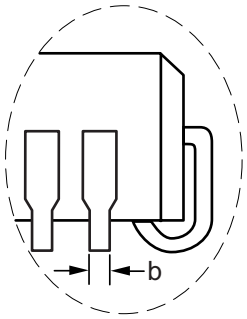
Top View



Side View



Side View



View B

Note:

1. A Pin 1 identifier must be located in the index area indicated.The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

2. Exact shape of this feature is optional.

Symbol		A	A1	A2	b	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.685	.650	.685	.650	.050 BSC
	NOM	.172	.105	-	-	.690	.653	.690	.653	
	MAX	.180	.120	.083	.021	.695	.656	.695	.656	

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

Drawings are not to scale.

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