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July 1988
Revised March 2001

FAIRCHILD

SEMICONDUCTOR™

100324

Low Power Hex TTL-to-ECL Translator

General Description

The 100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full −4.2V to −5.7V range.

When the circuit is used in the differential mode, the 100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

The 100324 is pin and function compatible with the 100124 with similar AC performance, but features power dissipation roughly half of the 100124 to ease system cooling requirements.
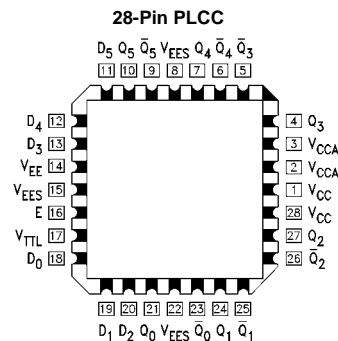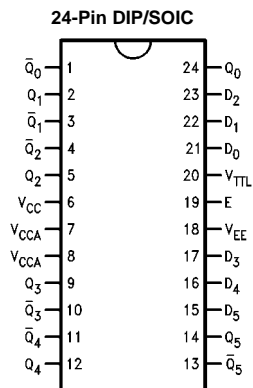
Features

■ Pin/function compatible with 100124
■ Meets 100124 AC specifications
■ 50% power reduction of the 100124
■ Differential outputs
■ 2000V ESD protection
■ −4.2V to −5.7V operating range
■ Available to MIL-STD-883
■ Available to industrial grade temperature range (PLCC package only)

Ordering Code:

Order Number	Package Number	Package Description
100324SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100324PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100324QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100324QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (−40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

24-Pin DIP/SOIC

$\bar{Q}_0$	1	24	Q_0
Q_1	2	23	D_2
$\bar{Q}_1$	3	22	D_1
$\bar{Q}_2$	4	21	D_0
Q_2	5	20	V_{TTL}
V_{CC}	6	19	E
V_{CCA}	7	18	V_{EE}
V_{CCA}	8	17	D_3
Q_3	9	16	D_4
$\bar{Q}_3$	10	15	D_5
$\bar{Q}_4$	11	14	Q_5
Q_4	12	13	$\bar{Q}_5$

28-Pin PLCC

Top pins: D_5 Q_5 $\bar{Q}_5$ V_{EES} Q_4 $\bar{Q}_4$ $\bar{Q}_3$ (11 10 9 8 7 6 5)

Left pins:
D_4 12
D_3 13
V_{EE} 14
V_{EES} 15
E 16
V_{TTL} 17
D_0 18

Right pins:
4 Q_3
3 V_{CCA}
2 V_{CCA}
1 V_{CC}
28 V_{CC}
27 Q_2
26 $\bar{Q}_2$

Bottom pins: (19 20 21 22 23 24 25) D_1 D_2 Q_0 V_{EES} $\bar{Q}_0$ Q_1 $\bar{Q}_1$

Pin Descriptions

Pin Names	Description
D_0–D_5	Data Inputs
E	Enable Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary
	Data Outputs

Truth Table

Inputs		Outputs	
D_n	E	Q_n	$\overline{Q}_n$
X	L	L	H
L	H	L	H
H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram
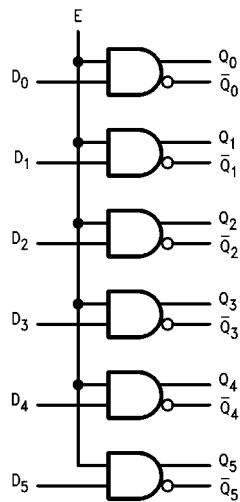
Absolute Maximum Ratings (Note 1)

Storage Temperature (T_{STG})	$-65°C$ to $+150°C$
Maximum Junction Temperature (T_J)	$+150°C$
V_{EE} Pin Potential to Ground Pin	$-7.0V$ to $+0.5V$
V_{TTL} Pin Potential to Ground Pin	$-0.5V$ to $+6.0V$
Input Voltage (DC)	$-0.5V$ to $+6.0V$
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	$\geq 2000V$

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	$0°C$ to $+85°C$
Industrial	$-40°C$ to $+85°C$
Supply Voltage (V_{EE})	$-5.7V$ to $-4.2V$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics (Note 3)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = $ GND, $T_C = 0°C$ to $+85°C$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	-1830	-1705	-1620		or $V_{IL\ (Min)}$	50Ω to $-2.0V$
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH(Min)}$	Loading with
V_{OLC}	Output LOW Voltage			-1610		or $V_{IL\ (Max)}$	50Ω to $-2.0V$
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	-1.2			V	$I_{IN} = -18$ mA	
I_{IH}	Input HIGH Current Data Enable			20 120	µA	$V_{IN} = +2.4V$, All Other Inputs $V_{IN} = $ GND	
	Input HIGH Current Breakdown Test, All Inputs			1.0	mA	$V_{IN} = +5.5V$, All Other Inputs $= $ GND	
I_{IL}	Input LOW Current Data Enable	-0.9 -5.4			mA	$V_{IN} = +0.4V$, All Other Inputs $V_{IN} = V_{IH}$	
I_{EE}	V_{EE} Power Supply Current	-70	-45	-22	mA	All Inputs $V_{IN} = +4.0V$	
I_{TTL}	V_{TTL} Power Supply Current		25	38	mA	All Inputs $V_{IN} = $ GND	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electric Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = $ GND, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.50	3.00	ns	Figures 1, 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Commercial Version (Continued)
SOIC and PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	Figures 1, 2
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.95		0.95		0.95	ns	PLCC Only (Note 4)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.70		0.70		0.70	ns	PLCC Only (Note 4)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1.60		1.60		1.60	ns	PLCC Only (Note 4)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		1.20		1.20		1.20	ns	PLCC Only (Note 4)

Note 4: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

DC Electrical Characteristics (Note 5)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40°C$ to $+85°C$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol	Parameter	$T_C = -40°C$		$T_C = 0°C$ to $+85°C$		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	$V_{IN} = V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620		or $V_{IL\ (Min)}$	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	$V_{IN} = V_{IH(Min)}$	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610		or $V_{IL\ (Max)}$	50Ω to −2.0V
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	Guaranteed LOW Signal for All Inputs	
V_{CD}	Input Clamp Diode Voltage	−1.2		−1.2		V	$I_{IN} = -18$ mA	
I_{IH}	Input HIGH Current Data Enable		20 120		20 120	µA	$V_{IN} = +2.4V$, All Other Inputs $V_{IN} = GND$	
	Input HIGH Current Breakdown Test, All Inputs		1.0		1.0	mA	$V_{IN} = +5.5V$, All Other Inputs = GND	
I_{IL}	Input LOW Current Data Enable	−0.9 −5.4		−0.9 −5.4		mA	$V_{IN} = +0.4V$, All Other Inputs $V_{IN} = V_{IH}$	
I_{EE}	V_{EE} Power Supply Current	−70	−22	−70	−22	mA	All Inputs $V_{IN} = +4.0V$	
I_{TTL}	V_{TTL} Power Supply Current		38		38	mA	All Inputs $V_{IN} = GND$	

Note 5: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = -40°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	Figures 1, 2
t_{TLH} t_{THL}	Transition Times 20% to 80%, 80% to 20%	0.35	1.80	0.45	1.70	0.45	1.70	ns	Figures 1, 2

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Test Circuit
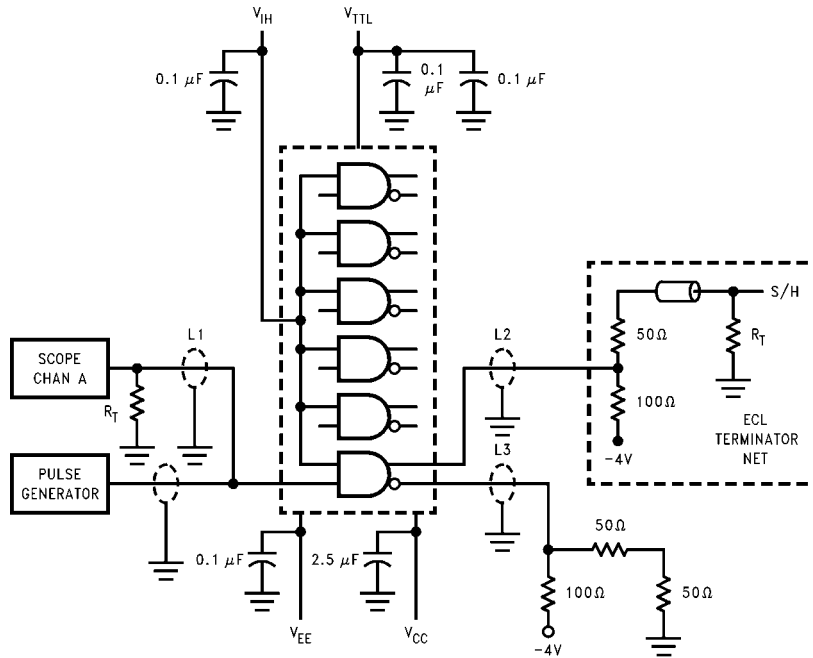
Note:

- V_{CC}, $V_{CCA} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5.0V$, $V_{IH} = +3.0V$
- L1, L2 and L3 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
- All unused outputs are loaded with 50Ω to −2V or with equivalent ECL terminator network
- C_L = Fixture and stray capacitance ≤ 3 pF
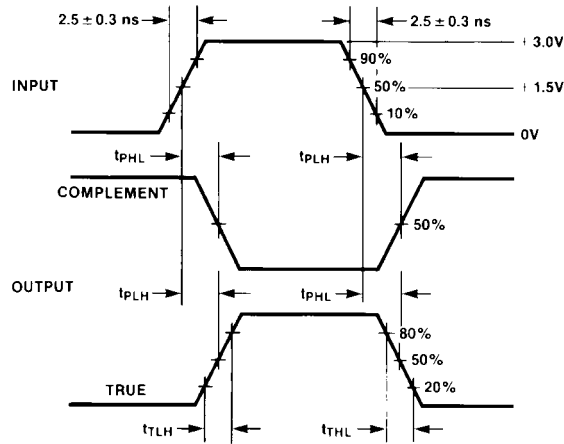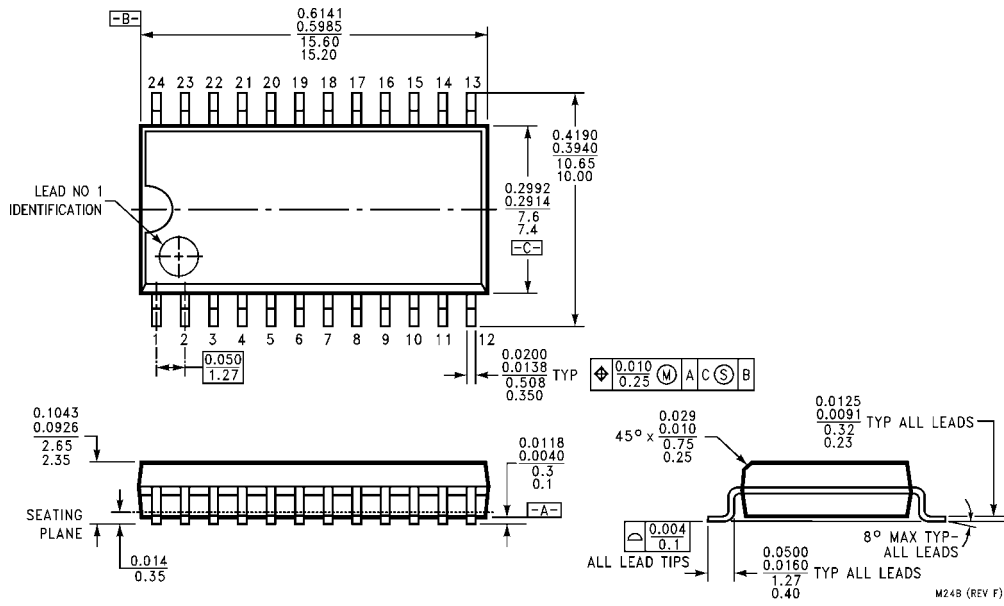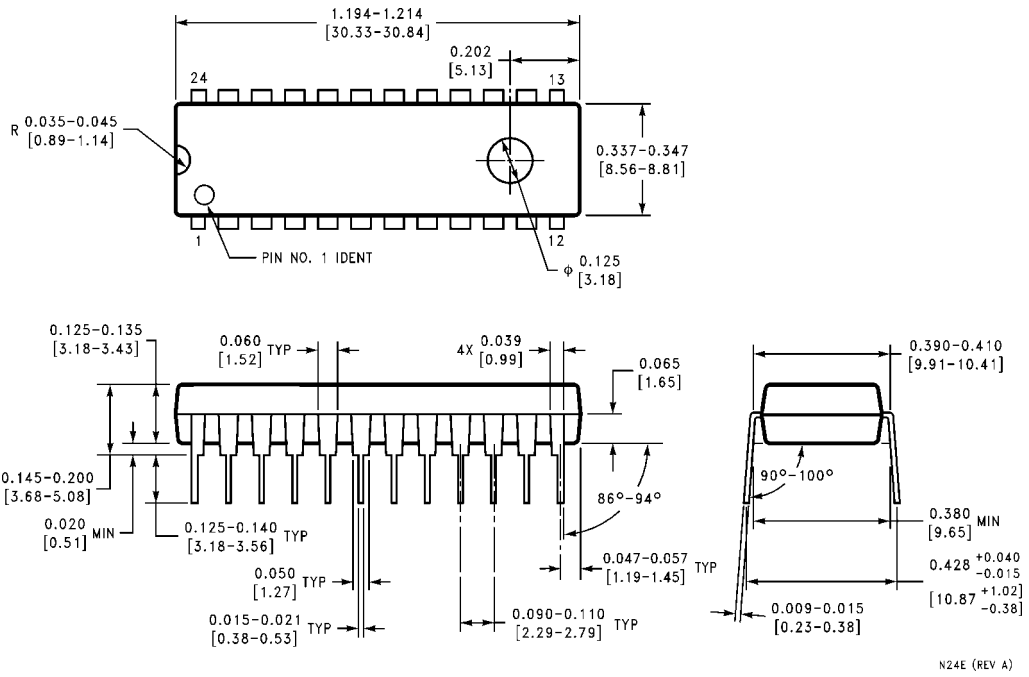
FIGURE 1. AC Test Circuit

Switching Waveform

FIGURE 2. Propagation Delay and Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted

**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.450 $^{+0.006}_{-0.000}$
[11.43] $^{+0.15}_{-0.00}$

PIN #1 IDENT

0.029±0.003 TYP
[0.74±0.08]

45° X 0.045
[1.14]

0.017±0.004 TYP
[0.43±0.10]

0.410±0.020 TYP
[10.41±0.51]

SEATING PLANE

0.020 MIN TYP
[0.51]

0.105±0.015 TYP
[2.67±0.38]

0.050 TYP
[1.27]

0.300 TYP
[7.62]

45° X 0.045
[1.14]

0.165-0.180 TYP
[4.19-4.57]

0.004 [0.10]

0.490±0.005 TYP
[12.45±0.13]
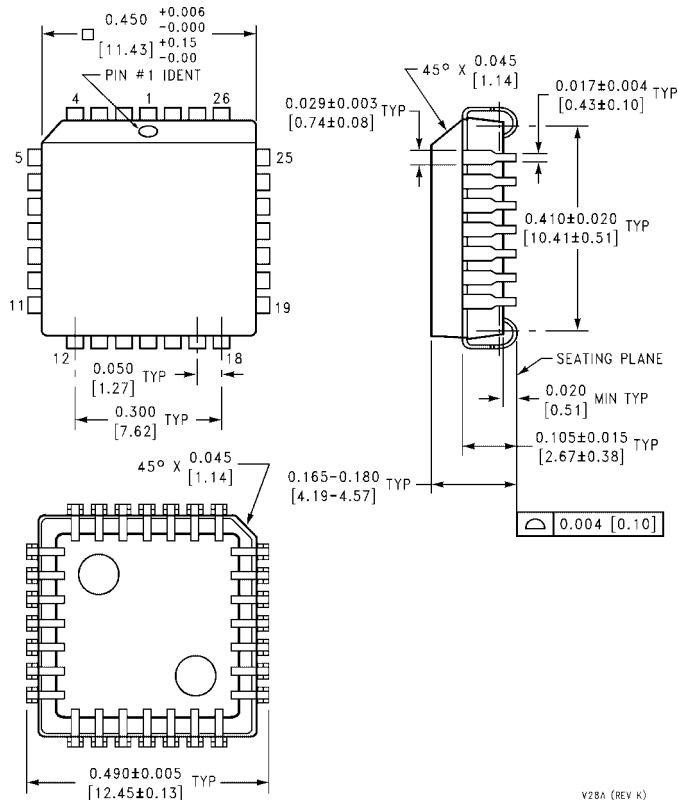
V28A (REV K)

28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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