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**SANYO**

CMOS LSI
# LC75822E/75822W — LCD Display Drivers

## Overview

The LC75822E and LC75822W are general-purpose LCD display drivers that can be used for frequency display in microprocessor-controlled radio receivers and in other display applications.

## Features

- 53 segment outputs (the maximum for static drive)
- Two drive types: static (1/1) duty (53 segments) and 1/2 duty (104 segments)
- Serial data input supports CCB* format communication with the system controller
- $\overline{\text{INH}}$ pin for turning off all display output
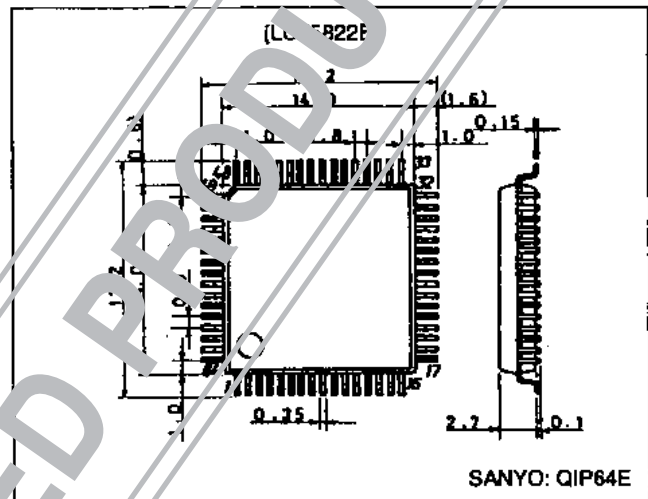- The LC75822 is a CCB version of the LC75821 product.

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- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.
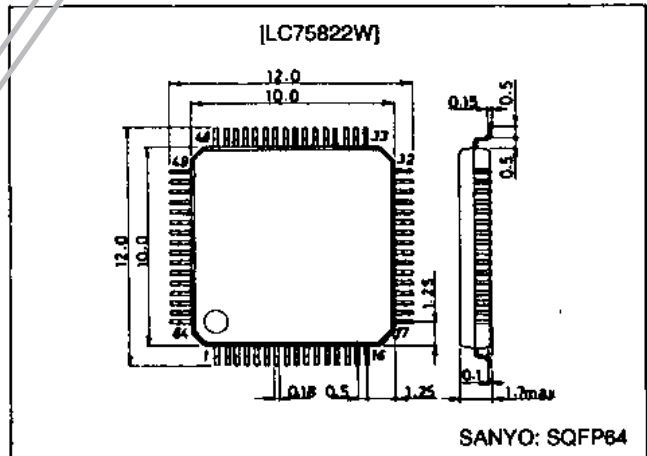
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## Package Dimensions

unit: mm
**3159-QFP64E**

CCB



[LC75822E]

SANYO: QIP64E

unit: mm
**3190-SQFP64**



[LC75822W]

SANYO: SQFP64

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# Specifications

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 to +7.0 | V |
| | $V_{LCD}$ | $V_{LCD}$ | –0.3 to $V_{DD}$ + 0.3 | V |
| Input voltage | $V_{IN}1$ | CE, CL, DI, $\overline{INH}$ | –0.3 to +7.0 | V |
| | $V_{IN}2$ | OSC: output off | –0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage | $V_{OUT}$ | OSC: output off | –0.3 to $V_{DD}$ + 0.3 | V |
| Output current | $I_{OUT}1$ | S1 to S53 | 30 | µA |
| | $I_{OUT}2$ | COM1, COM2 | 1.0 | mA |
| Allowable power dissipation | Pd max | Ta = 85°C | 100 | mW |
| Operating temperature | Topr | | –40 to +85 | °C |
| Storage temperature | Tstg | | –55 to +125 | °C |

## Allowable Operating Ranges at Ta = –40 to +85°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 3.0 | | 6.5 | V |
| | $V_{LCD}$ | $V_{LCD}$ | 3.0 | | $V_{DD}$ | V |
| Input high-level voltage | $V_{IH}1$ | $\overline{INH}$ | 0.7 $V_{DD}$ | | 6.5 | V |
| Input low-level voltage | $V_{IL}1$ | $\overline{INH}$ | 0 | | 0.3 $V_{DD}$ | V |
| Input high-level voltage | $V_{IH}2$ | CE, CL, DI | 0.8 $V_{DD}$ | | 6.5 | V |
| Input low-level voltage | $V_{IL}2$ | CE, CL, DI | 0 | | 0.2 $V_{DD}$ | V |
| Recommended external resistance | $R_{OSC}$ | OSC | | 51 | | kΩ |
| Recommended external capacitance | $C_{OSC}$ | OSC | | 680 | | pF |
| Guaranteed oscillation range | $f_{OSC}$ | OSC | 25 | 50 | 100 | kHz |
| Clock low-level pulse width | $t_{\phi L}$ | CL | 250 | | | ns |
| Clock high-level pulse width | $t_{\phi H}$ | CL | 250 | | | ns |
| Data setup time | $t_{ds}$ | CL, DI | 250 | | | ns |
| Data hold time | $t_{dh}$ | CL, DI | 250 | | | ns |
| CE wait time | $t_{cp}$ | CE, CL | 250 | | | ns |
| CE setup time | $t_{cs}$ | CE, CL | 250 | | | ns |
| CE hold time | $t_{ch}$ | CE, CL | 250 | | | ns |

## Electrical Characteristics for the Allowable Operating Ranges

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high-level current | $I_{IH}$ | CE, CL, DI, $\overline{INH}$: $V_I$ = 6.5 V | | | 5 | µA |
| Input low-level current | $I_{IL}$ | CE, CL, DI, $\overline{INH}$: $V_I$ = 0 V | –5 | | | µA |
| Output high-level voltage | $V_{OH}1$ | S1 to S53: $I_O$ = –10 µA | $V_{DD}$ – 1.0 | | | V |
| Output low-level voltage | $V_{OL}1$ | S1 to S53: $I_O$ = 10 µA | | | 1.0 | V |
| Output high-level voltage | $V_{OH}2$ | COM1, COM2: $I_O$ = –100 µA | $V_{LCD}$ – 0.6 | | | V |
| Output low-level voltage | $V_{OL}2$ | COM1, COM2: $I_O$ = 100 µA | | | 0.6 | V |
| Mid-level voltage | $V_{MID}1$ | COM1, COM2: $V_{LCD}$ = 6.5 V, $I_O$ = ±100 µA | 2.65 | 3.25 | 3.85 | V |
| | $V_{MID}2$ | COM1, COM2: $V_{LCD}$ = 3.0 V, $I_O$ = ±100 µA | 0.9 | 1.5 | 2.1 | V |
| Oscillator frequency | $f_{OSC}$ | OSC: R = 51 kΩ, C = 680 pF | 40 | 50 | 60 | kHz |
| Hysteresis voltage | $V_H$ | CE, CL, DI: $V_{DD}$ = 5 V | 0.3 | | | V |
| Current drain | $I_{DD}$ | | | | 0.6 | mA |
| | $I_{LCD}$ | $V_{LCD}$ | | | 2 | mA |

## Pin Assignment
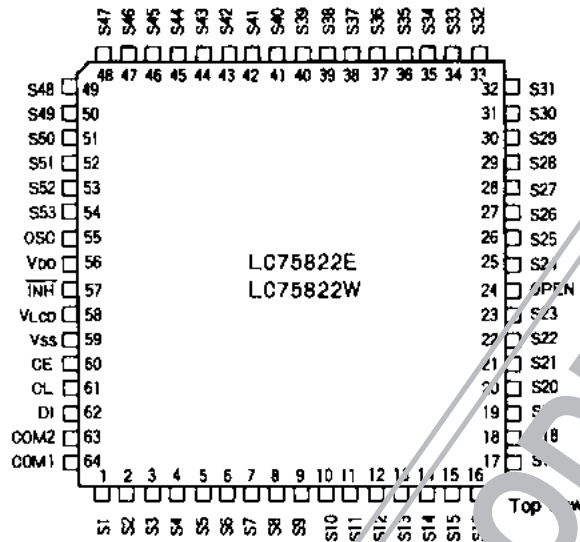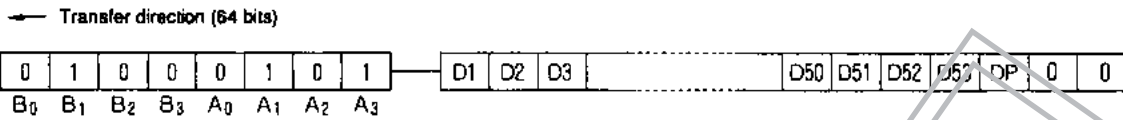


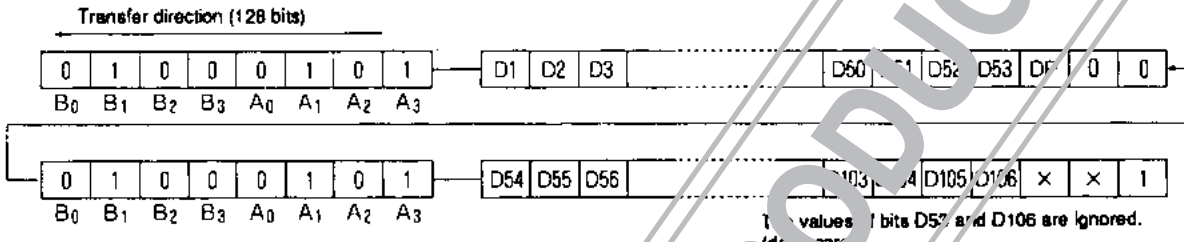## Block Diagram
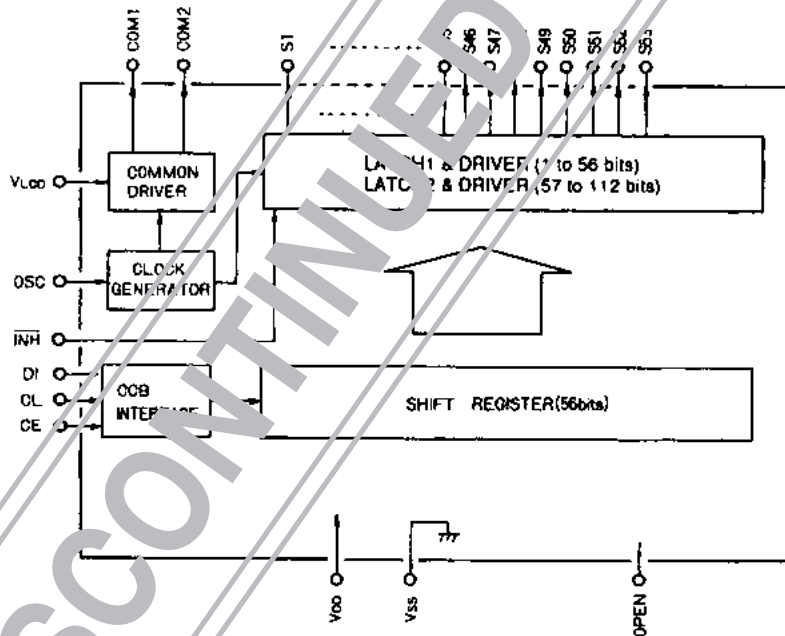


## Pin Functions

| Pin | Function |
|---|---|
| S1 to S53 | Segment output pins |
| COM1, COM2 | Common output pins (Only COM1 is used in static (1/1) drive. COM2 must be left open in that mode.) |
| V<sub>LCD</sub> | LCD bias voltage setting |
| OSC | Oscillator connection |
| CE, CL, DI | Serial data transfer inputs |
| V<sub>SS</sub>, V<sub>DD</sub> | Power supply |
| INH | Display off control input<br>INH = low (V<sub>SS</sub>) .........Display off (S1 to S53, COM1, COM2 = low)<br>INH = high (V<sub>DD</sub>).........Display on<br>Note that serial data transfers are still allowed when display output is turned off using this pin. |
| OPEN | Make no connections to this pin. |

## Data Transfer Format

1. Static (1/1) duty



Transfer direction (64 bits)

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D1 | D2 | D3 | | D50 | D51 | D52 | D53 | DP | 0 | 0 |

$B_0$ $B_1$ $B_2$ $B_3$ $A_0$ $A_1$ $A_2$ $A_3$

2. 1/2 duty (Only 64 bits need to be transferred if there are no more than 52 display segments. The transfer format is identical to the static duty case. It is not possible to change the D54 to D106 data without specifying the D1 to D53 data.)



Transfer direction (128 bits)

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D1 | D2 | D3 | | D50 | D51 | D52 | D53 | DP | 0 | 0 |

$B_0$ $B_1$ $B_2$ $B_3$ $A_0$ $A_1$ $A_2$ $A_3$

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D54 | D55 | D56 | | D103 | D104 | D105 | D106 | × | × | 1 |

$B_0$ $B_1$ $B_2$ $B_3$ $A_0$ $A_1$ $A_2$ $A_3$

The values of bits D53 and D106 are ignored.

CCB address: A2$_H$
DP: Drive type selection bit
    DP = 0: 1/1 duty
    DP = 1: 1/2 duty
D1 to D106: Display data
    Dn (for n = 1 to 106) = 0: Segment off
    Dn (for n = 1 to 106) = 1: Segment on
×: don't care

## Data Transfer Examples

1. Static duty

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D1 | D2 | D3 | | D52 | D53 | 0 | 0 | 0 |

2. 1/2 duty with 52 or fewer segments

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D1 | D2 | D3 | | D52 | D53 | 1 | 0 | 0 |
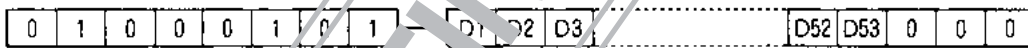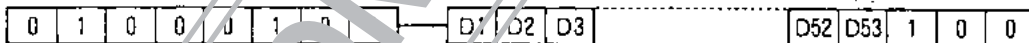
3. 1/2 duty with more than 52 segments

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D1 | D2 | D3 | | D52 | D53 | 1 | 0 | 0 |

| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D54 | D55 | D56 | | D105 | D106 | × | × | 1 |
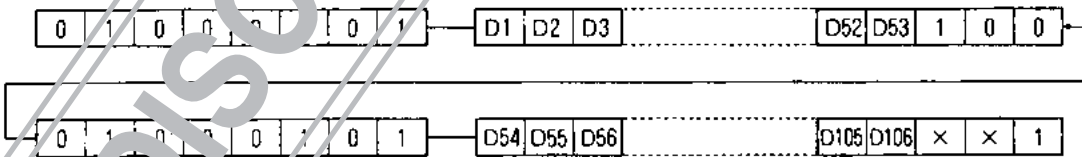
Note: The following transfer format is not allowed in 1/2 duty with 52 or fewer segments.

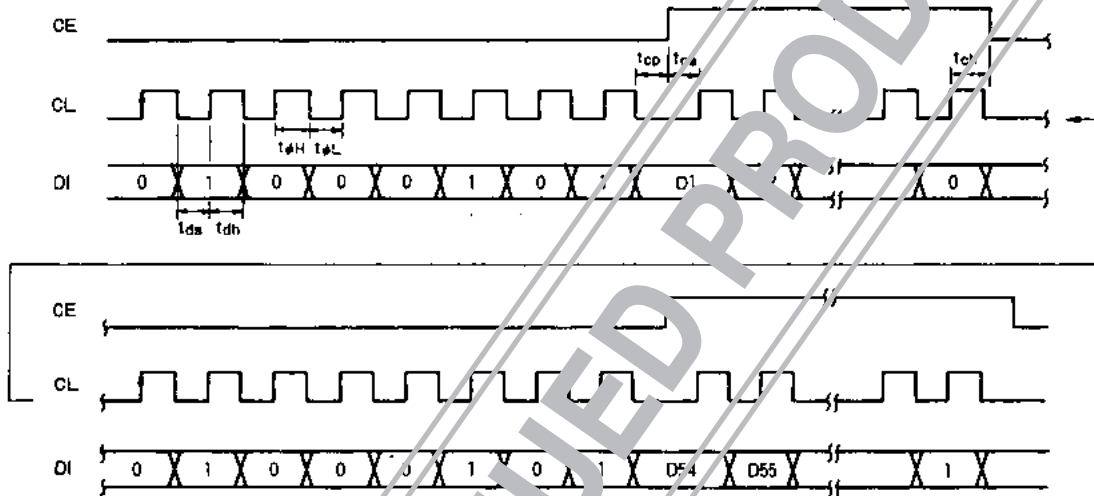| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | | D54 | D55 | D56 | | D105 | D106 | × | × | 1 |
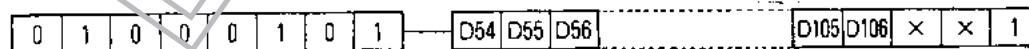
## Serial Data

1. Static duty (64 bits)
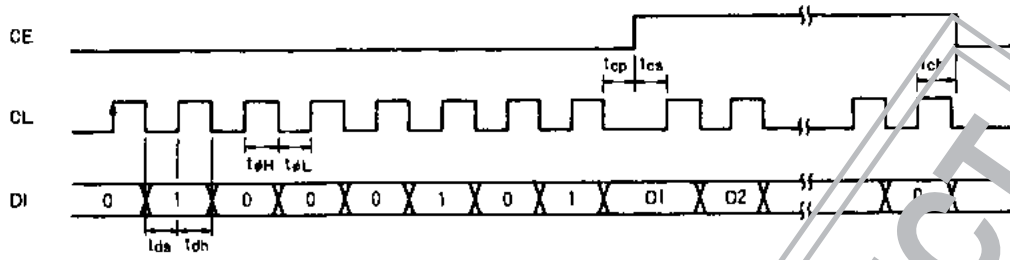


2. 1/2 duty (128 bits)



## Output Waveforms

1. Static duty

## 2. 1/2 duty



COM1

COM2

$\frac{f_{osc}}{512}$ (Hz)

S1 to S52 outputs when the COM1 segment is on

S1 to S52 outputs when the COM2 segment is on

S1 to S52 outputs when both the COM1 and COM2 segments are on

S1 to S52 outputs when both the COM1 and COM2 segments are off
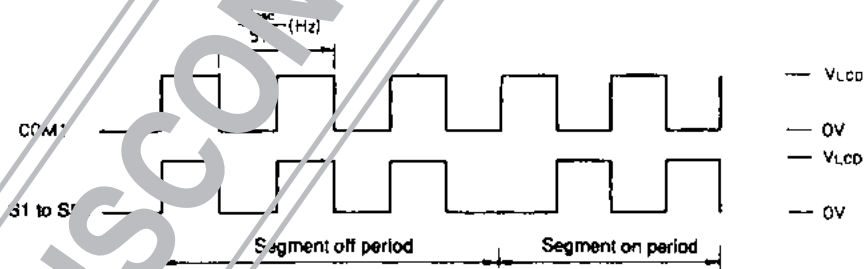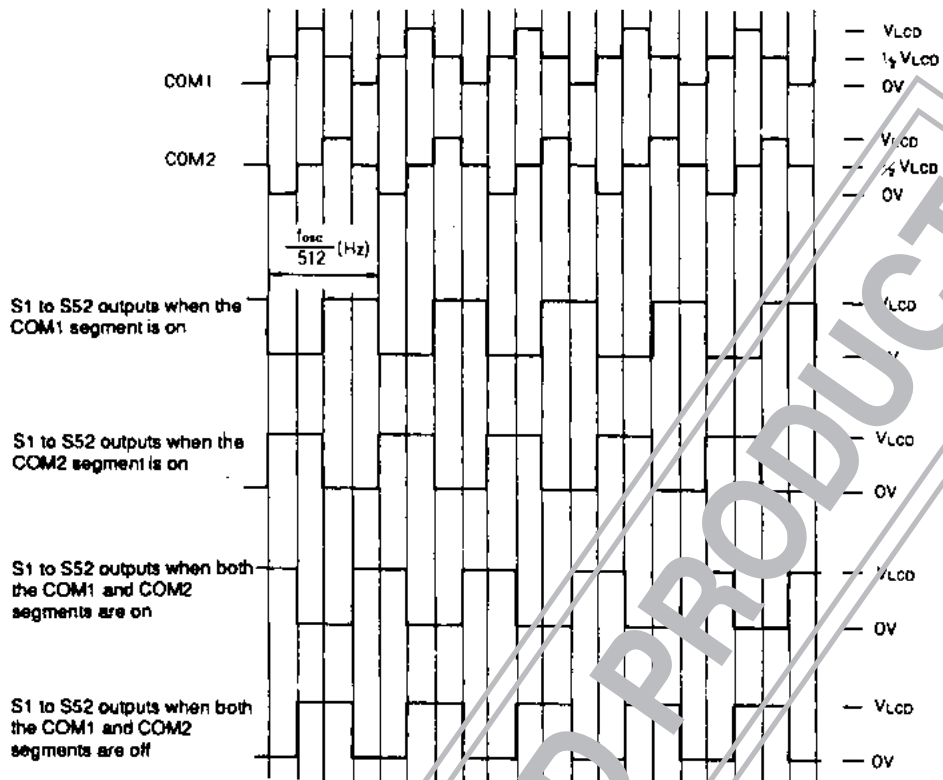
## Display Examples

### 1. Static drive (1/1 duty)

Example with 40 segments (up to 52 segments can be driven.)
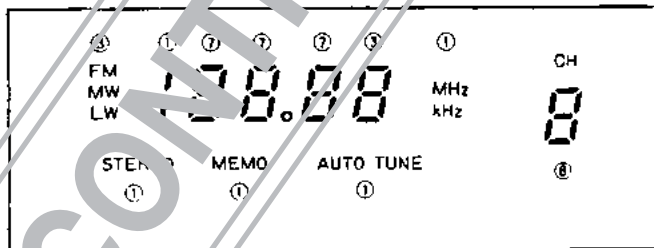


Note: Numbers in circles indicate the number of segments used.

### 2. 1/2 duty drive

Example with 80 segments (Up to 104 segments can be driven.)
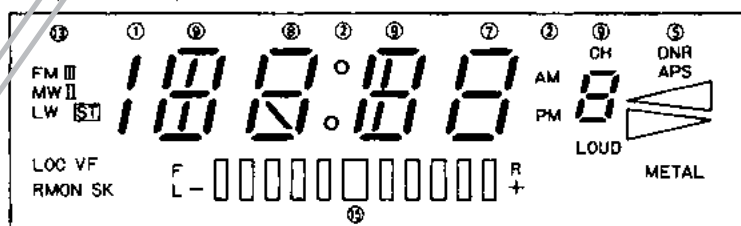
## Sample Application Circuit 1
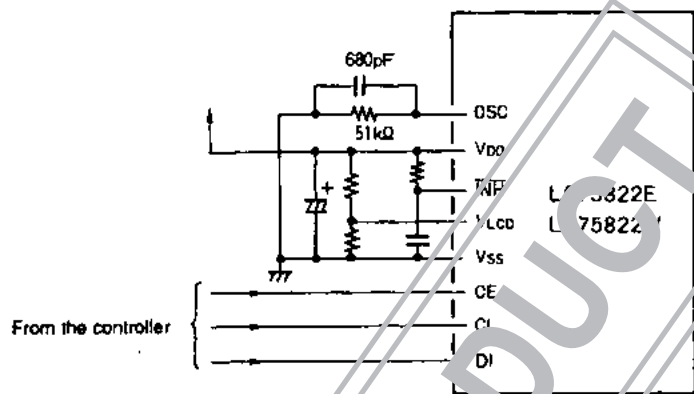


## Sample Application Circuit 2
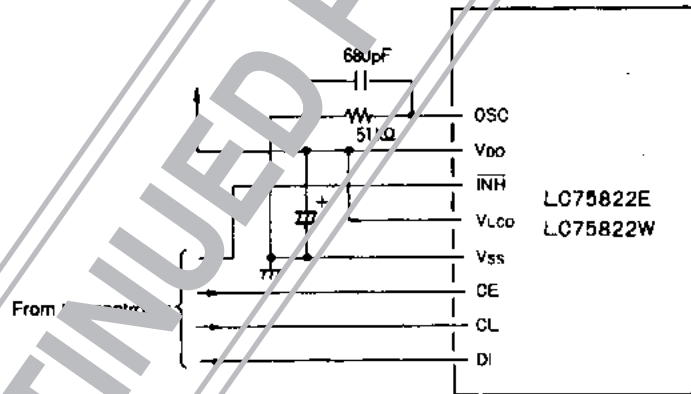


Note: The internal display data are undefined when power ($V_{DD}$) is first applied. Since a meaningless pattern will be displayed if the display is turned on in that state, the display should be turned off by setting $\overline{INH}$ low and turned on only after display data has been sent from the controller.

## Transfer (external Input) Data/Output Pin Correspondence

| DP / Output pin | 0 (1/1 duty) | 1 (1/2 duty) | COM1 | COM2 |
|---|---|---|---|---|
| S1 | D1 | D1 | O | |
|  |  | D2 | | O |
| S2 | D2 | D3 | O | |
|  |  | D4 | | O |
| S3 | D3 | D5 | O | |
|  |  | D6 | | O |
| ⋮ | ⋮ | ⋮ | | |
| S26 | D26 | D51 | O | |
|  |  | D52 | | O |
| S27 | D27 | D54 | O | |
|  |  | D55 | | O |
| S28 | D28 | D56 | O | |
|  |  | D57 | | O |
| ⋮ | ⋮ | ⋮ | | |
| S43 | D43 | D86 | O | |
|  |  | D67 | | O |
| S44 | D44 | D88 | O | |
|  |  | D89 | | O |
| S45 | D45 | D90 | O | |
|  |  | D91 | | O |
| S46 | D46 | D92 | O | |
|  |  | D93 | | O |
| S47 | D47 | D94 | O | |
|  |  | D95 | | O |
| S48 | D48 | D96 | O | |
|  |  | D97 | | O |
| S49 | D49 | D98 | O | |
|  |  | D99 | | O |
| S50 | D50 | D100 | O | |
|  |  | D101 | | O |
| S51 | D51 | D102 | O | |
|  |  | D103 | | O |
| S52 | D52 | D104 | O | |
|  |  | D105 | | O |
| S53 | D53 | Always on | O | |
|  |  | Always on | | O |

Note: Only COM1 is used in static (1/1 duty) drive.

## Oscillator Frequency

Refer to the figure below when determining the oscillator frequency.
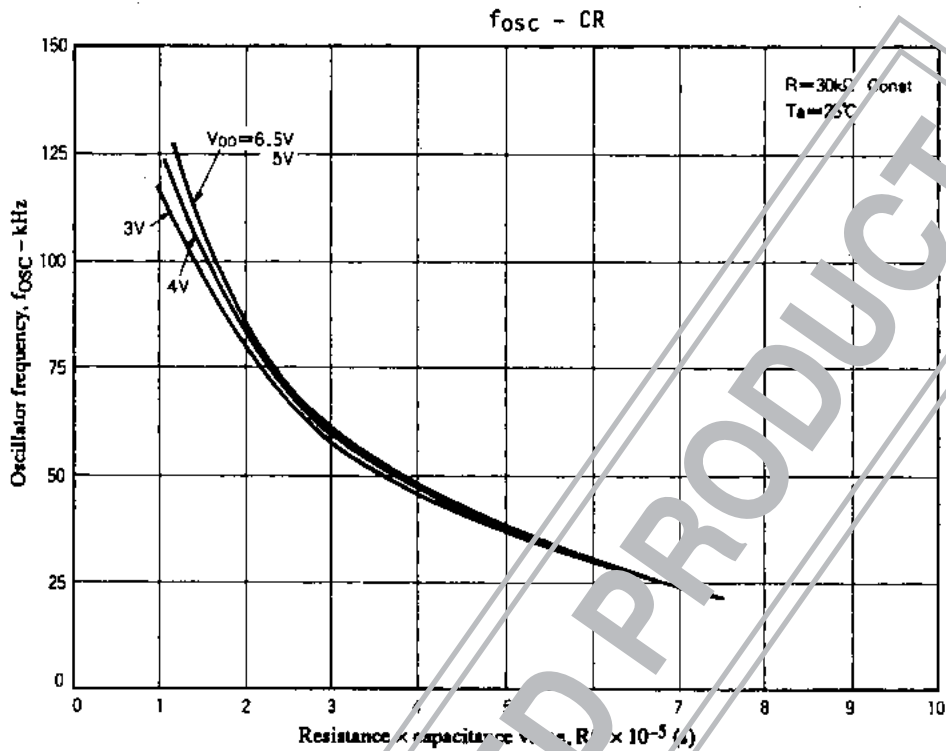


Figure 1   LC75822E, 75822W Oscillator Frequency vs. OSC Pin RC Constant
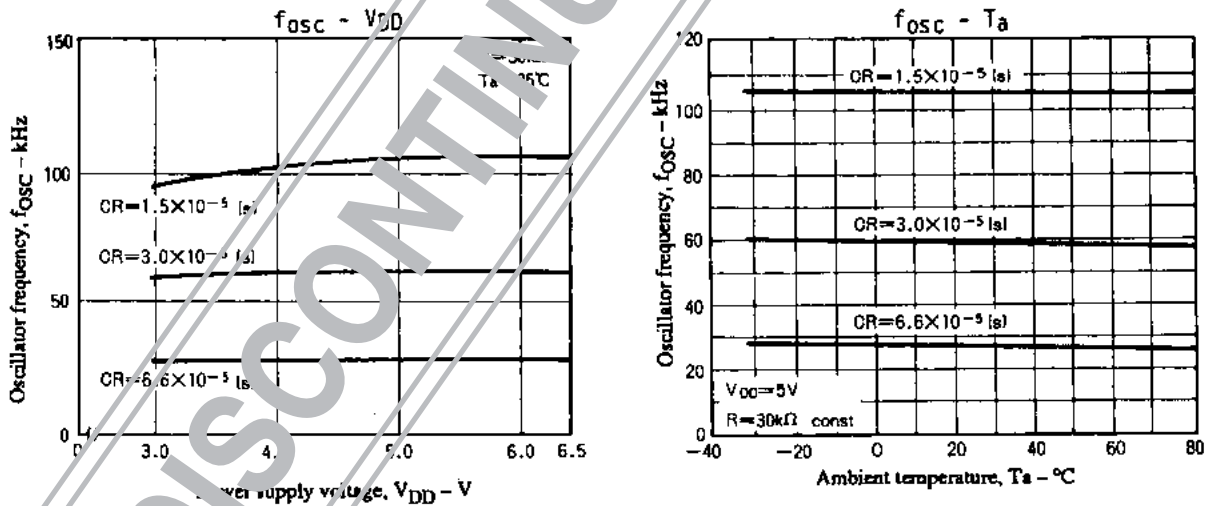


Figure 2  LC75822E, 75822W Oscillator Frequency vs. $V_{DD}$

Recommended range for external resistance:   10 to 100 kΩ (Carbon resistance)
Recommended range for external capacitance:  330 to 3300 pF
330 to 820 pF: (Ceramic capacitance with a zero temperature coefficient)
1000 to 3300 pF: (Mylar capacitance with a positive temperature coefficient)

DISCONTINUED PRODUCT