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Version 1.2, Aug 2004

# Datasheet

DS-CoreControl-TDA21107

TDA21107

Published by Infineon Technologies AG  
<http://www.infineon.com/DCDC>

**Power Management & Drive**



Never stop thinking.

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## High speed Driver with bootstrapping for dual Power MOSFETs



P-DSO-8

### Features:

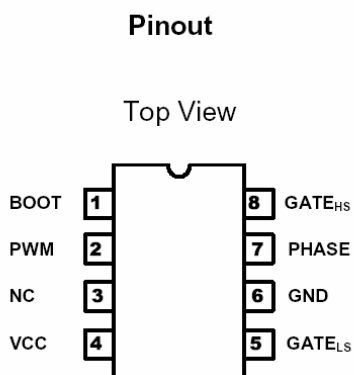
- Fast rise and fall times for frequencies up to 1 MHz
- Adjustable High Side MOSFET gate drive voltage via external voltage supply to BOOT for optimizing ON losses and gate drive losses ( 5V to 12V is recommended )
- Prevents from cross-conducting by adaptive gate drive control
- Supports shut-down mode for very low quiescent current through three-state input
- Compatible to standard PWM controller ICs (IFX, Intersil, Analog Devices, Richtek)
- Floating High Side MOSFET drive
- Power-on Overvoltage Protection
- Footprint compatible to ADP3418
- Ideal for multi-phase Desktop CPU supplies on motherboards and VRM's

### Application:

- Voltage Regulator Modules
- Low Output Voltage High Output Current DC-DC Converters
- Half-Bridge Class D Amplifier

Type	Package	Marking	Ordering Code
TDA21107	P-DSOP-8	21107	Q67042-S4251

### Pinout Drawing and Description:



Number	Name	Description
1	BOOT	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the high side N-Channel MOSFET
2	PWM	Input for the PWM signal from controller
3	NC	No Connection
4	VCC	Supply voltage
5	GATE <sub>LS</sub>	Gate drive output for the N-Channel Low Side MOSFET
6	GND	Ground
7	PHASE	To be connected to the junction of the High Side and the Low Side MOSFET
8	GATE <sub>HS</sub>	Gate drive output for the N-Channel High side MOSFET

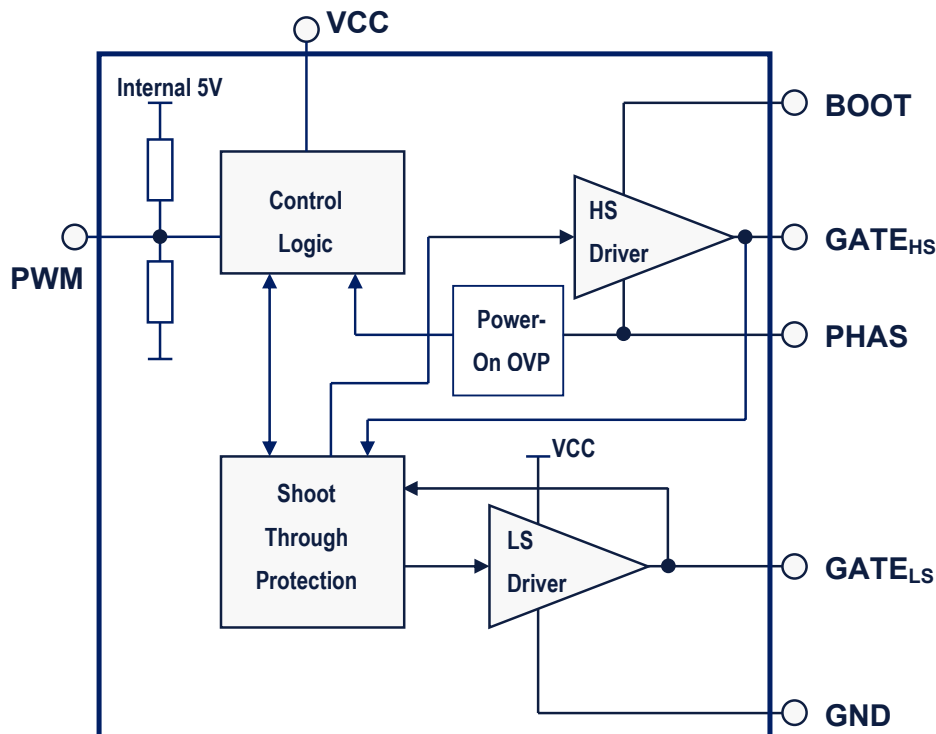
## General Description

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from PWM input pin to GATE<sub>HS</sub> and GATE<sub>LS</sub>, short rise and fall times and the same pin configuration as the ADP3418. In addition it provides several protection features as well as a shut down mode for efficiency reasons.

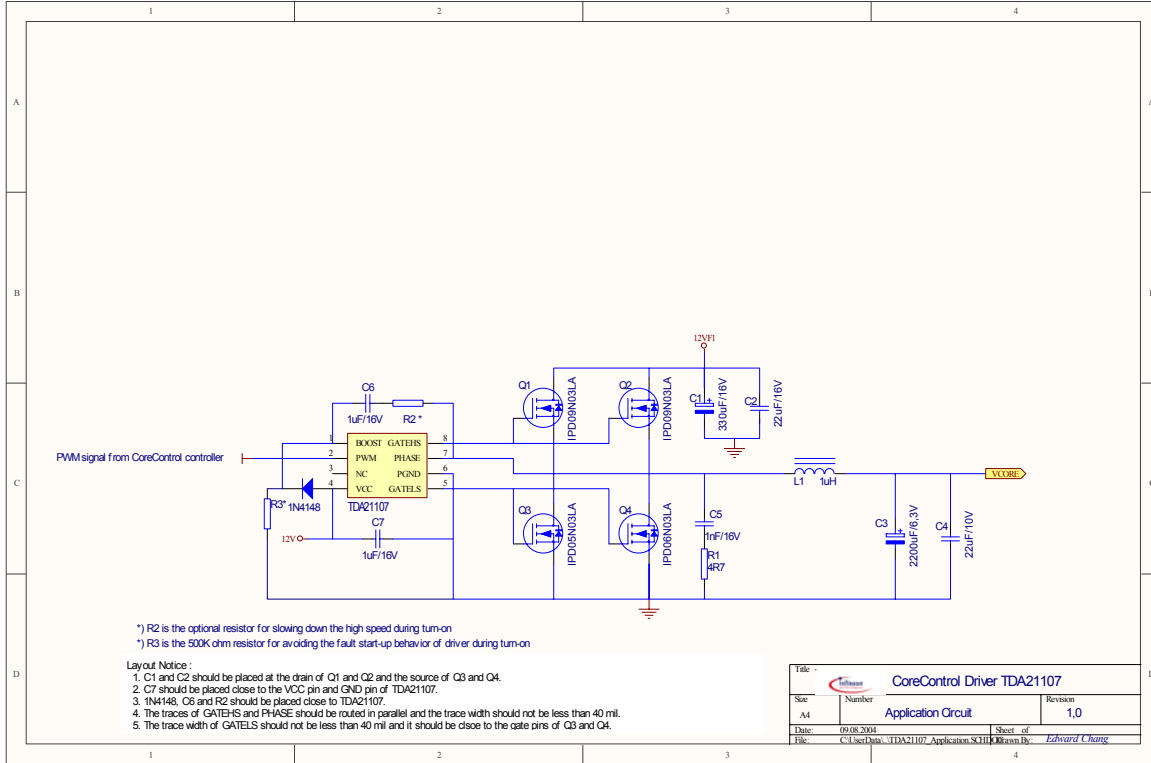
## Target application

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver's capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM's but also in motor drive and half bridge class-D amplifier type applications.

## Block Diagram



# Application Circuit



## Absolute Maximum Ratings

At  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Value		Unit
		Min	MAX	
Voltage supplied to 'VCC' pin; DC	$V_{VCC}$	-0.3	15	V
Voltage supplied to 'PWM' pin	$V_{PWM}$	-0.3	7	
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	$V_{BOOT} - V_{PHASE}$	-0.3	15	
Voltage supplied to 'BOOT' pin referenced to 'GND'	$V_{BOOT}$	-0.3	30	
Voltage rating at 'PHASE' pin,	$V_{PHASE}$	-4	15	
Voltage supplied to $GATE_{HS}$ pin referenced to 'PHASE'	$V_{GATEHS}$	$V_{PHASE} - 0.3$	$V_{BOOT} + 0.3$	
Voltage supplied to $GATE_{LS}$ pin referenced to 'GND'	$V_{GATELS}$	-0.3	$V_{VCC} + 0.3$	
Junction temperature	$T_J$	0	150	$^\circ\text{C}$
Storage temperature	$T_S$	-40	150	
Lead temperature (Soldering, 10 seconds)			260	
ESD Rating; Human Body Model			2	KV
Machine Mode			200	V
IEC climatic category; DIN EN 60068-1	55/150/56			

## Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-soldering point			90		K/W
Thermal resistance, junction-ambient			125		

## Operating Conditions

At  $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pins	$V_{VCC}$		10.8	12.0	13.2	V
Input signal transition frequency	f		50		500	KHz
Power dissipation	$P_{TOT}$	$T_A = 25\text{ }^\circ\text{C}$ , $T_J = 125\text{ }^\circ\text{C}$		0.8		W
Junction temperature	$T_J$		0		125	$^\circ\text{C}$
Ambient temperature	$T_A$		0		70	$^\circ\text{C}$



## Electrical Characteristic

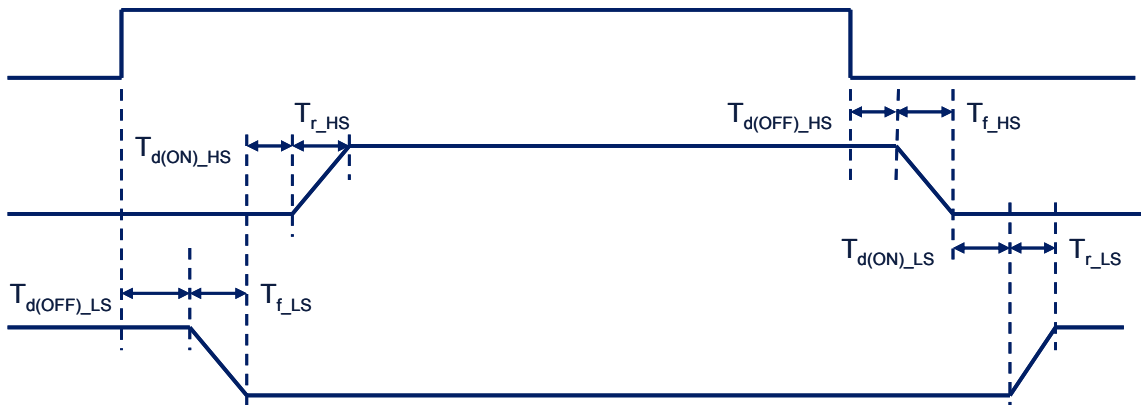
At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
<b>Supply Characteristic</b>						
VCC supply current	$I_{VCC}$	$V_{VCC} = 12\text{ V}$ $V_{PWM} = 0\text{ V}$		5	7	mA
Under-voltage lockout		$V_{VCC}$ rising threshold	8.6	9.4	10.2	V
Under-voltage lockout		$V_{VCC}$ falling threshold	7.25	8.05	8.85	
<b>Input Characteristic</b>						
Current in 'PWM' pin	$I_{PWM\_L}$	$V_{PWM} = 0\text{ V}$	-80	-110	-140	$\mu\text{A}$
Current in 'PWM' pin	$I_{PWM\_H}$	$V_{PWM} = 5\text{ V}$	80	110	140	
PWM pin open	$V_{PWM\_O}$		2.2	2.5	2.8	V
PWM Low level	$V_{PWM\_L}$		1.2	1.4	1.5	
PWM High level	$V_{PWM\_H}$		3.0	3.5	3.8	

At Tj = 25 °C, unless otherwise specified

Dynamic Characteristic						
Turn-on propagation Delay High Side	$t_{d(ON\_HS)}$	$P_{PVCC} = V_{VCC} = 12\text{ V}$ $C_{ISS} = 3000\text{ pF}$		40		ns
Turn-off propagation delay High Side	$t_{d(OFF\_HS)}$			30		
Rise time High Side	$t_{r\_HS}$			30		
Fall time High Side	$t_{f\_HS}$			40		
Turn-on propagation Delay Low Side	$t_{d(ON\_LS)}$			35		
Turn-off propagation delay Low Side	$t_{d(OFF\_LS)}$			30		
Rise time Low Side	$t_{r\_LS}$			30		
Fall time Low Side	$t_{f\_LS}$			30		

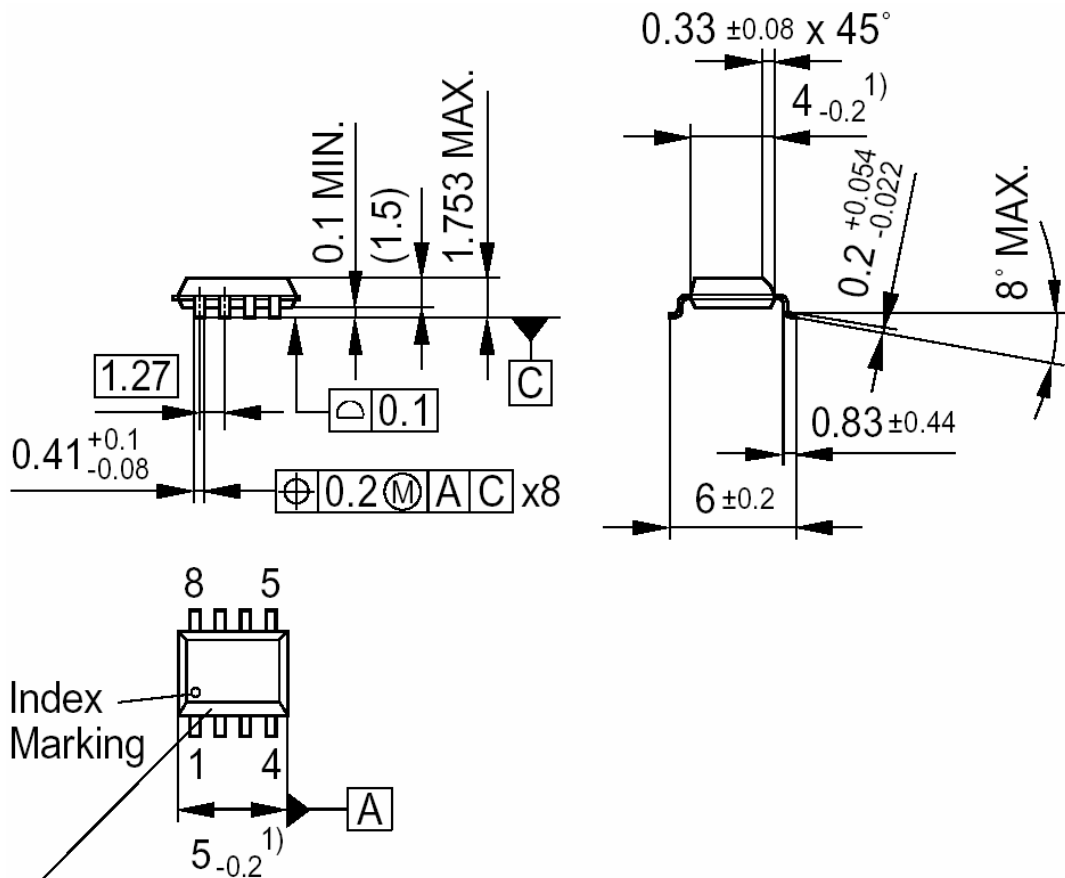
### Timing diagram



At Tj = 25 °C, unless otherwise specified

Parameter	Conditions	Values			Unit
		Min.	Typ.	Max.	
<b>Output Characteristic High Side (HS) and Low Side (LS), ensured by design</b>					
Output Reistance	HS; Source		2		$\Omega$
	HS; Sink		1.5		
	LS; Source	$V_{PVCC} = V_{VCC} = 12\text{ V}$	1.6		
	LS; Sink		1.2		

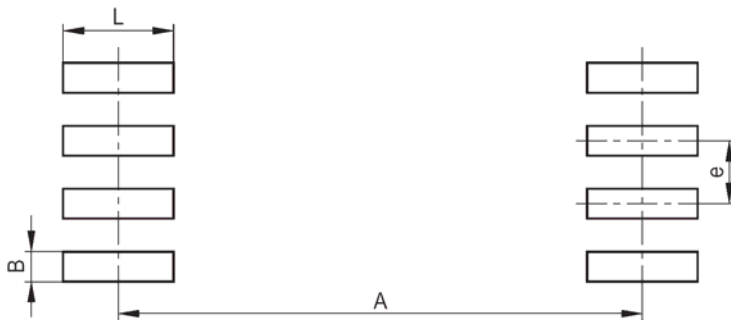
## Package Drawing P-DSO-8



Index Marking (Chamfer)

1) Does not include plastic or metal protrusion of 0.15 max. per side

## Footprint Drawing P-DSO-8



e	A	L	B
1.27 mm	5.69 mm	1.31 mm	0.65 mm

Revision History		
Datasheet DS-CoreControl-TDA21107		
Actual Release: V1.1 Date: 22.03.2005		Previous Release: V1.0 Date: 10.08.2004
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release
9	9	Add $t_{d(OFF)_{HS}} = 30 \text{ ns}$ and $t_{d(OFF)_{LS}} = 30 \text{ ns}$

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