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Panasonic

AN44150A

Realizing in One IC,
PWM Output Open Control by External PWM Signal and
PWM Output Loop Control by External DC Voltage and Current Peak Detection.

3-Phase Brushless Motor Drive IC

Features

- Supply voltage range: 6.0 V to 36 V
- Built-in 5-V regulator
- 3-phase 120-deg--energization drive system by 3-Hall-sensor
- Drive control mode is selectable:
  ·PWM open control by an external PWM signal (PWM through drive)
  ·PWM loop control by external DC voltage and current peak detection. (OFF time fixed current peak detection PWM drive)
- OFF time setting switching function
- Rotation direction switching function
- FG pulse switching function (1FG or 3FG)
- Short-brake/Free-running function
- Built in various protection functions: under voltage lock out (UVLO), thermal protection, motor restricted protection , overcurrent protection and drive output short protection

Applications

- Driver IC for 3-phase brushless motor

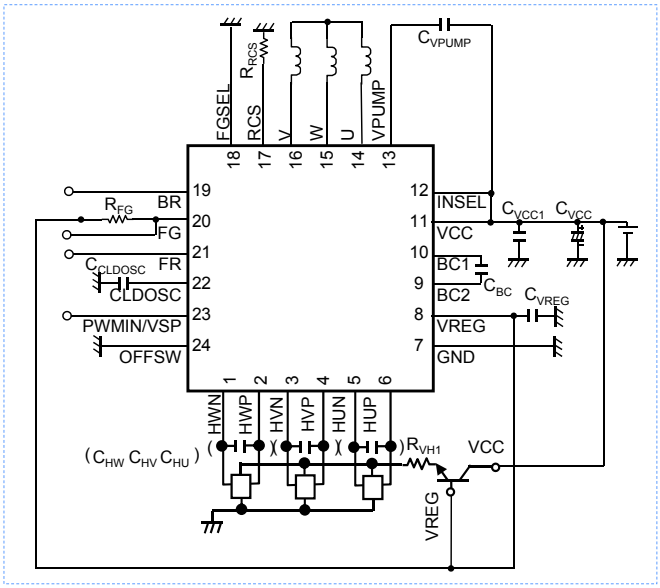
Package

- 24-pin plastic quad flat non-lead package (QFN type, size: 4 mm × 4 mm)

Summary

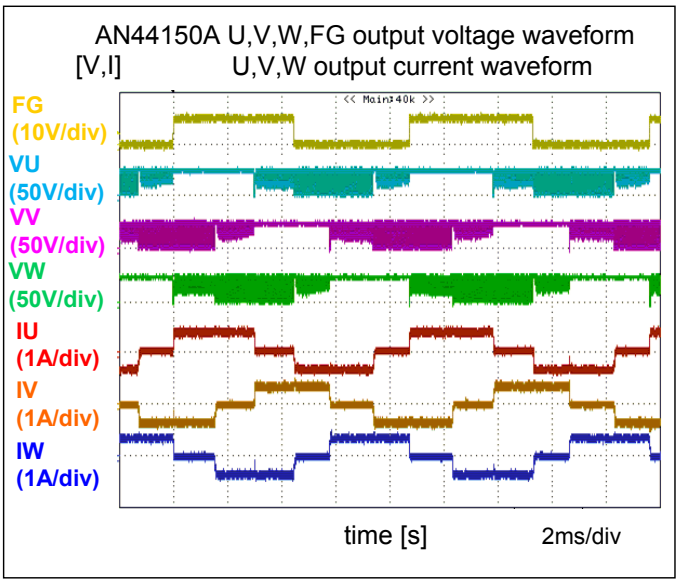
AN44150A is a driver IC for 3-phase brushless motor.
The rotor position detection by a 3-Hall-sensor and a 120-deg--energization drive system are adopted.
It is selectable the PWM through drive mode or the OFF time fixed current peak detection PWM drive mode.
Low power consumption of a motor module is realized, and it contributes to the application expansion of various motor units.

Application Circuit Example



Note: In the above circuit example, It's not that the operation of the volume production is guaranteed. When designing a mass production set, after having conducted an evaluation and verification enough, use it with the customer's responsibility.

Motor Drive Waveform



Conditions: PWMIN mode, PWMIN=20kHz, 50%duty
V_{CC} = 24 V, V_{FR} = H, FGSEL=L

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Absolute Maximum Rating

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{CC}	37	V	*1
Output current	Iu, Iv, Iw	±1.5	A	*1, *4
Operating ambient temperature	T_{OPR}	– 40 ~ + 80	°C	*2
Storage temperature	T_{STG}	– 55 ~ +150	°C	*2
Input voltage range	V_{OFFSW},V_{HUP},V_{HUN},V_{HVP}, V_{HVN},V_{HWP},V_{HWN},V_{BR}, V_{FR},$V_{PWMIN/VSP}$,V_{FGSEL}	– 0.3 ~ 6.0	V	—
	V_{INSEL}	– 0.3 ~ 37.0	V	—
Output voltage range	V_U, V_V, V_W	37	V	*1, *3
	V_{FG}	– 0.3 ~ 6.0	V	—
	V_{VREG},V_{RCS},V_{CLDOSC}	– 0.3 ~ 6.0	V	*3
	V_{BC1}	37	V	*3
	V_{BC2},V_{PUMP}	45	V	*3
Input current range	I_{FG}	0 ~10	mA	—
	I_{VREG}	0 ~ –10	mA	*4
ESD tolerance	MM	±200	V	—
	HBM	±2	kV	—

Notes:
If you give a stress above those listed under absolute maximum ratings, it is possible that permanent damage to the product. These are provisions for stress ratings, it is not guaranteed that functional operation of the device at the value greater than recommended operating range. When exposing to absolute maximum conditions for extended periods, it may affect the reliability of this product.
*1: It indicates when using in a range that does not exceed the absolute maximum rating, including the rated power consumption.
*2: Except the operating ambient temperature, and the storage temperature, all ratings are for Ta = 25 °C.
*3: Do not apply external voltage to these pins, and set them not to exceed the rated value even transitional.
*4: Do not apply external current to these pins, and set them not to exceed the rated value even transitional.

Rated Power Consumption

Package	θj-a	θj-c	P_D (Ta=25℃)	P_D (Ta=70℃)
24 pin Plastic Quad Flat Non-leaded Package (QFN type)	57.8°C/W	5.4 °C/W	2163mW	1384mW

Note:. For the actual usage, refer to the PD-Ta characteristics diagram in the package specification, follow the supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1: Glass-epoxy substrate (2 Layers) : 50×50×0.8t (mm) ,thermal via, back heat sink: Dai-pad , Soldered.

CAUTION
Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	V_{CC}	6.0	—	36	V	*1
Input voltage range	V_{INSEL}	0	—	V_{CC}	V	*1
	V_{OFFSW}	0	—	V_{VREG}	V	*1
	V_{FGSEL}	0	—	V_{VREG}	V	*1
	V_{RCS}	0	—	V_{VREG}	V	*1
	V_{BR}	0	—	V_{VREG}	V	*1
	V_{FR}	0	—	V_{VREG}	V	*1
	$V_{PWMIN/VSP}$	0	—	V_{VREG}	V	*1
External constants (reference)	C_{VCC}	—	47µ	—	F	*2
	C_{VCC1}	—	0.1µ	—	F	*2
	C_{VREG}	—	0.1µ	—	F	*2
	C_{BC}	—	0.01µ	—	F	*2
	C_{VPUMP}	—	0.01µ	—	F	*2
	C_{CLDOSC}	—	0.022µ	—	F	*2
	C_{HU}	—	0.01µ	—	F	*2
	C_{HV}	—	0.01µ	—	F	*2
	C_{HW}	—	0.01µ	—	F	*2
	R_{RCS}	0.16	0.27	—	Ω	*2 ,*3
	R_{FG}	—	51k	—	Ω	*2
	R_{VH1}	—	1k	—	Ω	*2

Notes:

*1 For the setting range of input control voltage, refer to the Electrical Characteristics, and the Functional Explanation.

*2 This value is an example. Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.

*3 A value less than this resistance is prohibited. If you set below this minimum value, there is a possibility that the output current exceeding rated current.

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Electrical Characteristics

at Vcc=24V,

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit current							
V_{CC} current	I_{CC1}	—	—	2.4	3.8	mA	
V_{CC} current at STBY mode	I_{CC2}	at STBY mode	—	350	700	uA	
Power block							
Output on-resistance	R_{ONHL}	I = ±1A (High side + Low side) Vcc=12V	0.7	1.14	1.55	Ω	
Output leak current	I_{PL}	—	—	10	50	uA	
Diode forward voltage	V_{DI}	I = 1A	—	1	1.6	V	
5V regulator block							
VREG voltage	V_{VREG}	—	4.7	5	5.3	V	
Voltage regulation	ΔV_{REG1}	Vcc=6 ~ 36V, Io=-5mA	—	20	50	mV	
Load regulation	ΔV_{REG2}	Io=-5m ~ -10mA	—	50	100	mV	
CLD oscillator circuit							
High level output voltage	V_{OHCLD}	Design target value	—	2.5	—	V	*2
Low level output voltage	V_{OLCLD}	Design target value	—	0.5	—	V	*2
Amplitude	V_{CLD}	—	1.3	2.0	2.7	Vpp	
External capacitor charge current	I_{CLD1}	Vcld=1.5V	-17.6	-12	-6.4	uA	
External capacitor discharge current	I_{CLD2}	Vcld=1.5V	6.4	12	17.6	uA	
Oscillation frequency	F_{CLD}	C=0.022uF (Design target value)	—	136	—	Hz	*2
Hall block							
Input bias current	I_{HALL}	—	– 2	0	2	uA	
Input dynamic range	V_{HALL}	—	0	—	VREG -1.7	V	
Hysteresis width	V_{OVhys}	—	9	20	35	mV	
Hysteresis level: L → H	V_{HYS1}	—	3	10	17	mV	
Hysteresis level: H → L	V_{HYS2}	—	-17	-10	-3	mV	
Hall input sensitivity	V_{HIN}	—	80	—	—	mV p-p	
Common-mode input voltage range	V_{ICM}	One side input bias	0	—	VREG	V	

Notes : *2 Typical design value

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Electrical Characteristics (continued)

at Vcc=24V,

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Charge pump output							
Output boosted voltage	V_{PUMP}	Ipump=0mA	V_{CC} +5	V_{CC} +7	V_{CC} +9	V	
VCC under voltage lock out							
Operation voltage	V_{UVLO}	—	4.5	4.8	5.1	V	
Hysteresis width	ΔV_{UVLO}	—	0.1	0.2	0.3	V	
Current limiter operation							
Limiter voltage	V_{RF}	INSEL=H	0.19	0.21	0.23	V	
FG Block							
Output on-resistance	V_{ONFG}	I_{FG}=5mA	-	40	60	Ω	
Output leak current	I_{LFG}	Vo=5V	-	-	10	uA	
BR Interface							
High level input voltage	V_{THBR}	—	2.0	—	VREG	V	
Low level input voltage	V_{TLBR}	—	0	—	1	V	
Input open voltage	V_{IOBR}	—	2.65	3	3.35	V	
Hysteresis width	V_{ISBR}	—	0.25	0.33	0.4	V	
High level input current	I_{IHBR}	V_{BR}=5V	45	60	75	uA	
Low level input current	I_{ILBR}	V_{BR}=0V	-60	-80	-100	uA	
FR Interface							
High level input voltage	V_{THFR}	—	2.0	—	VREG	V	
Low level input voltage	V_{TLFR}	—	0	—	1	V	
Input open voltage	V_{IOFR}	—	2.65	3	3.35	V	
Hysteresis width	V_{ISFR}	—	0.25	0.33	0.4	V	
High level input current	I_{IHFR}	V_{FR}=5V	45	60	75	uA	
Low level input current	I_{ILFR}	V_{FR}=0V	-60	-80	-100	uA	

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Electrical Characteristics (continued)

at Vcc=24V,

Note: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
PWMIN Interface (Switching by PWMIN/VSP pin, at INSEL=H)							
High level input voltage	V_{THPWMI}	—	2.0	—	VREG	V	
Low level input voltage	V_{TLPWMI}	—	0	—	1	V	
Input open voltage	V_{IOPWMI}	—	2.65	3	3.35	V	
Hysteresis width	V_{ISPWMI}	—	0.25	0.33	0.4	V	
High level input current	I_{IHPWMI}	V_{PWMIN}=5V	45	60	75	uA	
Low level input current	I_{ILPWMI}	V_{PWMIN}=0V	-67	-90	-113	uA	
Recommended input frequency	F_{PWMIN}	Design recommended value	0.5	—	60	kHz	
INSEL Interface							
High level input voltage	V_{INSELH}	—	VCC - 1	—	VCC	V	
Low level input voltage	V_{INSELL}	—	0	—	1	V	
FGSEL Interface							
High level input voltage	V_{FGSELH}	—	VREG - 1	—	VREG	V	
Low level input voltage	V_{FGSELL}	—	0	—	1	V	
OFFSW Interface							
High level input voltage	V_{OFFSWH}	—	VREG - 1	—	VREG	V	
Low level input voltage	V_{OFFSWL}	—	0	—	1	V	
VSP Interface (Switching by PWMIN/VSP pin, at INSEL=L)							
Input dynamic range L level	V_{SPDL}	—	0.8	1	1.2	V	
Input dynamic range H level	V_{SPDH}	—	2.25	2.5	2.75	V	
Input to output gain	V_{SPG}	VSP=1.3 ~ 2.2V	0.126	0.14	0.154	V/V	
Threshold voltage of free-run comparator	V_{FRC}		0.8	0.9	1.0	V	
OFF time1	V_{OFFT1}	OFFSW=H	1.1	2.2	3.5	us	
OFF time2	V_{OFFT2}	OFFSW=L	4.2	7.0	11	us	
Thermal protection							
Thermal shutdown operation temperature	TSD	Design target value	-	160	-	℃	*1
Hysteresis width	ΔTSD	Design target value	-	40	-	℃	*1

Notes : *1 These are values checked by design but not production tested.

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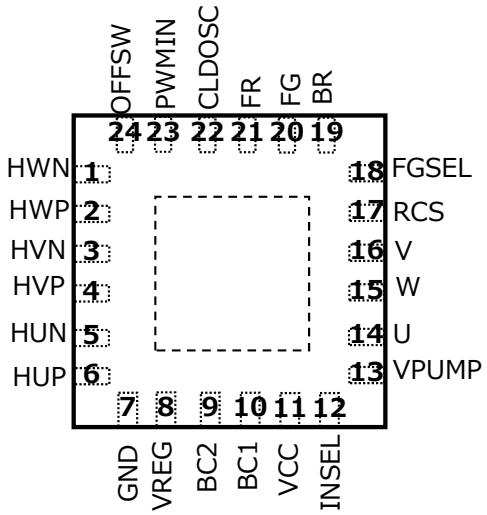
■ Pin Configuration

TOP VIEW



Pin Functions

Pin No.	Pin name	Type	Description
1	HWN	Input	Hall amplifier input W (-), Connected to the output pin of the Hall element.
2	HWP	Input	Hall amplifier input W (+), Connected to the output pin of the Hall element.
3	HVN	Input	Hall amplifier input V (-), Connected to the output pin of the Hall element.
4	HVP	Input	Hall amplifier input V (+), Connected to the output pin of the Hall element.
5	HUN	Input	Hall amplifier input U (-), Connected to the output pin of the Hall element.
6	HUP	Input	Hall amplifier input U (+), Connected to the output pin of the Hall element.
7	GND	GND	Ground
8	VREG	Output	Internal reference voltage (5V)
9	BC2	Output	For charge pump 2, Capacitor is connected between BC1 and BC2
10	BC1	Output	For charge pump 1, Capacitor is connected between BC1 and BC2
11	VCC	Power Supply	Supply voltage for IC and motor.
12	INSEL	Input	PWMIN or VSP mode selection pin
13	VPUMP	Output	Charge pump voltage output
14	U	Output	U-phase output
15	W	Output	W-phase output
16	V	Output	V-phase output
17	RCS	Output	Motor current limit (PWMIN mode) / Motor current detector (VSP mode)
18	FGSEL	Input	FG output mode selection
19	BR	Input	Brake mode selection
20	FG	Output	FG external output
21	FR	Input	Forward / Reverse rotation direction selection
22	CLDOSC	Input	Setting oscillation frequency of motor restricted protection
23	PWMIN/VSP	Input	PWM input (PWMIN mode) or DC voltage input (VSP mode) for motor control
24	OFFSW	Input	PWM OFF time selection

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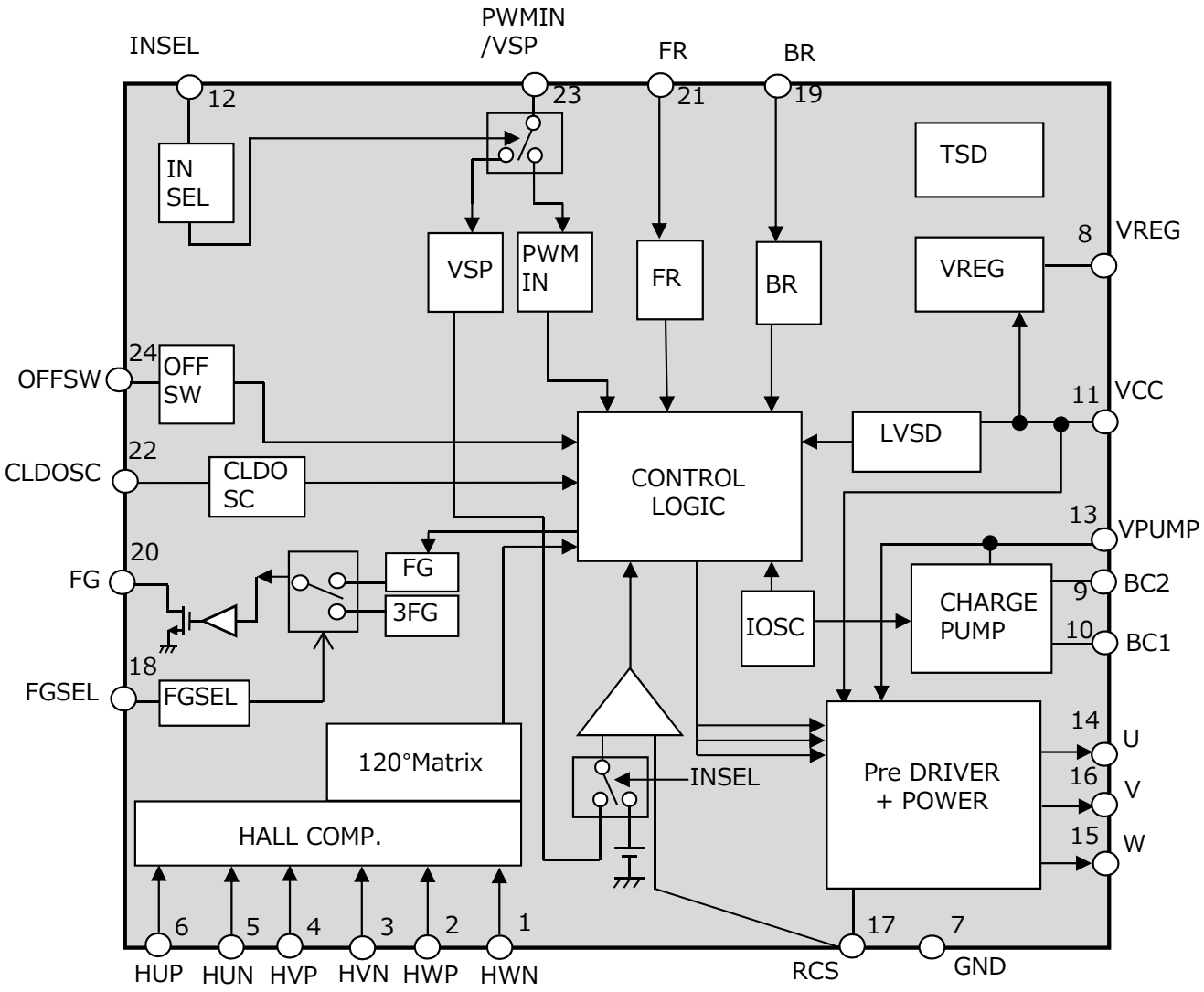
■Block diagram



Note: This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

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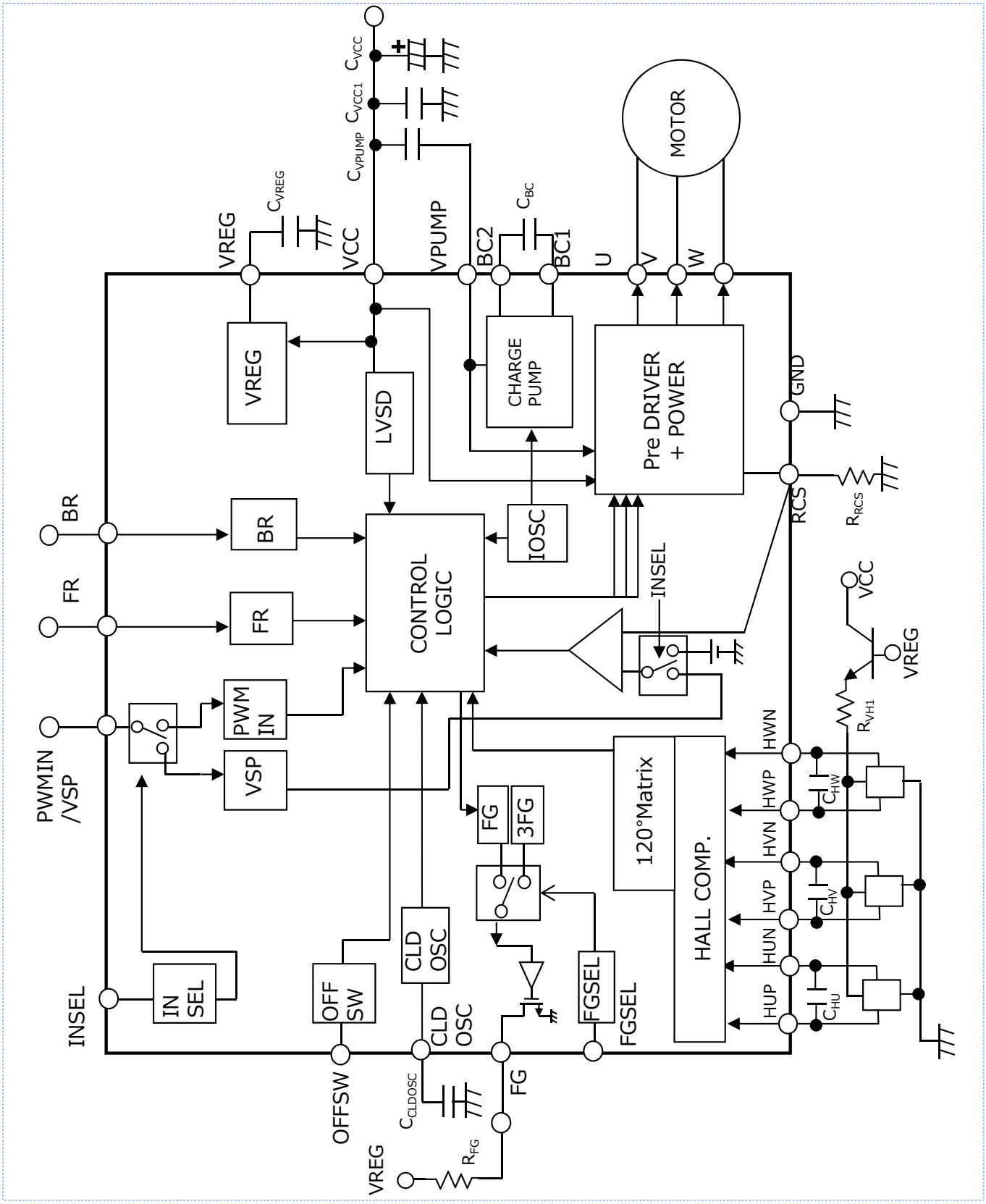
■Application Circuit Diagram



Note: ·This simplified application circuit is not guaranteed the operation of mass production set.
Use this IC after sufficient evaluation and examination on customer responsibility when designing the set.
·For the feature explanation, this block diagram may be partially omitted or simplified.

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■ Functional Pin Table

1. Selection of PWMIN mode or VSP mode（selectable by INSEL pin）			
Pin name	Input	Status	Description
INSEL	H(VCC)	PWMIN mode	External PWM signal is input and the PWM through drive mode which carries out open control of the output is chosen.
	L(GND)	VSP mode	External DC voltage is input and the OFF time fixed PWM drive mode which carries out loop control of the output by current peak detection is chosen.
2. Selection of FG output			
FGSEL	H(VREG)	3FG	3FG pulse output
	L(GND)	1FG	1FG pulse output
3. Selection of Fixed OFF time			
OFFSW	H(VREG)	OFF time 1	2.2u sec
	L(GND)	OFF time 2	7.0u sec
4. Function of Brake			
BR	H or Open	SBRK	Low side : Short brake
	L	Normal	Normal drive.
5. Function of Forward/Reverse			
F/R	H or Open	Forward	Rotation U→V→W
	L	Reverse	Rotation W→V→U

6. PWMIN/VSP pin input.			
Selection mode	Pin condition	Drive mode	Description
PWMIN mode (INSEL=H) →PWM signal input	PWM signal input	Normal Drive	An output power transistor is made to drive by the frequency and duty of an input PWM signal. PWMIN=L → Low side power : ON PWMIN=H → Low side power : OFF
	0% duty input	Free Run	If H level mode of an input PWM signal is continued in about 5 msec, it judges with duty 0% and will be in a free-run mode.
VSP mode (INSEL=L) →DC voltage input	VSP voltage of 1V to 2.5V is input.	Normal Drive	The input range of VSP voltage is 1V to 2.5V. It is made to drive by the current peak detection according to VSP voltage and the resistance of the RCS pin.
	VSP<0.9V	Free Run	It will be in a free-run mode by VSP<0.9V.
	VSP>2.5V	MAX Drive	It drives in the mode of VSP=2.5V.

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■Protection Function

Function name	Operate	Release	Note
TSD	160℃	120℃	All phases are OFF while protection function works. (output = HiZ) Moreover, when the TSD protection operates, the timer count of a restricted protection is made to stop.
Current limit (at PWMIN mode)	0.21V	After fixed time progress	In PWM through drive mode, if motor current reaches the current value decided by the resistance connected to the RCS pin and the internal reference voltage of 0.21V, output current will be restricted in turning off an output for a fixed time. OFF time can be decided by setting of an OFFSW pin. (OFFSW=H : 2.2usec, OFFSW=L : 7.0usec)
UVLO (VCC)	4.8V	5.0V	It is protection of the low-voltage condition of the power supply voltage. If protected operation is carried out, low side output power is turned on and it becomes a low side short brake.
Motor restricted protection	When FG pulse does not change within a set time. (latch protection)	・F/R operation ・at UVLO ・to STBY mode ・BR operation ・at TSD (count stop)	The count for restricted protection is made to stop at the time of TSD protected operation. Protection release and a count are reset except above. A protection setting time is determined by the external capacity value connected to the CLDOSC pin. (Time(s) = External Cap(uF) × 85)
Short protection of Motor output - GND,VCC	latch protection by constant time detection.	・at UVLO ・to STBY mode	Latch protection is carried out. Release is performed by UVLO and STB.

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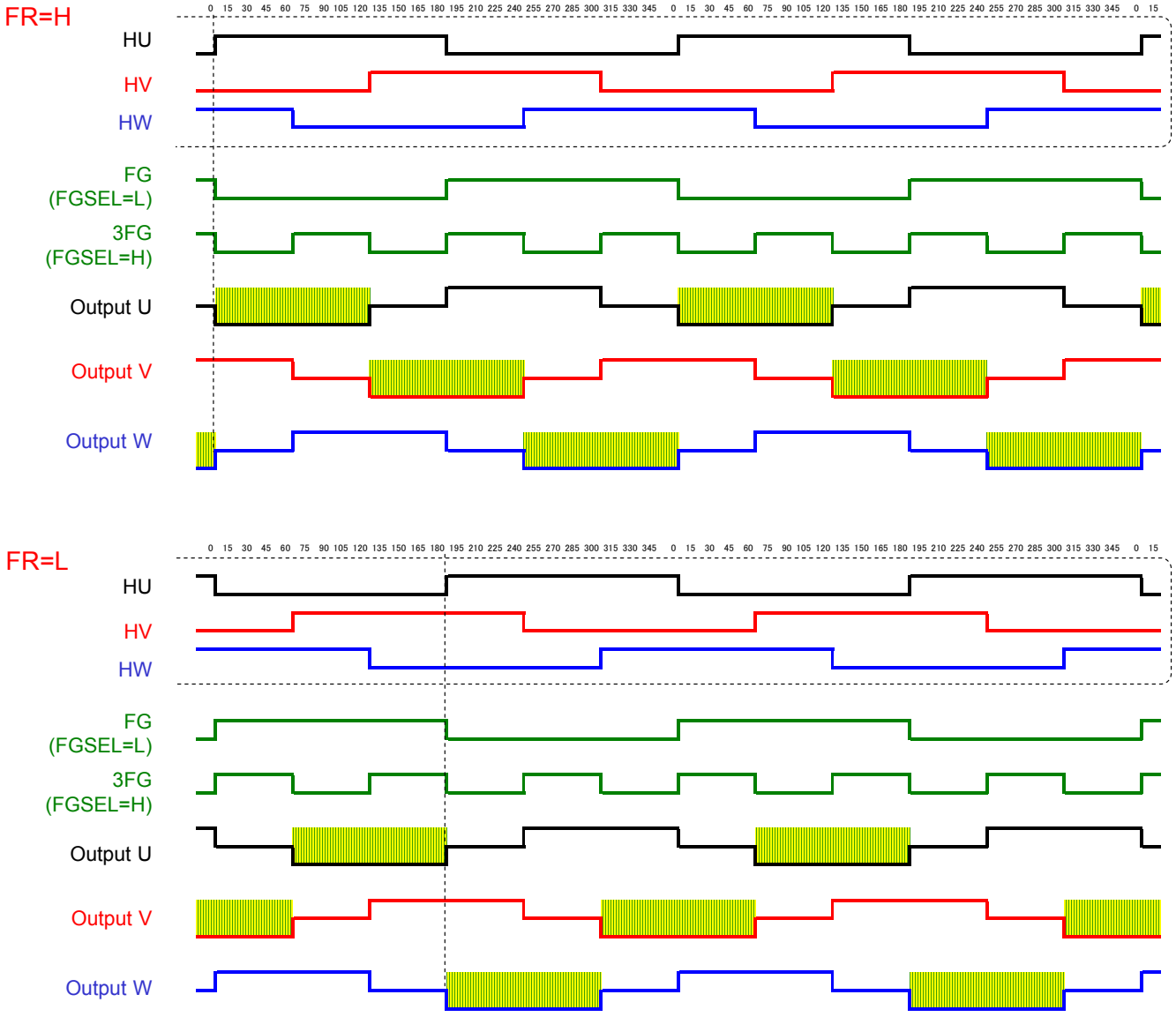
■3 Phase Drive State Diagram



FR=H			FR=L			OUTPUT		
HU	HV	HW	HU	HV	HW	U	V	W
H	L	H	L	H	L	PWM	H	Z
H	L	L	L	H	H	PWM	Z	H
H	H	L	L	L	H	Z	PWM	H
L	H	L	H	L	H	H	PWM	Z
L	H	H	H	L	L	H	Z	PWM
L	L	H	H	H	L	Z	H	PWM

■ As for FG output, the inversion signal of HU is output.

HU, HV, and HW = H show the following state, respectively.
HUP > HUN,
HVP > HVN,
HWP > HWN.

About the output U, V, and W,
As for H, output high side power is ON,
As for PWM, output power is a switching mode,
As for Z, output power is OFF,
It is shown.

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Functional Explanation

1. Selection of PWMIN mode or VSP mode

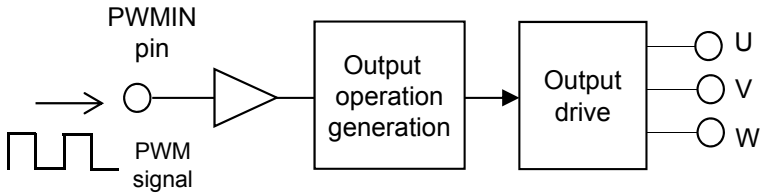
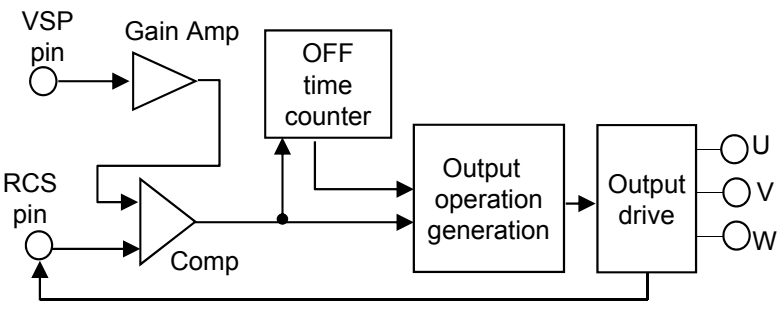
As a motor drive mode, it features two modes in this IC.
The mode selection is selectable by INSEL pin.

INSEL=H → PWMIN mode
INSEL=L → VSP mode

PWMIN mode・・・ This mode is the mode which inputs a PWM signal into a PWMIN/VSP pin and makes an output drive with the signal.
It is the open control drive of a PWM through system.

VSP mode・・・・・・DC voltage is input into a PWMIN/VSP pin and it operates in the fixed OFF time current peak detection PWM drive mode which makes it drive with carrying out current detection in a RCS pin.
It is the loop control by current peak detection.

Moreover, opening of the INSEL pin is prohibited.
Be sure to apply voltage to the pin so that the polarity can be decided.

Drive mode	PWM system	PWM generation	Summary block diagram
PWM IN mode	PWM through	PWMIN = PWM OUT	
VSP mode	Fixed OFF time	ON Timing :Fixed OFF time progress OFF Timing :Setting current value detection	

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Functional explanation (continued)

2. Start Up/Free Run/Standby(STB) mode

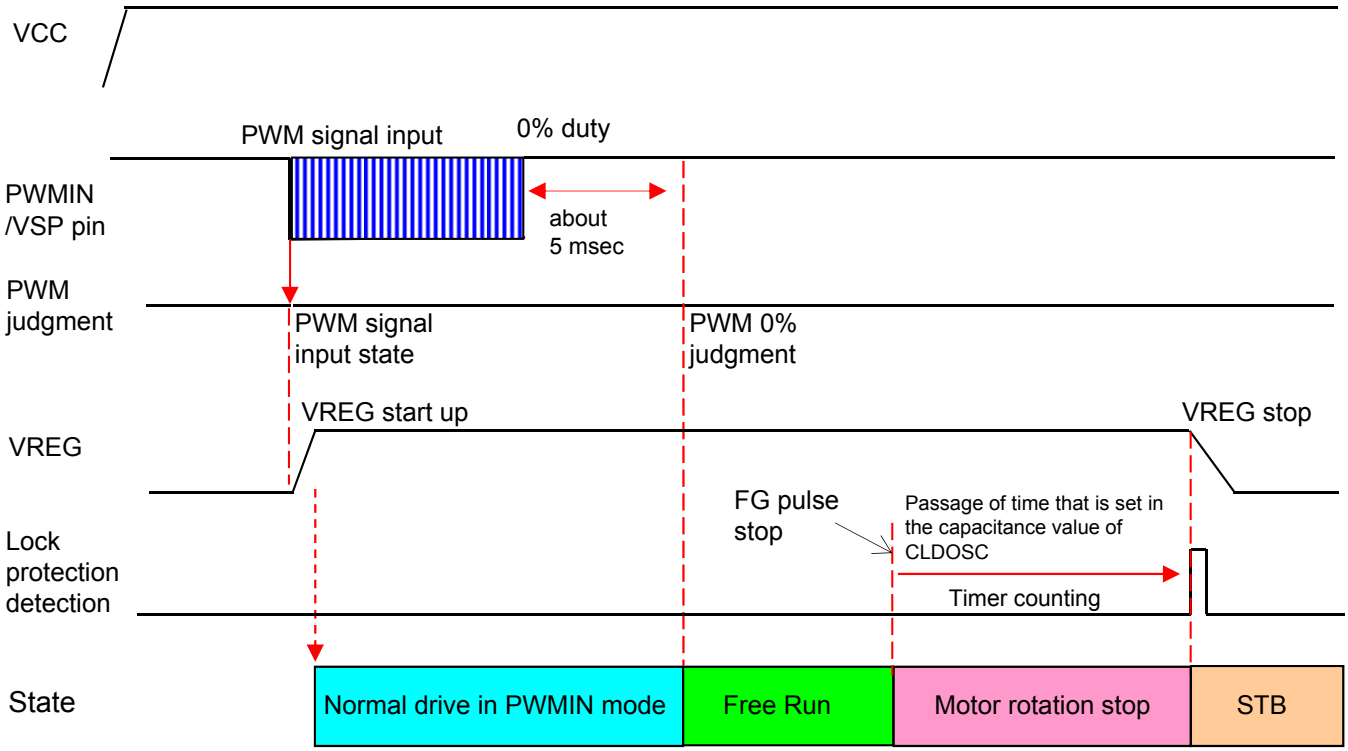
・In this IC, the transition conditions to Start Up, Free Run and STB mode are shown.

・PWMIN mode

Start Up・・・・ After applying the VCC of power supply within the operation limits, if a PWM signal is input from a PWMIN/VSP pin, a PWM input is judged and internal VREG voltage circuit starts. If it becomes the VREG voltage on which the internal circuit can operate, it becomes a normal drive in the PWMIN mode.

Free Run・・・ If the 0% duty mode (H level) of a PWM signal continues in about 5 msec, it judges as a PWM 0% inside IC, and becomes Free Run mode. At the time of Free Run, low side power outputs are all OFF, and high side power output of the detection phase of a hole is in ON state.

STB・・・・・・・・After a Free Run, rotation of a motor is stopped, FG pulse is no longer output, time that is decided by capacity value connected to the CLDOSC pin elapses, it transits to STB mode. Internal VREG voltage is stopped in the STB mode.



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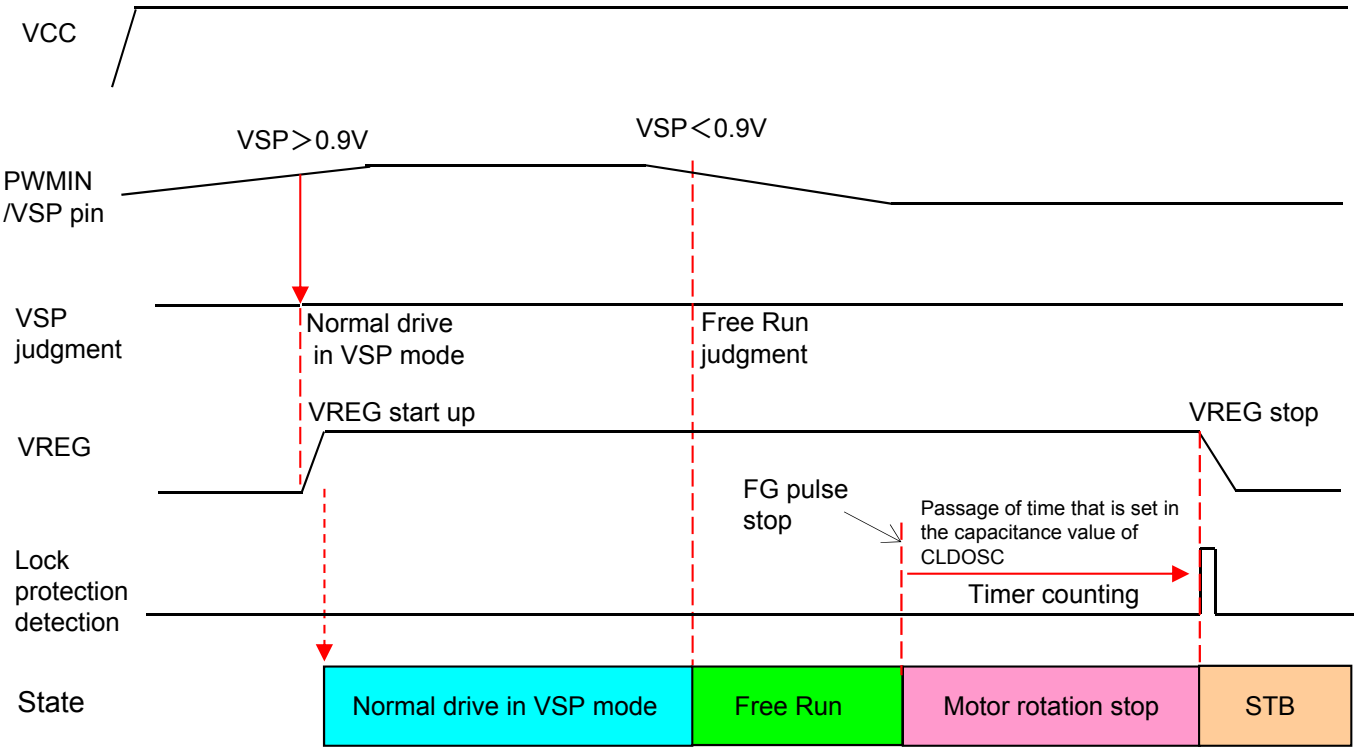
Functional Explanation (continued)

・VSP mode

Start Up・・・・After applying the VCC of power supply within the operation limits, if the voltage of 0.9V or more from PWMIN/VSP pin is input, it is judged as normal drive, and internal voltage circuit starts. If it becomes the VREG voltage on which the internal circuit can operate, it becomes a normal drive in the VSP mode. (However, VSP voltage input range of VSP mode is 1V to 2.5V.)

Free Run・・・If PWMIN/VSP pin voltage becomes 0.9V or less, it is judged as free-run in the IC, and it becomes Free Run mode.
At the time of Free Run, low side power outputs are all OFF, and high side power output of the detection phase of a hole is in ON state.

STB・・・・・・・ After a Free Run, the rotation of the motor is stopped . From the time the FG pulse is not detected, after the time elapses that is determined by the capacitance value connected to the terminal CLDOSC, it transits to the STB mode. And it stops the internal VREG voltage in the STB mode.



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Functional Explanation (continued)

3. Speed control

・PWMIN mode (INSEL=H)

By inputting a PWM signal to PWMIN/VSP pin and controlling its duty, it controls the output.

PWMIN/VSP pin:
L level voltage input → PWM phase (Low side) output ON
H level voltage input → PWM phase (Low side) output OFF

In the PWMIN mode, if the input PWM signal voltage continues in about 5 msec, it judges as 0% duty, and transits to Free Run mode.

・VSP mode (INSEL=L)

By inputting the DC voltage to PWMIN/VSP pin and controlling the voltage, it controls the motor current.
VSP mode is OFF time constant current peak detection system. By setting a target current value, make the loop control to match its value.

$$\text{Target current value(A)} = \frac{(\text{VSP input voltage} - 1) \times 0.14\ (\text{V})}{\text{RCS external resistance value}\ (\Omega)}$$

Input voltage range of VSP in normal drive of VSP mode is 1V to 2.5V.
When VSP voltage is 0.9V or less, it becomes Free Run mode.
If you input more than 2.5V voltage to VSP, it is set to 2.5V in the IC.

Functional Explanation (continued)

4. Motor restricted protection circuit

When FG non-signal state continues for a certain period of time in the motor normal operation mode, restricted protection circuit operates.
In the restricted protection mode, low side power outputs are in 3-phase OFF state.
The value of the restricted protection time can be calculated by the following equation approximately.

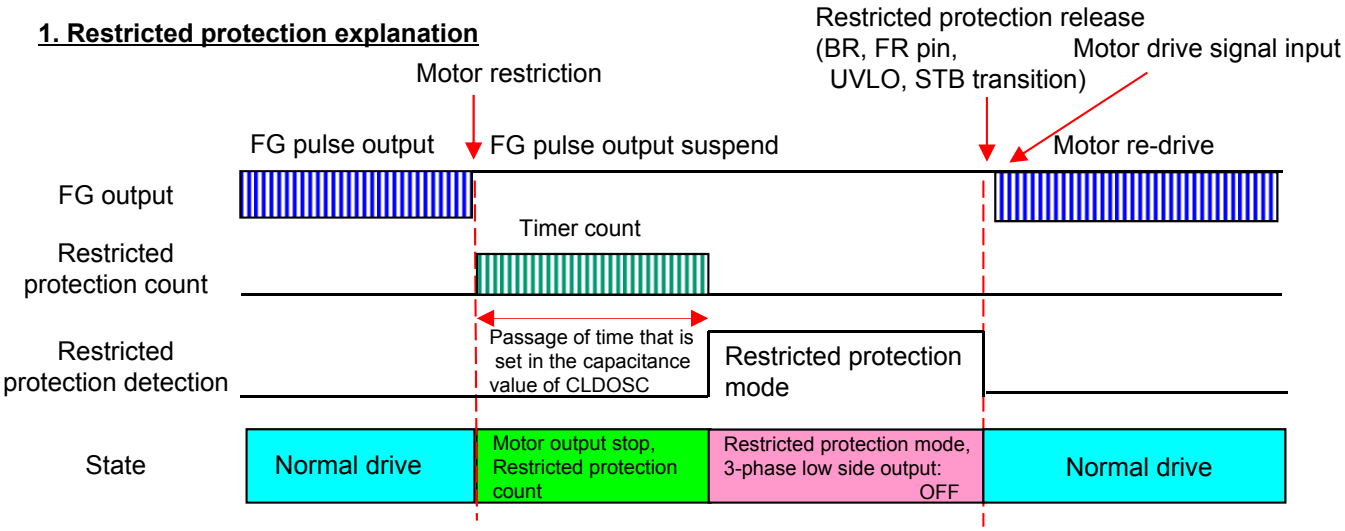
Restricted protection setting time (s) ≒ Capacitance value of CLDOSC (uF) x 85

If you connect capacitance of 0.047uF in CLDOSC pin, the restricted protection time is about 4s.
Make setting with a margin for motor start-up time.

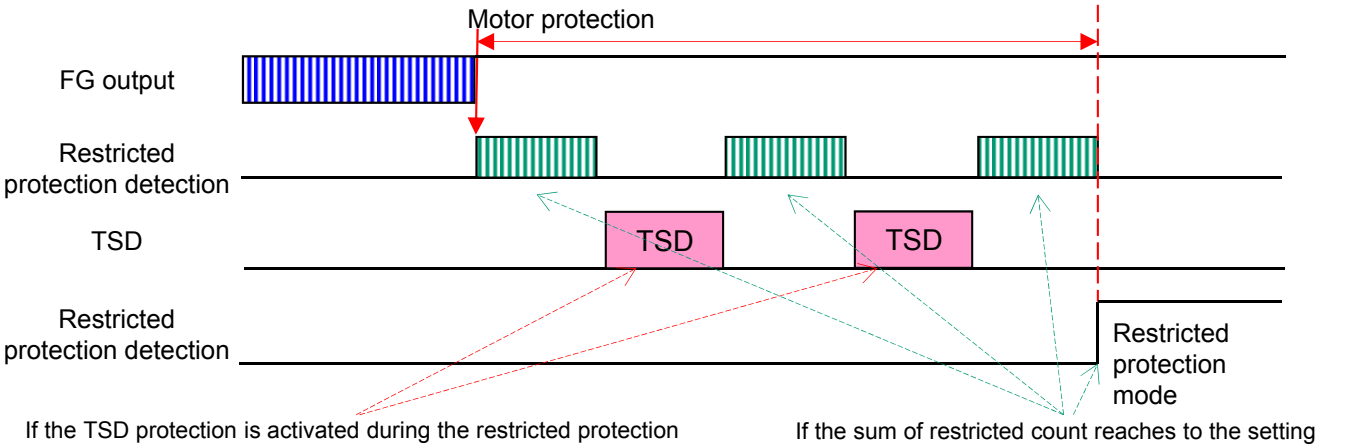
Conditions to release the motor restricted protection, and to reset the counter are as follows.
- BR pin: Short brake setting
- In switching the FR pin
- In detecting UVLO mode
- In transiting to STB mode
- at TSD protection (count stop)

This setting time is used as the time from free-run, stopping motor, until entering STBY mode.
If you do not use the restricted protection, connect the CLDOSC pin to the GND. (However, It will not be able to transit to the STBY mode.)

1. Restricted protection explanation



2. Restricted protection explanation in operating TSD protection



If the TSD protection is activated during the restricted protection count, it stops the restricted protection count during the protection.

If the sum of restricted count reaches to the setting time, it transits to the Restricted protection mode.

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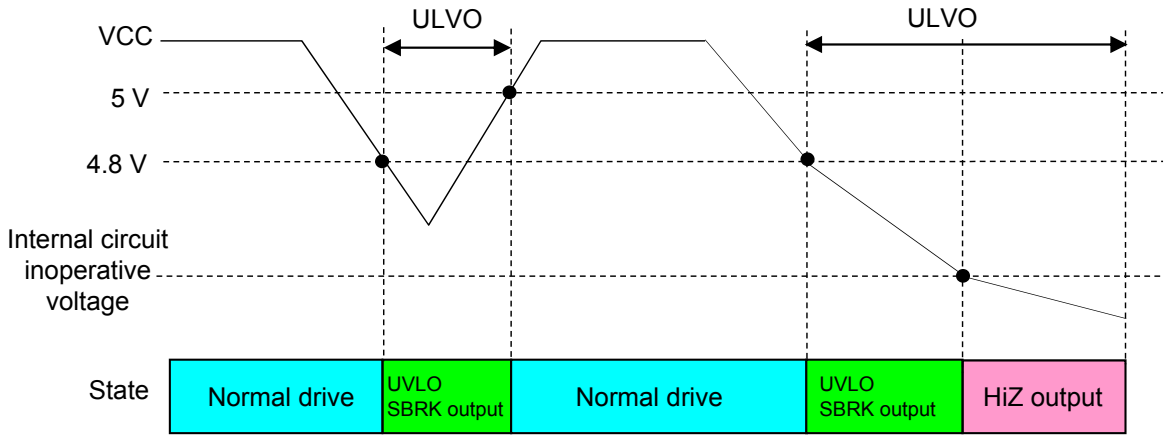
Functional Explanation (continued)

5. Low voltage protection

This IC monitors the voltage VCC. If VCC voltage becomes 4.8V or less, low-voltage protection is activated.
In the low voltage protection operation, the output of each phase is in Short-circuit braking mode (low side short).

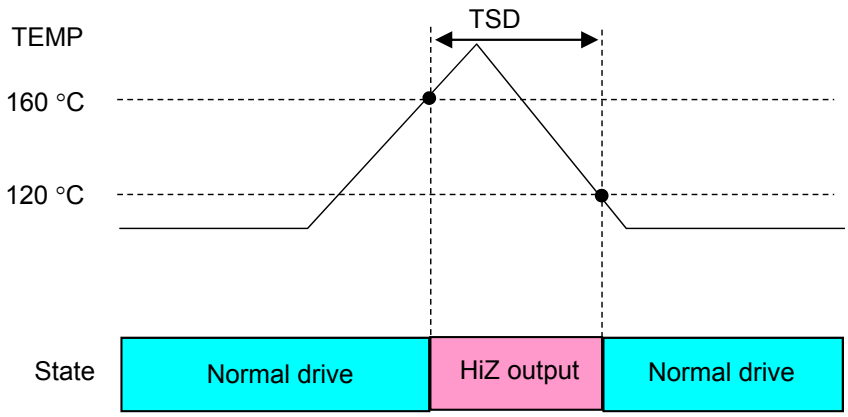
In addition, if the VCC voltage drops further, the internal circuit is no longer working properly, the outputs, all phases are HiZ (all phases OFF).

Hysteresis of 0.2V is set in the VCC low voltage protection function. If the VCC is restored to 5V from protection mode, the low voltage protection is released.



6. Thermal protection (TSD)

If an IC junction temperature is 160℃ (design target value) or more, the thermal protection is activated, and the motor outputs are all HiZ (all phases OFF).
If the IC junction temperature is 120℃ (design target value) or less, the protection is released. During the period of TSD protection, the count of the restricted protection circuit is stopped.



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Functional Explanation (continued)

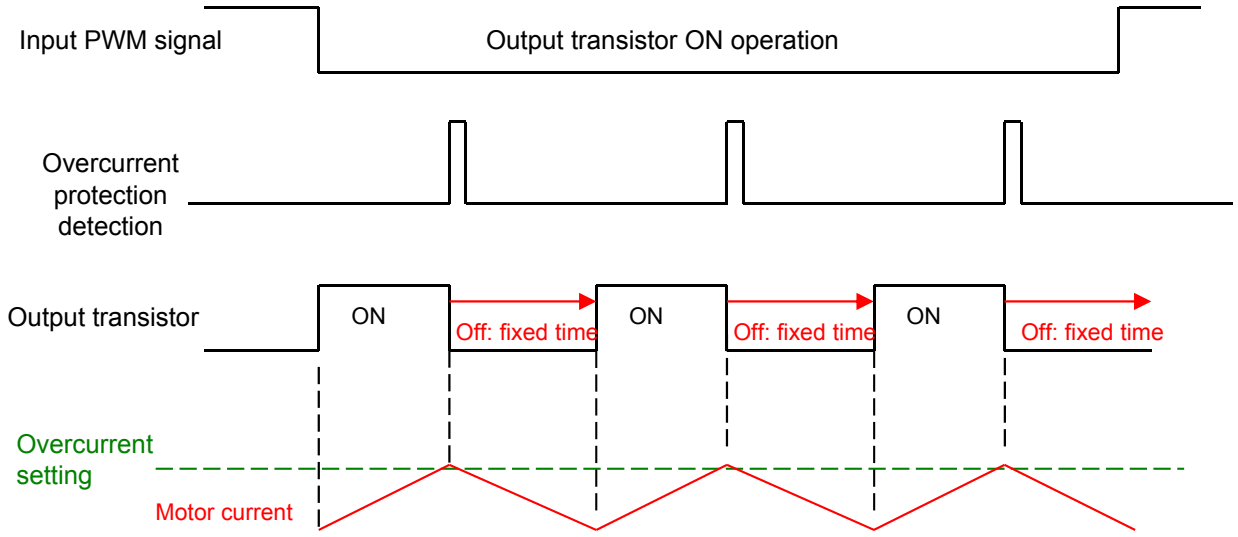
7. Overcurrent protection (PWMIN mode)

Here, describes the overcurrent protection setting in PWMIN mode.
Overcurrent setting value is determined by the resistance value connected to the RCS pin.

Overcurrent setting value (A) = 0.21 (V) / RCS resistance value (Ω)

After detecting a current greater than the setting value, by shutting off the output transistor during the predetermined time, it protects an over-current.

Off time is possible to switch using OFFSW pin.
OFFSW=H: Off time 2.2 usec
OFFSW=L: Off time 7.0 usec



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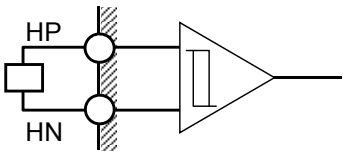
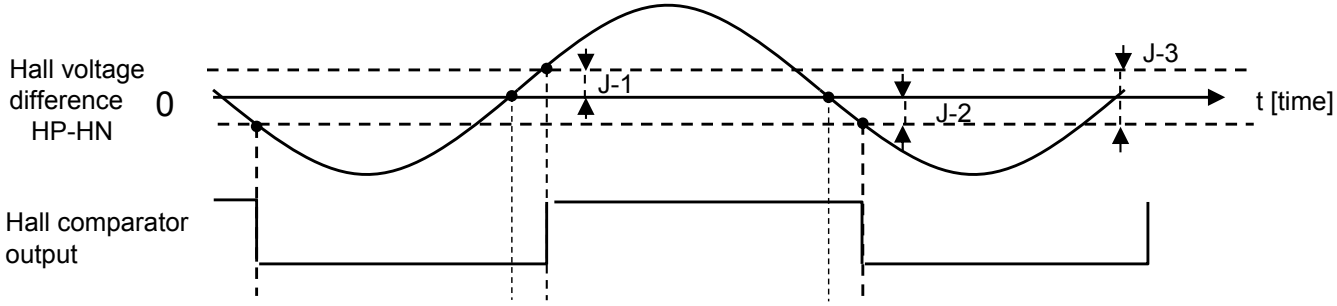
Functional Explanation (continued)

8. Hall input

Hall hysteresis comparator carries out position detection. If the amplitude of the sine wave is small, the phase delay of the comparator output becomes significant, therefore, increase the amplitude. Recommendation is 200 mV or more. Also, if the hole chattering occurs, put capacitor between HP (2, 4, 6 pin) and HN (1, 3, 5 pin).

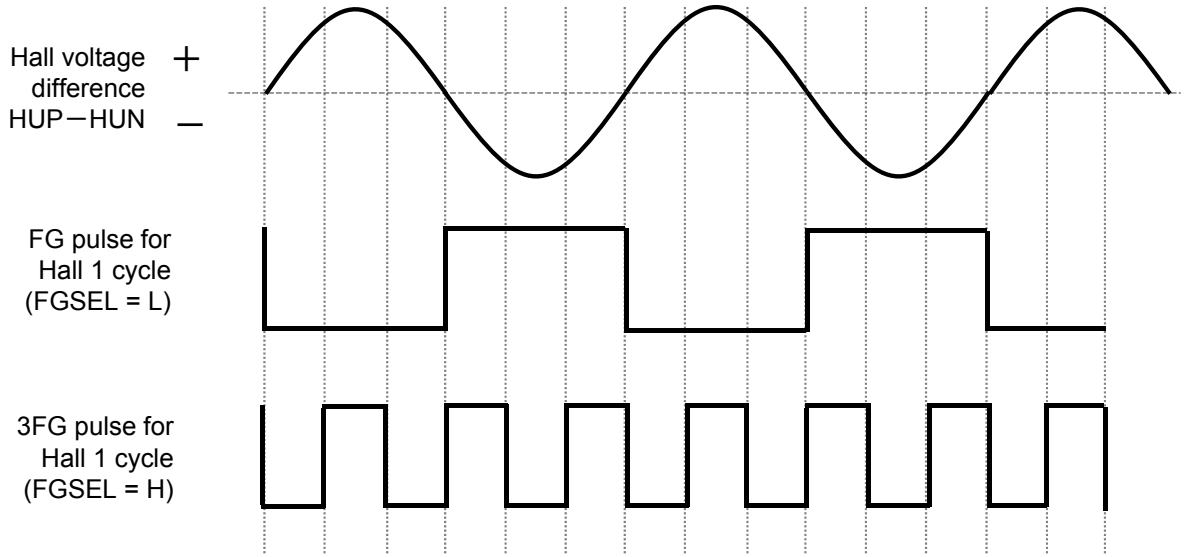


The following is a schematic diagram of the characteristics.
J-1 hysteresis level: 10 mV L → H
J-2 hysteresis level: 10 mV H → L
J-3 hysteresis width: 20.0 mV (typ)



・Relationship between Hall voltage and FGSEL

By switching FGSEL pin, for the one cycle sine wave of Hall, it outputs FG pulse one cycle or three cycles.



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Functional Explanation (continued)

9. FGSEL pin

For Hall 1 cycle, you can choose whether the output of the FG pin is 1FG or 3FG.
See the previous page for more information.

Open of the FGSEL pin is prohibited.
On the board, give it to VREG voltage or GND voltage.

10. OFFSW pin

In the VSP mode, you can set the OFF time of OFF time constant current peak detection PWM drive control.
At OFFSW = H, OFF time is 2.2 usec.
At OFFSW = L, OFF time is 7.0 usec.

In the PWMIN mode, you can set the protection time of the overcurrent protection operation.
At OFFSW = H, protection time is 2.2 usec.
At OFFSW = L, protection time is 7.0 usec.

Refer to page 20 for more information.

Open of the OFFSW pin is prohibited.
On the board, give it to VREG voltage or GND voltage.

11. BR pin

By the voltage setting of BR pin, you can choose whether the output is normal drive or low side SBRK of low side power output three-phase ON.

At BR=L: Output is normal drive.
At BR=H: Output is low side SBRK.

When open the BR pin, it generates about 3V in the internal circuit, and it is determined that BR = H internally, then it transits to SBRK mode.

Drive the BR pin with an external voltage.
If the VREG voltage of IC is used, at the time becoming STBY mode, VREG voltage is not lowered and voltage of 1 to 2V is output. So the use of voltage VREG is prohibited.

At short braking, brake current is determined by the motor and speed.
Consider enough to prevent the IC destruction.

Functional Explanation (continued)

12. FR pin

By the voltage setting of the FR pin, you can choose whether forward rotation or reverse rotation.

FR=H: Output is forward rotation.
FR=L: Output is reverse rotation.
Refer to page 13 for more information.

When you open the FR pin, it generates about 3V in the internal circuit, it is determined that the FR = H internally, and it becomes the forward rotation mode.

Drive FR pin by an external voltage.
If you use the VREG voltage of IC, when it becomes STBY mode, VREG voltage does not fall and VREG voltage about 1 to 2V is output, so the use of voltage VREG is prohibited.

In addition, F/R control is instantly reversed.
At the time of instantaneous reversal when the motor is driven, there is a possibility of high current generated by the rotational speed or the current value.
By dropping the number of revolutions before reversal, etc., you must fully assess so that the IC is not broken.

13. PWMIN/VSP pin

●In the PWMIN mode, it becomes the pin of the PWM signal input.

PWMIN=L: PWM drive output is ON. (ON duty)
PWMIN=H: PWM drive output is OFF. (OFF duty)

In addition, this pin also shares with the activation determination. In the STBY mode, L-level voltage is input to the PWMIN pin, it releases the STBY mode, and VREG voltage starts.

Also, this pin shares with free-run determination. Under normal operating conditions, if the time that PWMIN is H level continues in 5 msec, it determines 0% duty internally and the output becomes the Free run mode.
At the time of 0% duty in 5msec before free-run, the outputs in the upper phase 2 are ON, and they are in the upper SBRK mode. By a motor and rotational speed, there is a possibility of high current generation.
If you want to transit from high duty to free-run, you should fully assess so that the IC is not broken, .

When you open the PWMIN/VSP pin in the PWMIN mode, it generates about 3V in the internal circuit, and it is determined that the H-level voltage input internally, and the outputs become OFF, and it stop the motor drive.

●In the VSP mode, it becomes the pin of DC voltage input.

By the input of the 1V to 2.5V and loop control of the current peak detection according to the input voltage, it drives the output.
This pin also shares with the activation determination, if DC voltage of 0.9V or more is input, it releases the STBY mode, and VREG voltage starts.

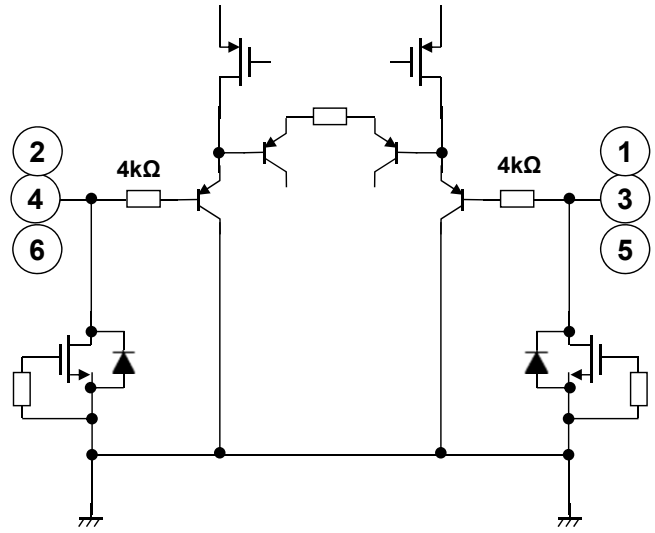
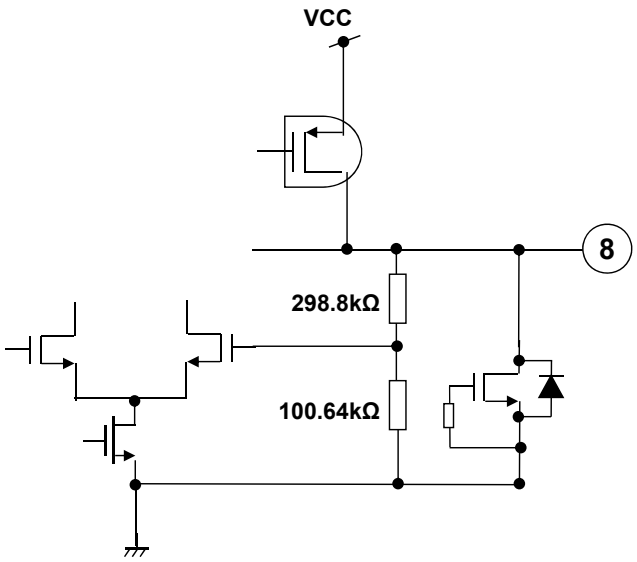
Also, this pin shares with free-run determination. By the input voltage of 0.9V or less, it comes up with free-run decision.

When you open the PWMIN/VSP pin in the VSP mode, it is determined that the voltage is 0.9V or less internally, the operation stops the motor drive.

Refer to page 14-17 for more information.

PIN EQUIVALENT CIRCUIT

Note: The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Internal circuit	Impedance	Description
1, 2, 3, 4, 5, 6		—	Pin1(HWN) ,Pin3(HVN),Pin5(HUN) :Hall amplifier (U, V, W) – input pin Pin2(HWP) ,Pin4(HVP),Pin6(HUP) :Hall amplifier (U, V, W) + input pin
8		—	Pin8(VREG) :Internal reference voltage (5V)

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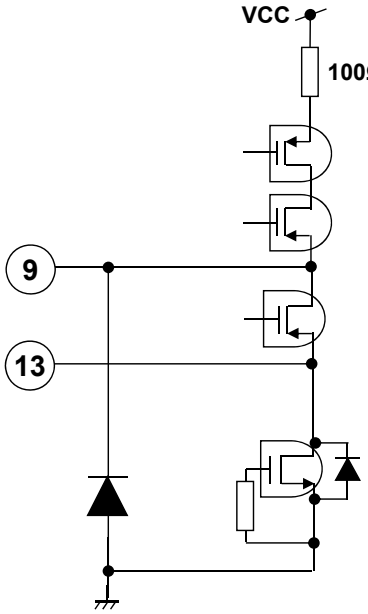
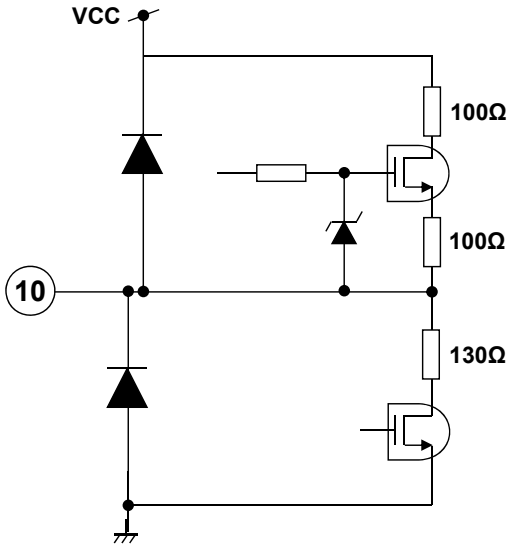
PIN EQUIVALENT CIRCUIT (continued)

Note: The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Internal circuit	Impedance	Description
9, 13		—	Pin9（BC2） :For charge pump capacitor connection pin 2 Connect a capacitor between this pin and Pin10 (BC1). Pin13（VPUMP） :Charge pump voltage output pin Connect a capacitor between this pin and Pin11 (VCC).
10		—	Pin10(BC1) :For charge pump capacitor connection pin 1

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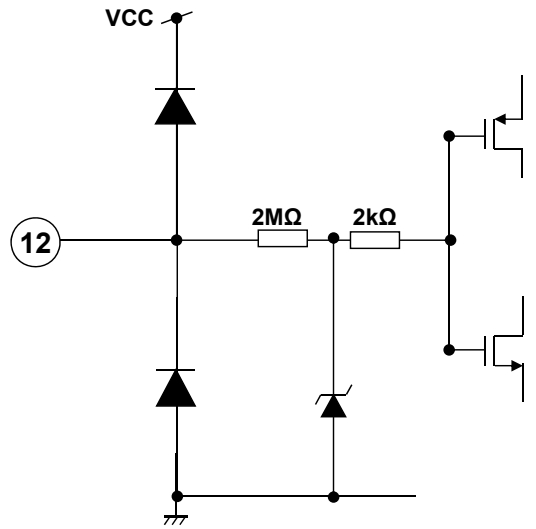
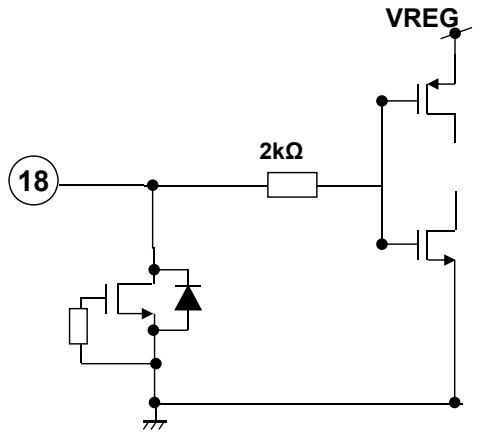
PIN EQUIVALENT CIRCUIT (continued)

Note: The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Internal circuit	Impedance	Description
12		—	Pin12（INSEL） :PWMIN or VSP mode selection pin
18		—	Pin18(FGSEL) :FG output mode selection pin

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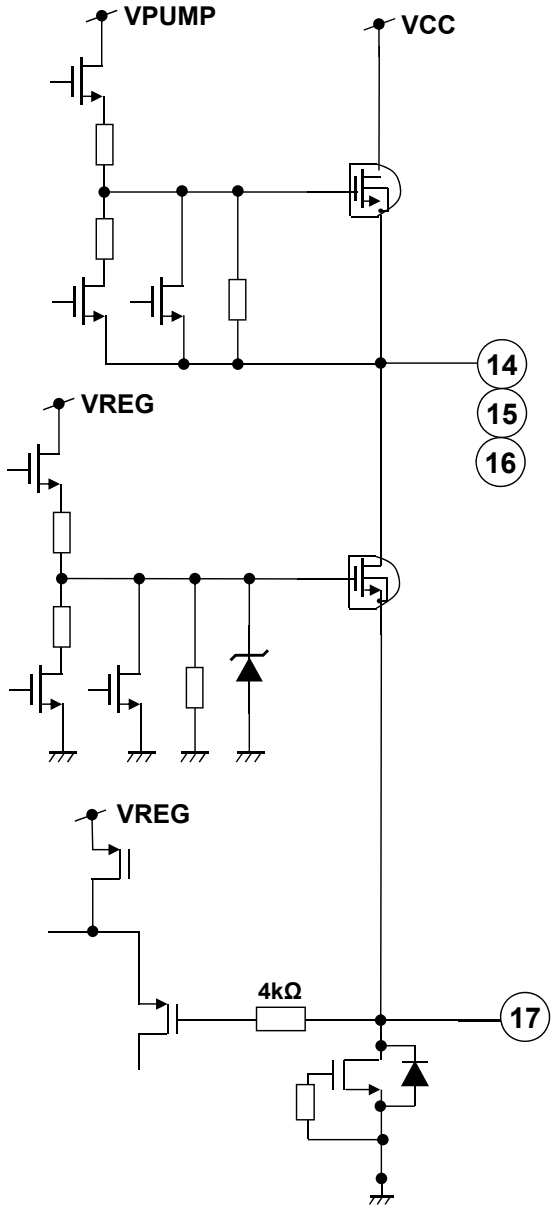
PIN EQUIVALENT CIRCUIT (continued)

Note: The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Internal circuit	Impedance	Description
14, 15, 16, 17		—	Pin14(U), 15(W), 16 (V) :Motor drive output pin Pin17（RCS） :Motor current limit (PWMIN mode) / Motor current detector (VSP mode) pin

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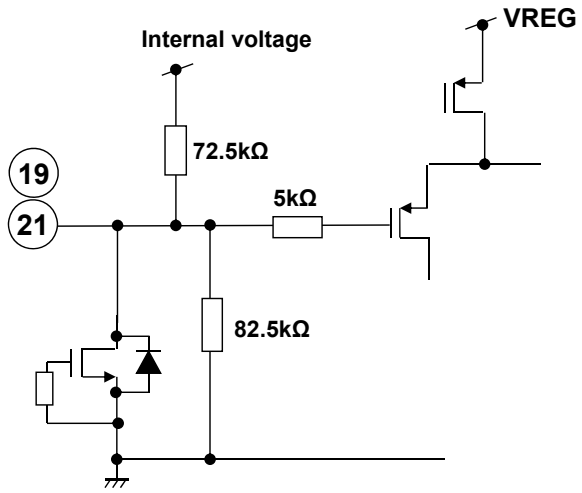
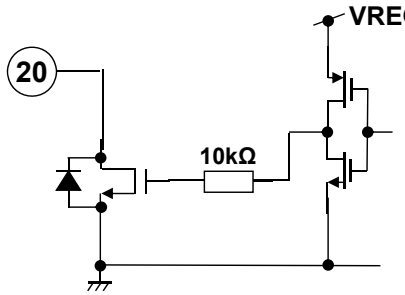
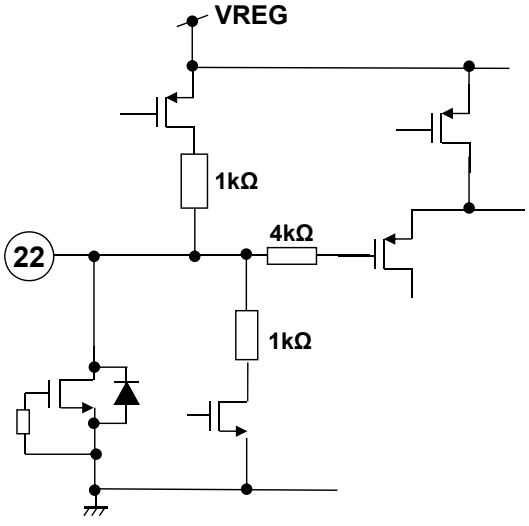
PIN EQUIVALENT CIRCUIT (continued)

Note: The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Internal circuit	Impedance	Description
19, 21		38.6kΩ	Pin19（BR） :Brake mode selection pin Pin21（FR） :Forward / Reverse rotation direction selection pin
20		—	Pin20(FG) :FG signal output pin
22		—	Pin22(CLDOSC) :Setting oscillation frequency of motor restricted protection pin

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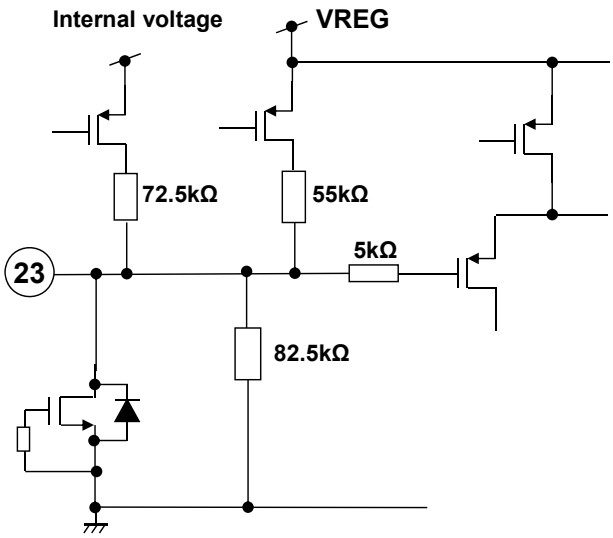
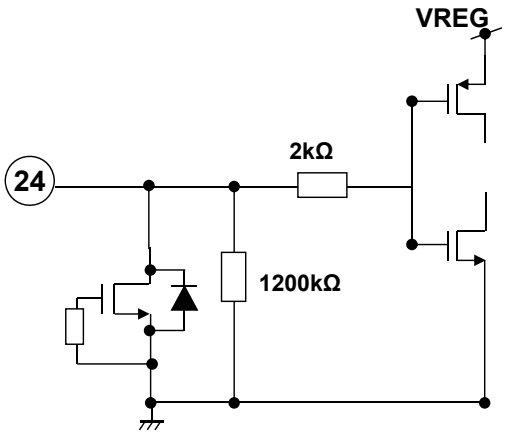
PIN EQUIVALENT CIRCUIT (continued)

Note: The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Internal circuit	Impedance	Description
23		33kΩ	Pin23（PWMIN/VSP） :PWM input (PWMIN mode) or DC voltage input (VSP mode) for motor control selection pin
24		—	Pin24(OFFSW) :PWM OFF time selection pin

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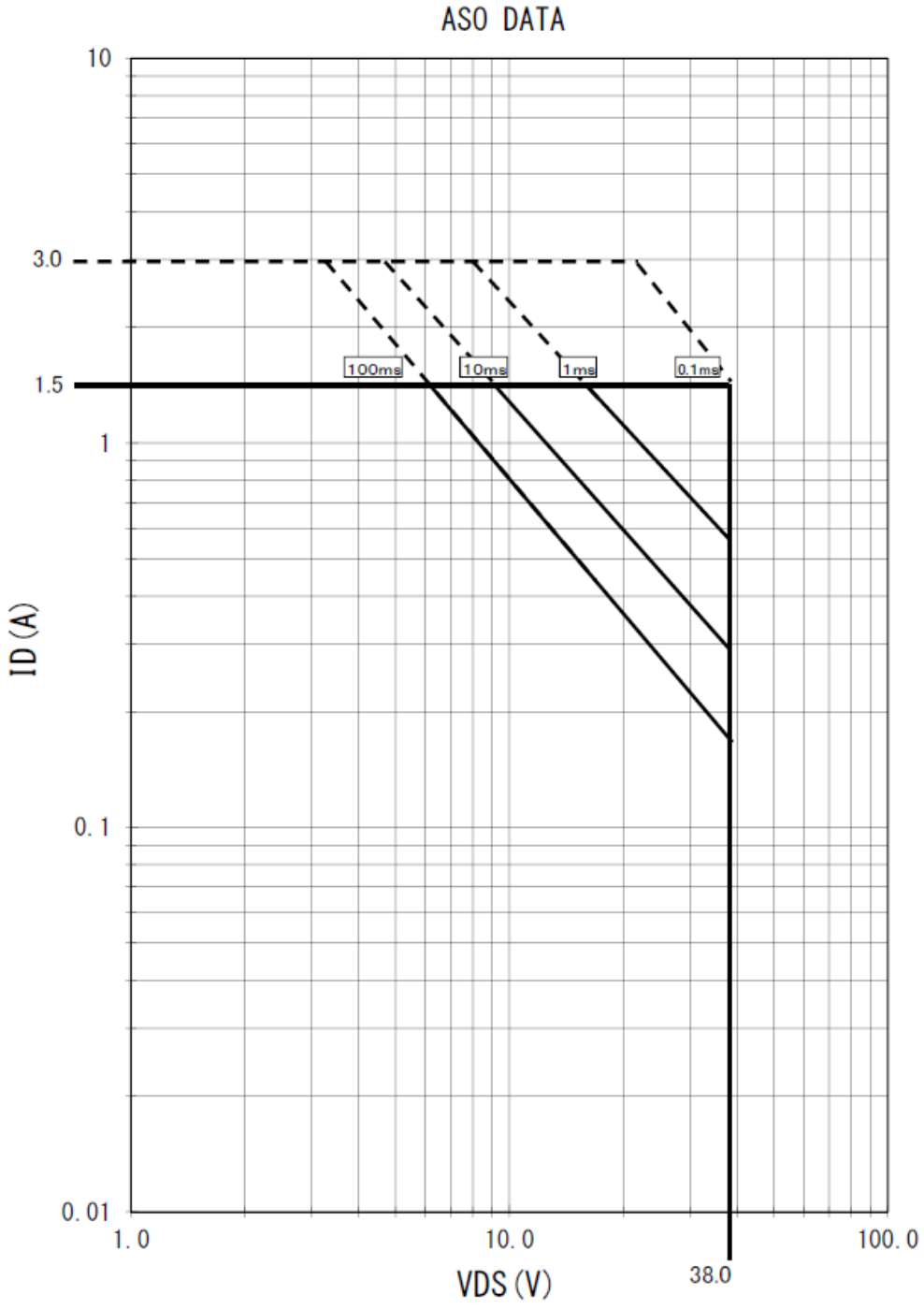
■Technical data

Ta = 25 °C, Single pulse

1. Safe Operating Area

Note: The characteristics listed below are reference values based on the IC design and are not guaranteed values.

This data is the data of Ta = 25 °C, one-shot pulse.
In actual use, it is considered that the rise of Tj and the application of multiple pulses, use this as reference data.
In your company, as well as to perform sufficient reliability test, perform the evaluation set.



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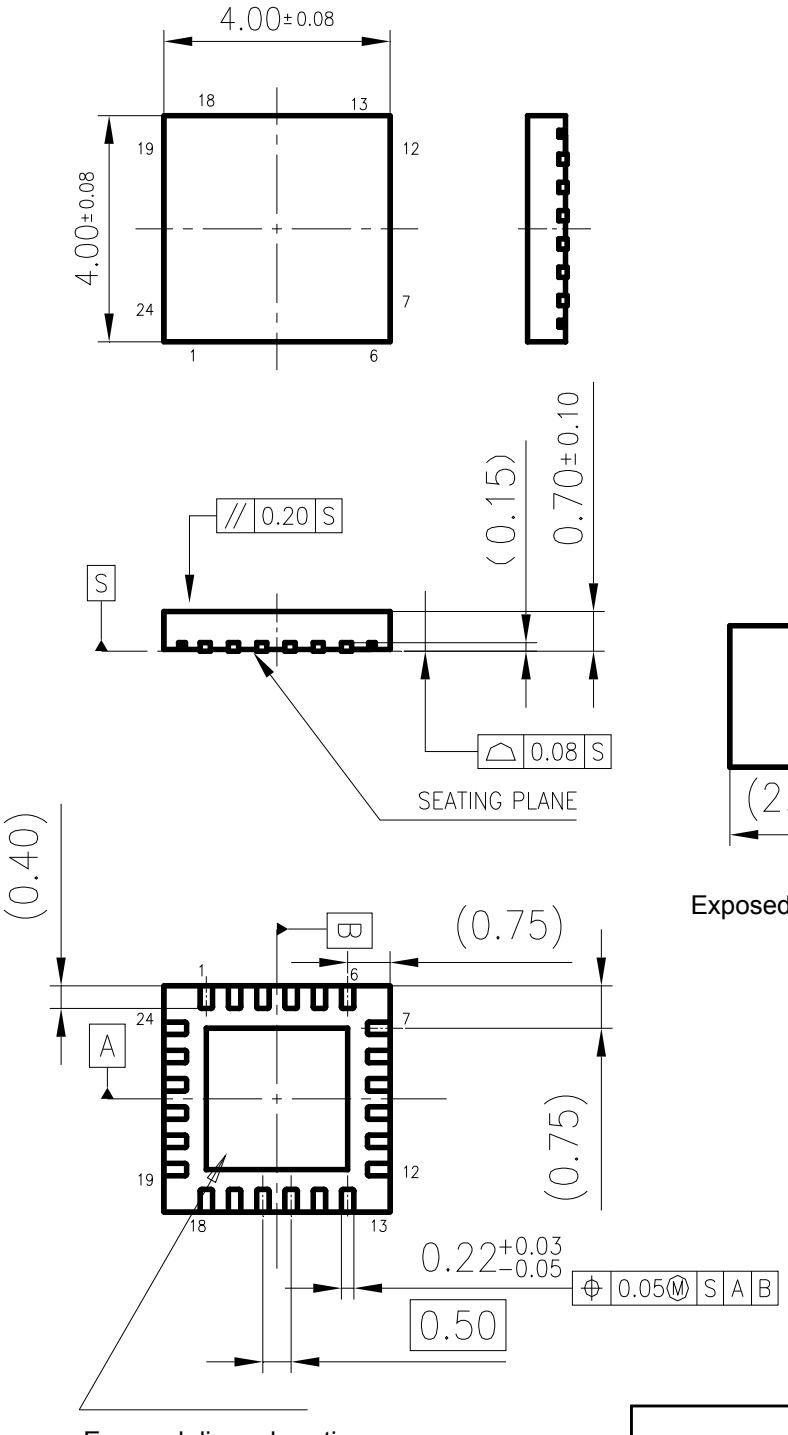
Package Information (Reference outline view)

Package Code: HQFN024-A-0404AZ

Unit: mm



Exposed die pad section

Exposed die pad section

Sealing Material: Br/Sb-free epoxy resin
Lead material: Cu alloy
Lead surface treatment: Pd plating

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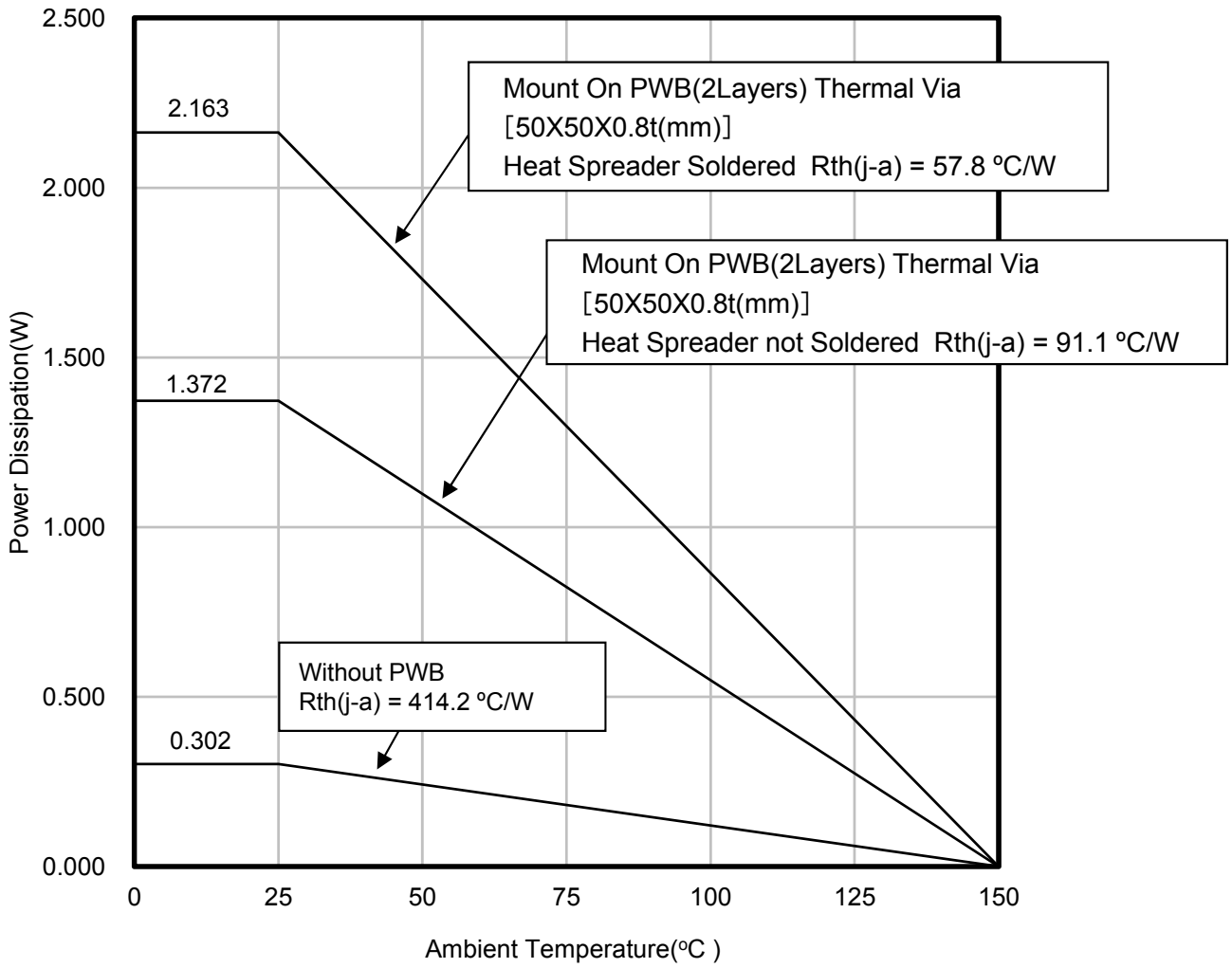
Package Information (continued)

Dissipation (Technical data)
Package Code: HQFN024-A-0404AZ



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Package Information (continued)

Dissipation (supplementary material)

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity.
（Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
2-layer	2-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta ：Ambient air temperature
※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc ：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj ：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

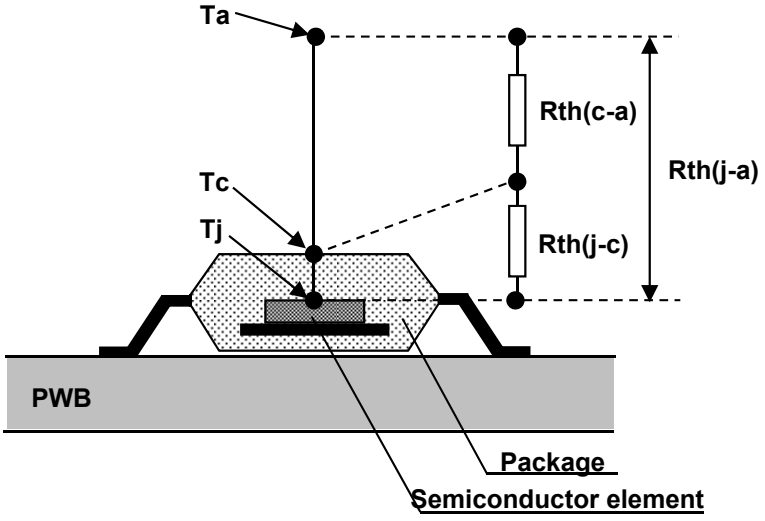

Fig1. Definition image

[Definition formula]

$$Tj=\{Rth(j-c)+Rth(c-a)\}\times P+Ta$$
$$=Rth(j-a)\times P+Ta$$

$$Rth(j-c)=\frac{Tj-Tc}{P}\ (℃/W)$$

$$Rth(c-a)=\frac{Tc-Ta}{P}\ (℃/W)$$

$$Rth(j-a)=\frac{Tj-Ta}{P}\ (℃/W)$$

$$=Rth(j-c)+Rth(c-a)$$

P:power(W)

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■ IMPORTANT NOTICE

1. When using the IC for new models, verify the safety including the long-term reliability for each product on customer responsibility.

2. When the application system is designed by using this IC, be sure to confirm notes in this book. Be sure to read the notes to descriptions and the usage notes in the book.

3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.

4. This IC is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.

5. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.

6. Pay attention to the direction of IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.

7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Configuration.

8. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.

9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply. Although the short circuit protection circuit is built in about the following pins, when it is made to connect too hastily, it may destroy depending on VCC voltage.
   Pin14(U), Pin15(W), Pin16(V)

■ IMPORTANT NOTICE (continued)

10.The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.

11.Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

12.Product which has specified ASO (Area of Safe Operation) should be operated in ASO, and thoroughly evaluate in order to prevent the damage of IC.

13.Verify the risks which might be caused by the malfunctions of external components.

14.Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process.

15.When designing PCB pattern of RCS pin(Pin17), place a resistor for current detection close to the IC.
Otherwise, the setting value for over current protection may fluctuate due to the impedance of wiring pattern between RCS pin and the resistor.

16.It is not recommended for the use of solder dip.

17.Connect a bypass capacitor to VCC pin, close to the IC, and apply a voltage with sufficiently low impedance to it.

18.After turning on VCC, while the VCC voltage rises to the set voltage, If the VCC voltage is reduced by a motor drive, it may not start properly, you should fully evaluate and consider the current capability of the power supply.

19.Connect the metallic plate (fin) on the back side of the IC to the GND potential. The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.

20. Sufficient thermal design should be done not to exceed the power dissipation, based on the conditions of power supply, load and ambient temperature.

■ Usage Notes

•Precautions for this IC

1.Precautions for power activation and breaking speed

After resetting the all circuit by the activation of UVLO, power-up sequence of this IC continues to launch the system in order by release of UVLO.
Therefore, set the VCC (pin 11) so that the voltage rises with slew rate of 0.24/ms or less during power-on, and it falls with the rate of -0.24 V/ms or more during power-off.

It is recommended to perform a sufficient reliability test and evaluation of the product with the incorporated IC before applying the IC to a product.

2. Precautions for booster circuit

・Capacitor C_{VPUMP} between the VPUMP pin (pin 13) and VCC pin in the figure explaining the application circuit on page 10 can be used between the VPUMP pin and GND pin (pin 7). When the capacitor is connected between the VPUMP pin and GND pin, check that the dielectric strength of the capacitor is 50 V. The dielectric strength of the capacitor connected between the VPUMP pin and VCC pin can be 16 V. [Recommended value: C_{BC} = 0.01 μF (with a dielectric strength of 50 V); C_{VPUMP} = 0.01 μF (with the above dielectric strength)]

・When the VCC starts rising, an inrush current flows into the capacitor (C_{BC}) between the BC1 pin and BC2 pin and the capacitor (C_{VBUMP}) between the VPUMP pin and GND pin. Fully evaluate and set the C1 and C2 capacitance values to protect the IC from destruction caused by the inrush current.
If the capacitance (C_{BC}) is excessively high, the VPUMP voltage may not be fully stepped up. Conversely, if the capacitance is excessively low, a current capacity necessary for the booster circuit may not be obtained. Fully evaluate and set the C_{BC} capacitance value so that the VPUMP voltage will be high enough.

・Set the capacitance of the VPUMP pin so that the voltage on the VPUMP pin (pin 13) will not exceed 45 V even transiently when starting the motor from the motor standby mode .

3. Note on the capacity between VCC and GND

This IC adopts a PWM drive method, and the output transistor is turned on and off with a high current. This easily generates noise, which may malfunction or damage the IC. In order to protect the IC from malfunctioning or destruction due to noise, the power supply must be fully stabilized. Therefore, the capacitor between the VCC pin and ground must be as close as possible to the IC. Pay utmost attention so that the IC will not be damaged or malfunction due to PWM noise.

■ Usage Notes (continued)

• Precautions for this IC (continued)

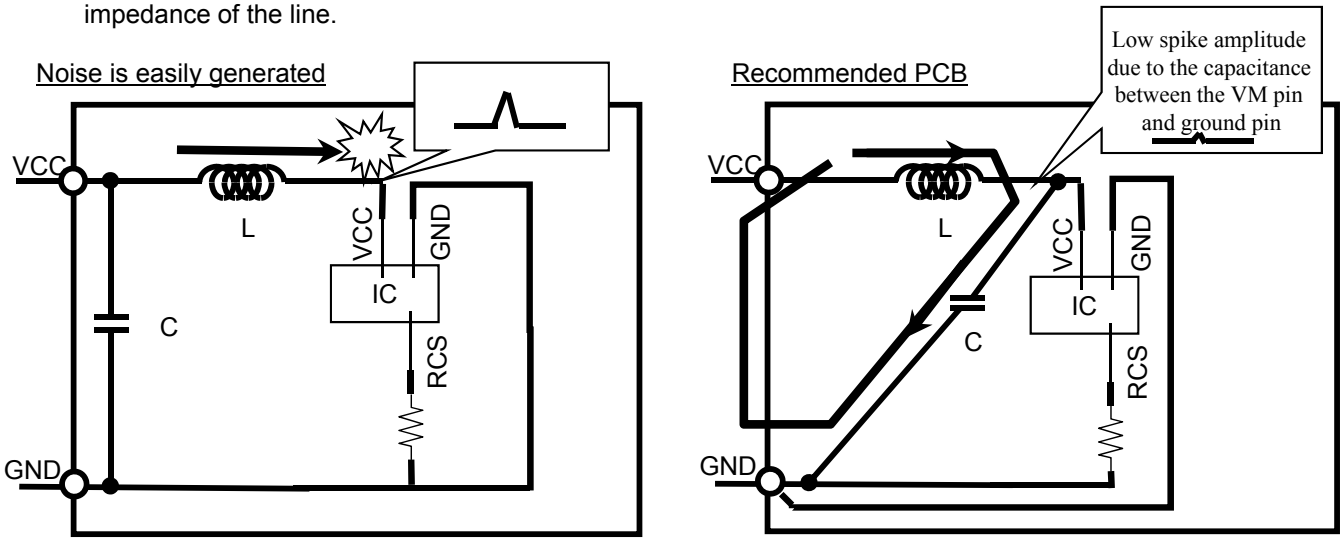
4. Motor PCB pattern

A high current flows into the IC. Therefore, the common impedance of the PCB pattern cannot be ignored. Take the following points into consideration and design the PCB pattern of the motor.

- A high current flows into the line between the VCC connector and the VCC pin (pin 11) of the IC. Therefore , noise is easily generated at the time of switching due to the inductance (low) of the line, which may result in the malfunctioning or destruction of the IC (see the circuit diagram on the left-hand side). As shown in the circuit diagram on the right-hand side, the escape way of the noise is secured by connecting a capacitor to the connector close to the VCC pin of the IC. This makes it possible to suppress the direct VCC pin voltage of the IC. Make the settings as shown in the circuit diagram on the right-hand side as much as possible. The inductance (low) of the line increases in proportion to the length of the pattern. Design the line between the VCC connector and the VCC pin of the IC so that the line will be as thick as possible and as short as possible.

- The line from the current detection resistor (RCS) to the RCS pin (pin 17) is very important. Therefore, it is recommended to connect an independent line to the RCS pin from the root of the detection resistor as much as possible. If RCS separates from IC, the right current value will not be detected due to the impedance of the line. If installation near the IC is difficult, monitor and check that the motor current waveform and RCS current waveform are normal.

- The line from the GND connector to the RCS resistor and the line to the GND pin (pin 7) of the IC must be independent from each other. If they are common with the line to the RCSF, the ground voltage of the IC will fluctuate due to the impedance of the line, which may result in the malfunctioning of the IC. Design the ground line so that the line will be as thick as possible and as short as possible in order to suppress influence of the impedance of the line.



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■ Usage Notes (continued)

• Precautions for this IC (continued)

5. Motor restricted protection function

In this IC, as described in page 18, motor restricted protection function is built in.
The operating time of motor restricted protection can be determined by the capacitance value of the CLDOSC pin. The time is obtained from the following formula. This formula is, however, prepared with no consideration to the temperature characteristics.

Motor restricted protection operating time(s) = 256 × External capacitance (C_{CLDOSC}) (uF) ×
Hysteresis width (V_{CLD}) × {1/Charge current (I_{CLD1}) + 1/Discharge current (I_{CLD2})}
≒ 85 × External capacitance

In the actual use, since it is considered that such as increase of Tj by power consumption, thoroughly evaluate, and set the external capacitor.

Notes:

1. When the CLDOSC pin is open, the motor restricted protection time is very short due to CLD oscillation by parasitic capacitance. If CLD oscillation frequency is too short, since the IC internal counter is not be able to detect the CLD oscillation, the protection function does not operate normally. In determining CLD oscillation frequency, please thoroughly evaluate.

2. If the CLDOSC pin chatters beyond the hysteresis width, the motor restriction protection function can malfunction. Design the wiring pattern so that the CLDOSC pin will not chatter.

3. If the motor restricted protection is not used, by connecting CLDOSC pin to GND, you can disable the restricted protection. However, in this case, it does not transit to STBY mode.

6. BR, FR, PWMIN/VSP pin

BR, FR, PWMIN / VSP pins are MCU interface. In the case that the current setting of the motor is large and lead line of GND is long, the potential of GND pin of the IC may be increased.
If 0V is input from the microcomputer, there is a case to be negative potential in the potential difference between the GND pin of this IC and the interface pin. If these pins detect under -0.3V, note that there is a possibility to break or malfunction.

7. Note on short brake

For short brake mode, the brake current will be determined according to the speed of rotation and motor.
For entering the short brake mode, please evaluate the study and identify, such as reducing the motor current, and decreasing the number of revolutions.
Refer to the ASO data and fully evaluate the circuit so that the IC will not be damaged.

8. Note of Forward/Reverse switching

When performing instant reversal of the motor drive, there is a possibility of high current generated by the rotational speed or current value at the time of inversion.
Please evaluate the study and identify, such as decreasing the number of revolutions before reversal.
Refer to the ASO data and fully evaluate the circuit so that the IC will not be damaged.

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■ Usage Notes (continued)

• Precautions for this IC (continued)

9. Notes on free-run transition

In the PWMIN mode, if the determination that PWMIN is H level continues in 5 msec, it performs duty decision 0% internally, it sets output in free-run state.
At the time of 0% duty in 5 msec before free run, Output is in the upper SBRK state of the upper side two-phase ON.
By a motor and rotational speed, there is a possibility of high current generation.
If you want to transit to free-run from the high duty, please enough study so that the IC is not destroyed.

10. Notes of a sudden change of the motor speed

In the case of changing abruptly to the low-speed from the high speed of the motor, since there is a possibility that the power supply voltage is increased by the motor current is returned to power source, thoroughly evaluate and examine.

11. Notes about FG pin

The output of FG pin (pin 20) is open-drain.
By connecting a pull-up resistor to a given power supply, use in the current range and within the allowable terminal voltage.
FG is the output of the comparator between the input pins, HUP, HUN.
For this reason, if the FG output is chattering, please connect a capacitor between HUP-HUN.
In this case, we recommend that you connect also capacitors between HVP-HVN, and HWP-HWN to match the hole pin condition of the three-phase.
In addition, note that FG output becomes High momentarily at power-on and cut-off.

■ Usage Notes (continued)

• Precautions for this IC (continued)

12. Protection function
In this IC, 4 protection function is built in. Note and check the following items.

Function	Activation/Release conditions	Output	Note
UVLO (VCC)	• Protection start Under 4.8 V (VCC, typ) • Protection release Over 5 V (VCC, typ)	High side Power :OFF Low side Power :ON (Short-brake)	In the protection operation, it becomes lower short brake. There is a possibility of high current generation by the short brake of the motor rotation, Identify sufficiently without destroyed.
Overcurrent protection	・ Protection start RCSS voltage: Over 0.21V (typ.) ・ Protection release After a fixed time has passed	Stopping PWM operation a fixed time	Please design considering the board pattern with reference to the P37. In addition, in consideration of overcurrent detection level, variation of the resistance, the temperature, etc., design the full consideration so as not to exceed the rated resistance value of the RCS.
Motor restricted protection	• Protection start In the setting time, the motor rotation signal is not detected. • Protection release ・at switching F/R ・at BR operation ・at UVLO operation ・at STB transition	High side Power 1 phase: ON Low side Power 3 phase: OFF (Free run)	There is a possibility that the restricted protection occurs in the long start-up time motor. Thoroughly evaluate and connect an external capacitor. This setting time also serves the time from the motor stop after free-run to standby, Please set the capacitance value in consideration of the time. When connecting it to GND, the restricted protection function is disabled, but note that the transition to standby also becomes disabled.
Thermal protection	・ Protection start T_J: Over 160 °C (typ.) ・ Protection release T_J: Under 120 °C (typ.)	Power all phase OFF	In the protection operation, it becomes all phases off. If the protection operation repeats on and off at the motor rotation, reverse current is generated. Please note the power rise.

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(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

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