

阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .



VNB35NV04 / VNP35NV04 VNV35NV04 / VNW35NV04

“OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFET

TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNB35NV04	10 m Ω (*)	30 A	40 V
VNP35NV04			
VNV35NV04			
VNW35NV04			

(*) For PowerSO-10 only

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

The VNB35NV04, VNP35NV04, VNV35NV04, VNW35NV04 are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology,

D²PAK **PowerSO-10™**

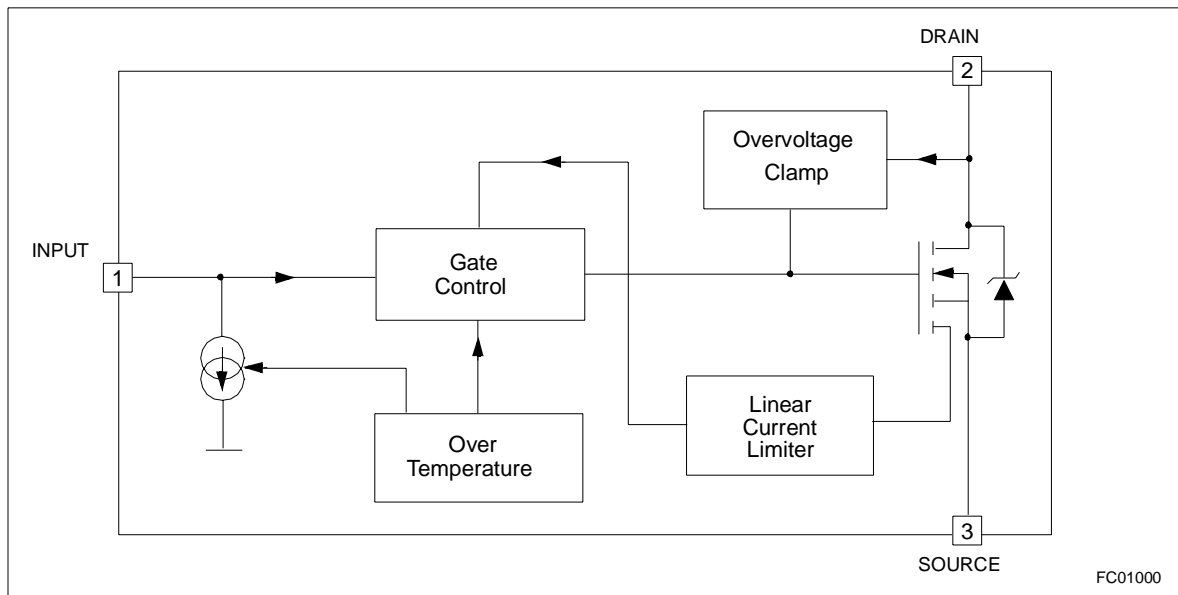
TO-220 **TO-247**

ORDER CODES:

D ² PAK	VNB35NV04
TO-220	VNP35NV04
PowerSO-10™	VNV35NV04
TO-247	VNW35NV04

intended for replacement of standard Power MOSFETS from DC up to 25KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments. Fault feedback can be detected by monitoring the voltage at the input pin.

BLOCK DIAGRAM

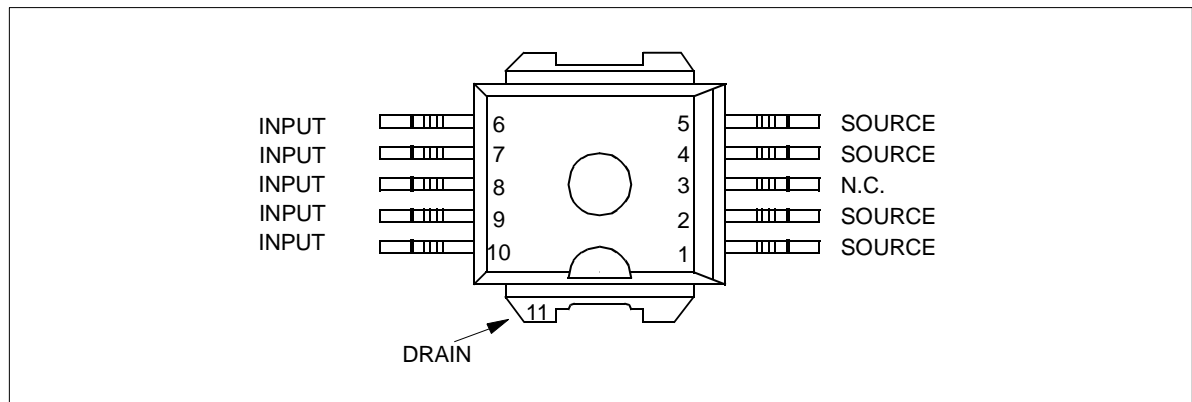


VNB35NV04 / VNP35NV04 / VNV35NV04 / VNW35NV04

ABSOLUTE MAXIMUM RATING

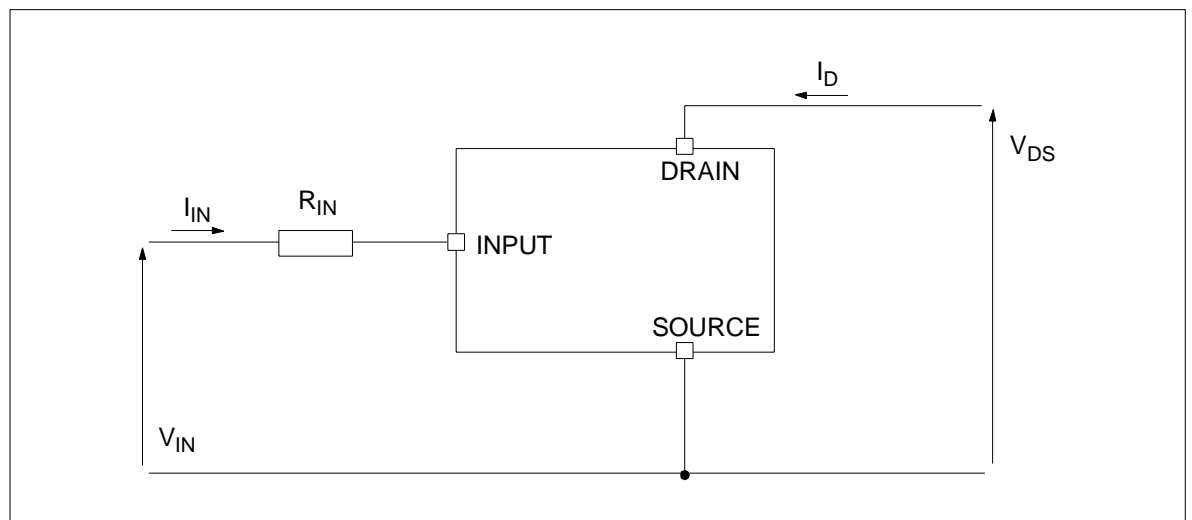
Symbol	Parameter	Value				Unit
		PowerSO-10™	D ² PAK	TO-220	TO-247	
V_{DS}	Drain-source Voltage ($V_{IN}=0V$)	Internally Clamped				V
V_{IN}	Input Voltage	Internally Clamped				V
I_{IN}	Input Current	+/-20				mA
$R_{IN\ MIN}$	Minimum Input Series Impedance	4.7				Ω
I_D	Drain Current	Internally Limited				A
I_R	Reverse DC Output Current	-30				A
V_{ESD1}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)	4000				V
V_{ESD2}	Electrostatic Discharge on output pin only ($R=330\Omega$, $C=150pF$)	16500				V
P_{tot}	Total Dissipation at $T_c=25^\circ C$	125	125	125	208	W
T_j	Operating Junction Temperature	Internally limited				$^\circ C$
T_c	Case Operating Temperature	Internally limited				$^\circ C$
T_{stg}	Storage Temperature	-55 to 150				$^\circ C$

CONNECTION DIAGRAM (TOP VIEW)



(*) For the pins configuration related to TO-220, TO-247, D²PAK, see outlines at page 1.

CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter		Value				Unit
			PowerSO-10™	D2PAK	TO-220	TO-247	
R _{thj-case}	Thermal Resistance Junction-case	MAX	1	1	1	0.6	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	MAX	50(*)	50(*)	50	30	°C/W

(*) When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 μm thick) connected to all DRAIN pins.

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 150°C, unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CLAMP}	Drain-source Clamp Voltage	V _{IN} =0V; I _D =15A	40	45	55	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	V _{IN} =0V; I _D =2mA	36			V
V _{INTH}	Input Threshold Voltage	V _{DS} =V _{IN} ; I _D =1mA	0.5		2.5	V
I _{ISS}	Supply Current from Input Pin	V _{DS} =0V; V _{IN} =5V		100	150	μA
V _{INCL}	Input-Source Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6 -1.0	6.8	8 -0.3	V
I _{DSS}	Zero Input Voltage Drain Current (V _{IN} =0V)	V _{DS} =13V; V _{IN} =0V; T _j =25°C V _{DS} =25V; V _{IN} =0V			30 75	μA

ON

Symbol	Parameter	Test Conditions	Max		Unit
			PowerSO-10	D ² PAK TO-220 / TO-247	
R _{DS(on)}	Static Drain-source On Resistance	V _{IN} =5V; I _D =15A; T _j =25°C V _{IN} =5V; I _D =15A; T _j =150°C	10 20	13 24	mΩ

VNB35NV04 / VNP35NV04 / VNV35NV04 / VNW35NV04

ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^\circ\text{C}$, unless otherwise specified)

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}^*	Forward Transconductance	$V_{DD}=13\text{V}; I_D=15\text{A}$		35		S
C_{OSS}	Output Capacitance	$V_{DS}=13\text{V}; f=1\text{MHz}; V_{IN}=0\text{V}$		1300		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}; I_D=15\text{A}$		150	500	ns
t_r	Rise Time			840	2500	ns
$t_{d(off)}$	Turn-off Delay Time	$V_{gen}=5\text{V}; R_{gen}=R_{IN\ MIN}=4.7\Omega$ (see figure 1)		980	3000	ns
t_f	Fall Time			600	1500	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}; I_D=15\text{A}$		4	12	μs
t_r	Rise Time			27	100	μs
$t_{d(off)}$	Turn-off Delay Time	$V_{gen}=5\text{V}; R_{gen}=2.2\text{K}\Omega$ (see figure 1)		34	120	μs
t_f	Fall Time			31	110	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}; I_D=15\text{A}$ $V_{gen}=5\text{V}; R_{gen}=R_{IN\ MIN}=4.7\Omega$		18		$\text{A}/\mu\text{s}$
Q_i	Total Input Charge	$V_{DD}=12\text{V}; I_D=15\text{A}; V_{IN}=5\text{V}$ $I_{gen}=2.13\text{mA}$ (see figure 5)		118		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD}^*	Forward On Voltage	$I_{SD}=15\text{A}; V_{IN}=0\text{V}$		0.8		V
t_{rr}	Reverse Recovery Time	$I_{SD}=15\text{A}; di/dt=100\text{A}/\mu\text{s}$		400		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=30\text{V}; L=200\mu\text{H}$		1.4		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, figure 2)		7		A

PROTECTIONS ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=6\text{V}; V_{DS}=13\text{V}$	30	45	60	A
t_{dlim}	Step Response Current Limit	$V_{IN}=6\text{V}; V_{DS}=13\text{V}$		50		μs
T_{jsh}	Overtemperature Shutdown		150	175	200	$^\circ\text{C}$
T_{jrs}	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf}	Fault Sink Current	$V_{IN}=5\text{V}; V_{DS}=13\text{V}; T_j=T_{jsh}$	10	15	20	mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j=25^\circ\text{C}; V_{DD}=24\text{V}$ $V_{IN}=5\text{V}; R_{gen}=R_{IN\ MIN}=4.7\Omega; L=24\text{mH}$ (see figures 3 & 4)	1.7			J

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 25KHz. The only difference from the user's standpoint is that a small DC current I_{SS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION:

internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- LINEAR CURRENT LIMITER CIRCUIT:

limits the drain current I_D to I_{lim} whatever the INPUT pin voltages is. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:

these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- STATUS FEEDBACK:

in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{SS} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Fig.1: Switching Time Test Circuit for Resistive Load

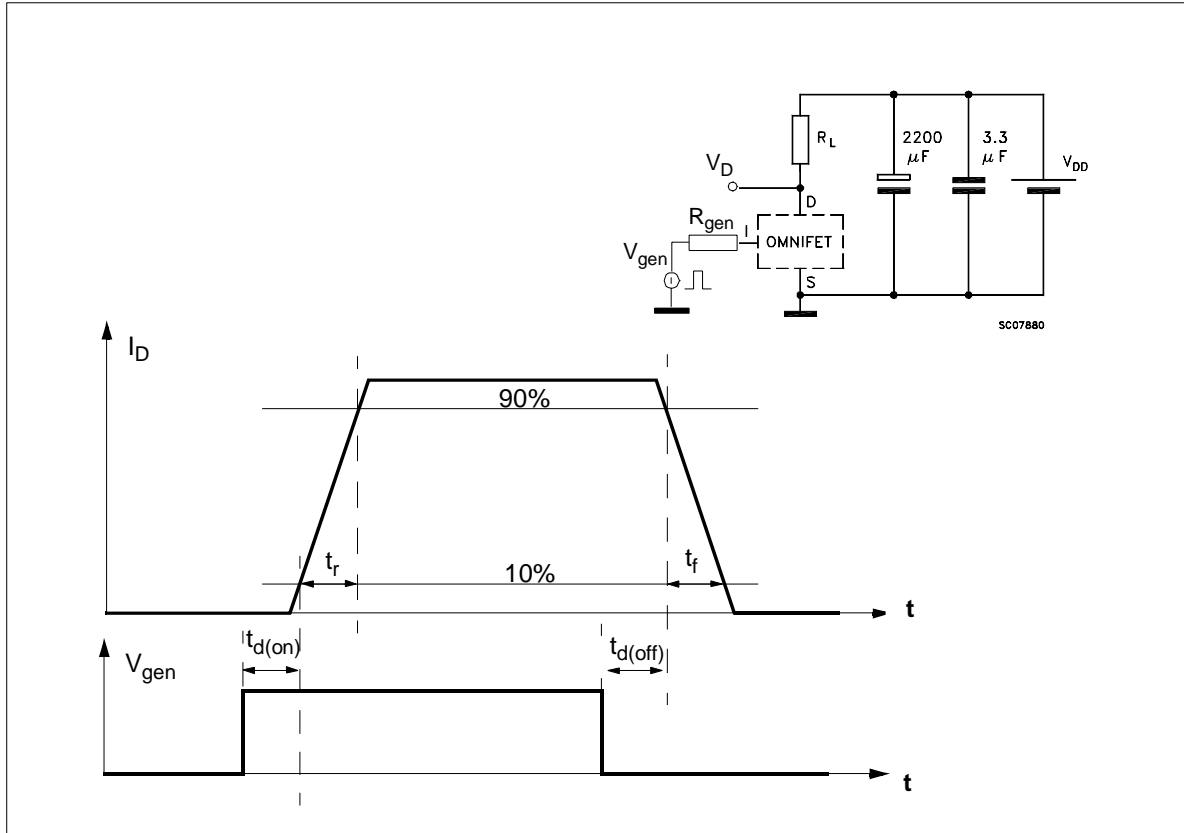


Fig.2: Test Circuit for Diode Recovery Times

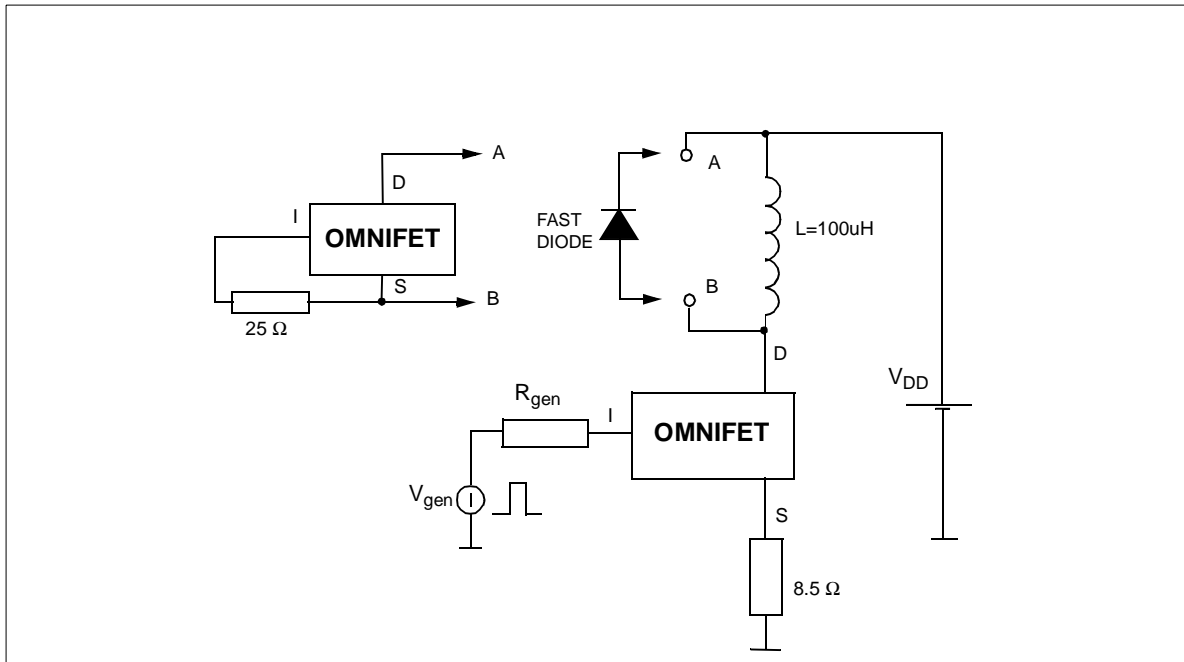


Fig. 3: Unclamped Inductive Load Test Circuits

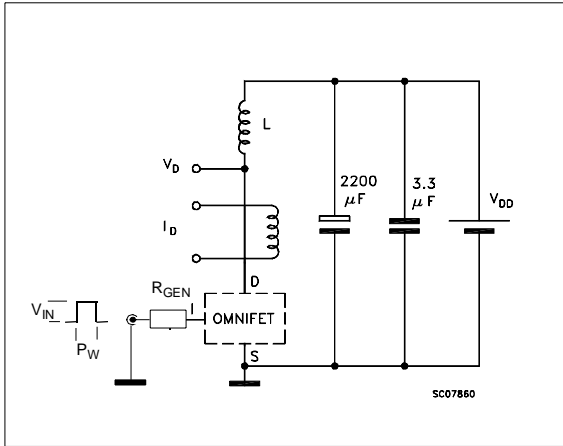


Fig. 4: Unclamped Inductive Waveforms

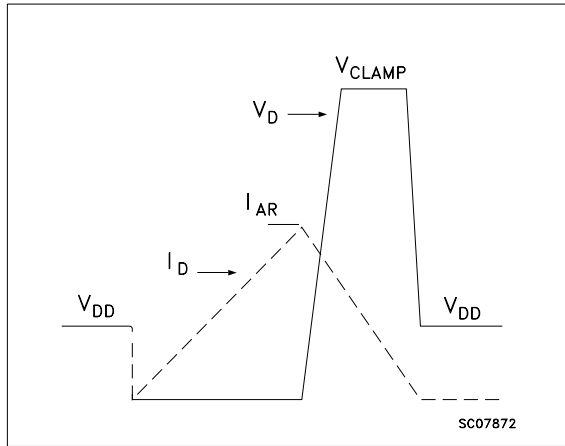


Fig. 5: Input Charge Test Circuit

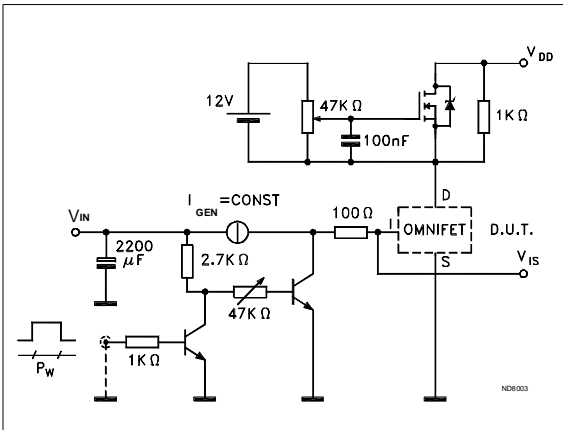


Fig 6 : Thermal Impedance for TO-220

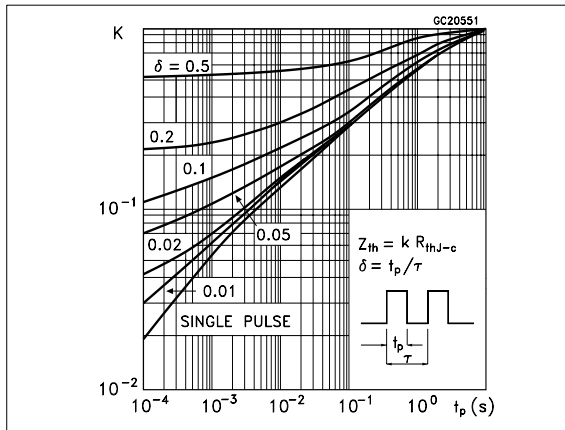
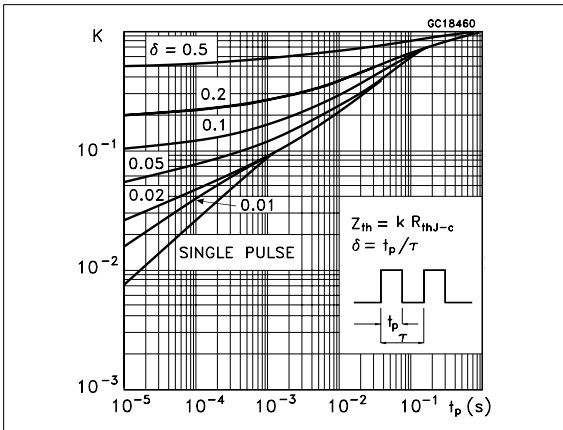
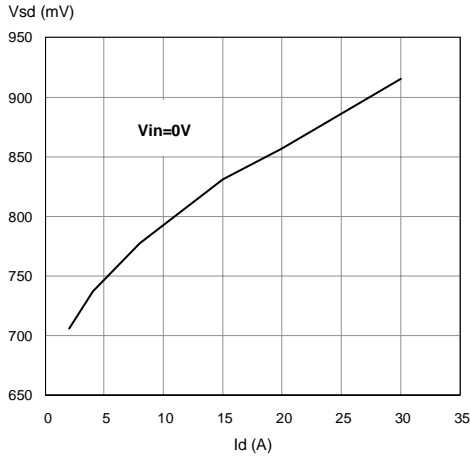


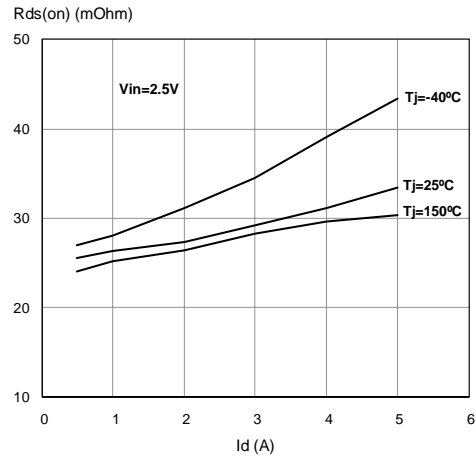
Fig. 7: Thermal Impedance for TO-247



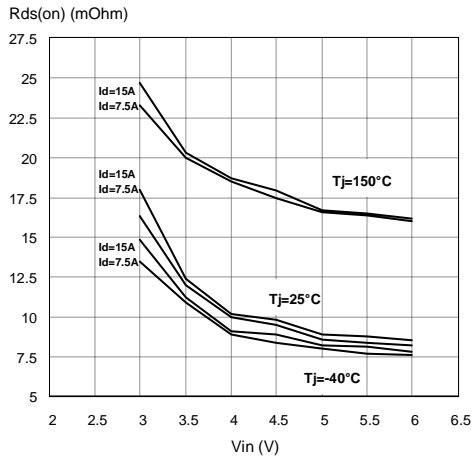
Source-Drain Diode Forward Characteristics



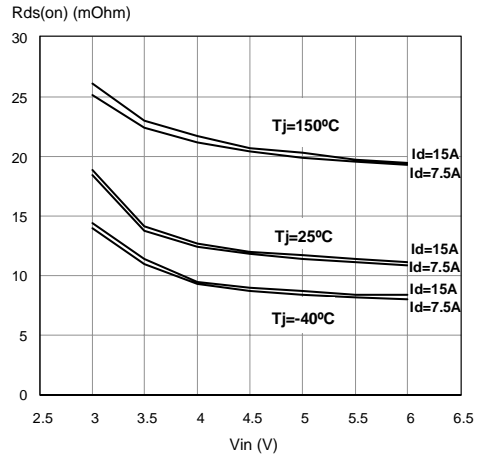
Static Drain Source On Resistance



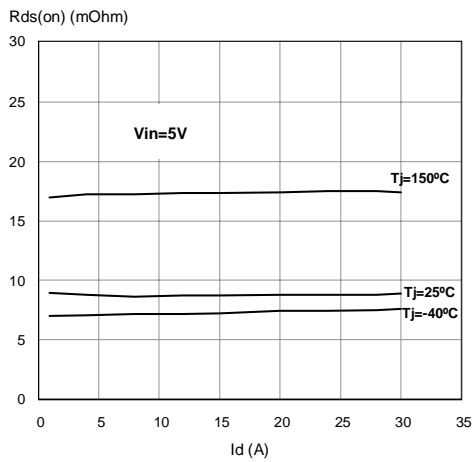
PowerSO-10 Static Drain-Source On resistance Vs. Input Voltage



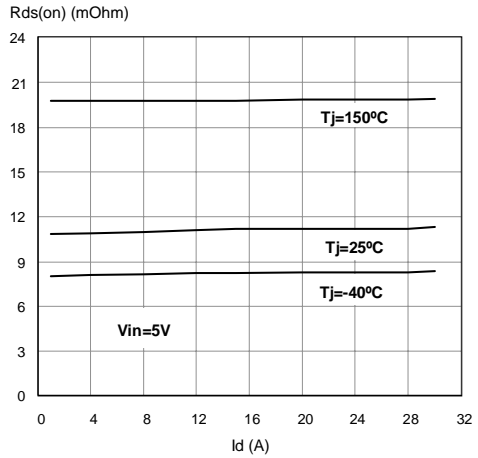
D2PAK, TO-220 & TO-247 Static Drain-Source On resistance Vs. Input Voltage



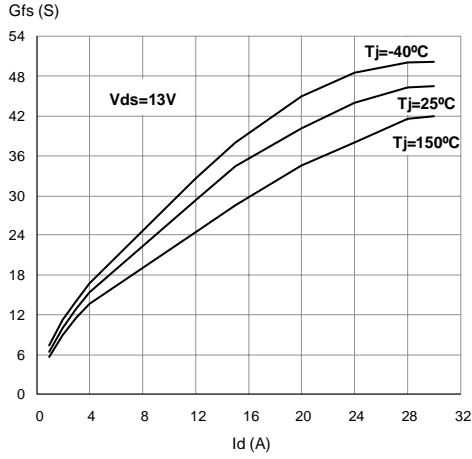
PowerSO-10 Static Drain-Source On Resistance Vs. Id



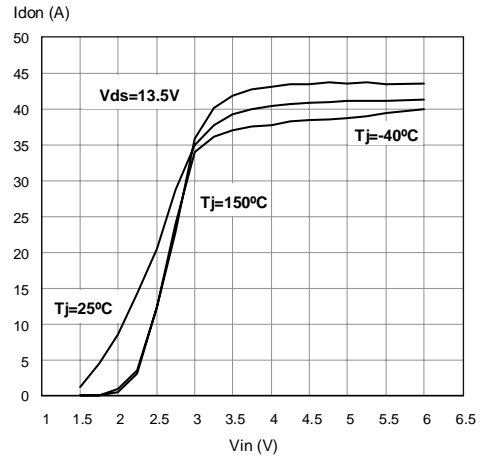
D2PAK, TO-220 & TO-247 Static Drain-Source On Resistance Vs. Id



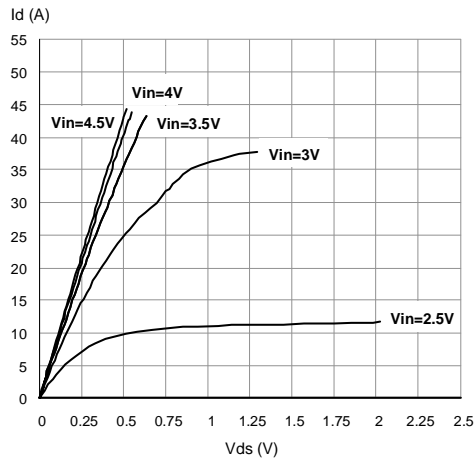
Transconductance



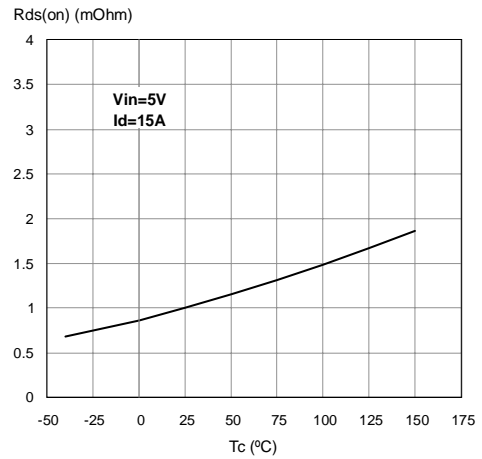
Transfer Characteristics



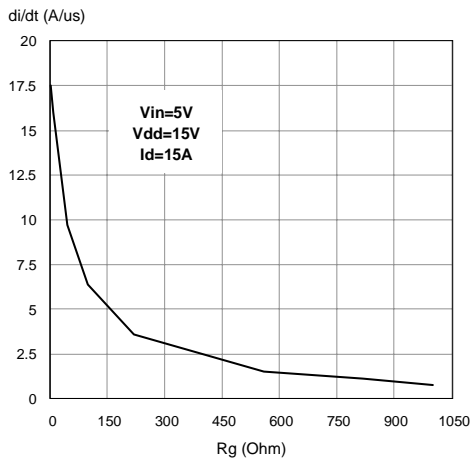
Output Characteristics



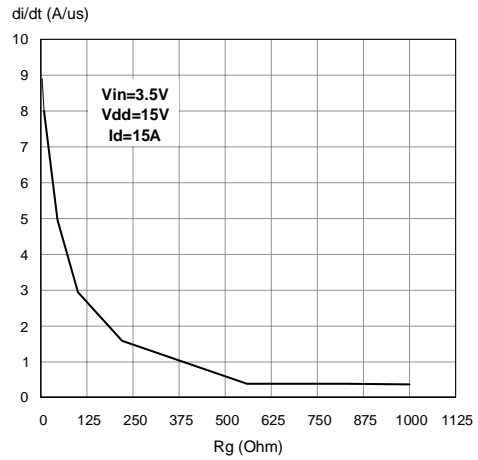
Normalized On Resistance Vs. Temperature



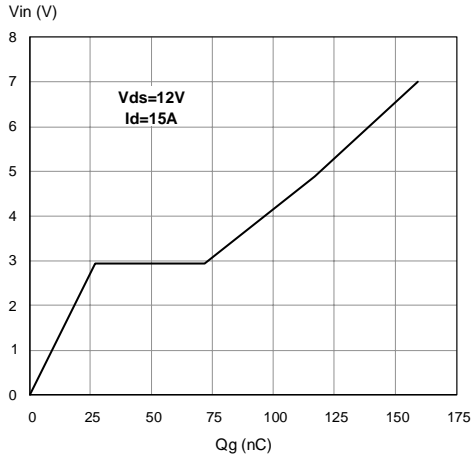
Turn On Current Slope



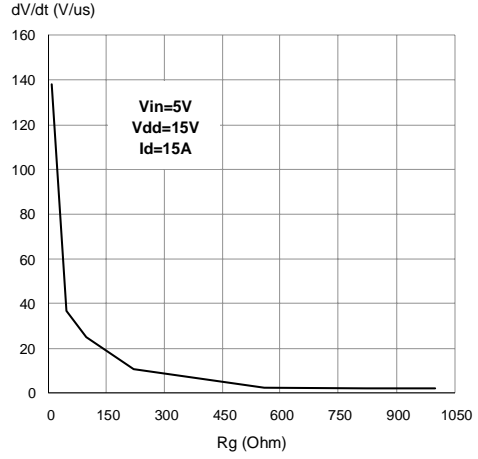
Turn On Current Slope



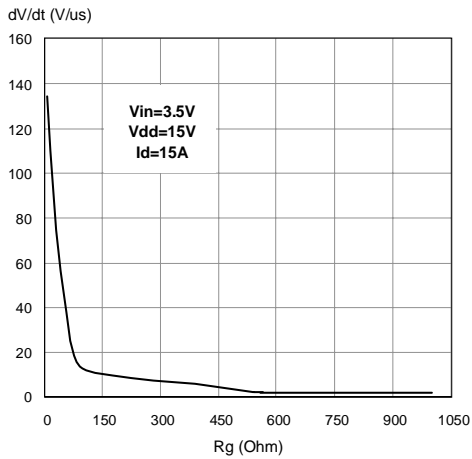
Input Voltage Vs. Input Charge



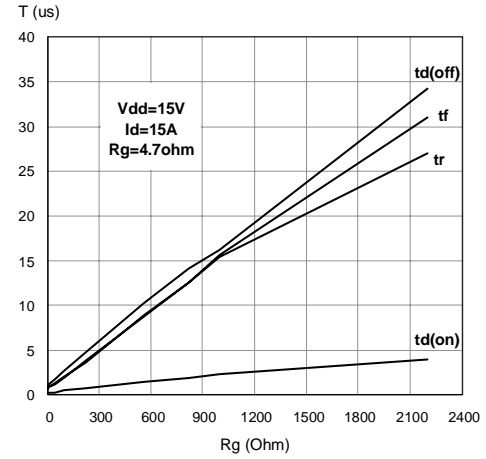
Turn off drain source voltage slope



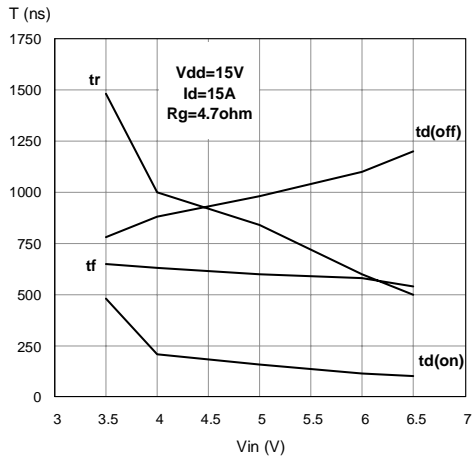
Turn Off Drain-Source Voltage Slope



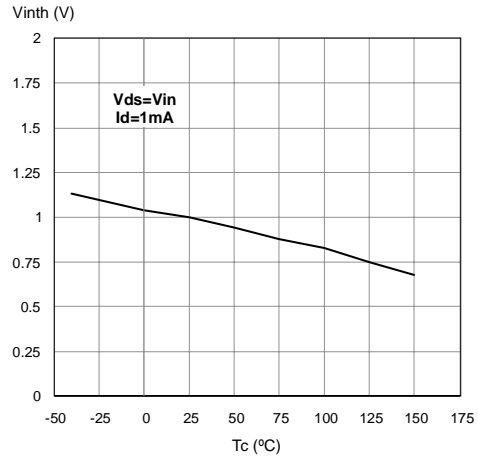
Switching Time Resistive Load



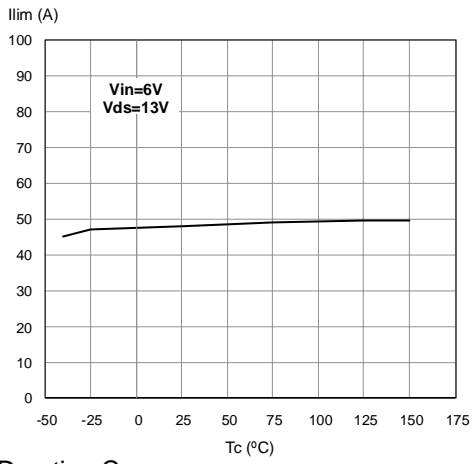
Switching Time Resistive Load



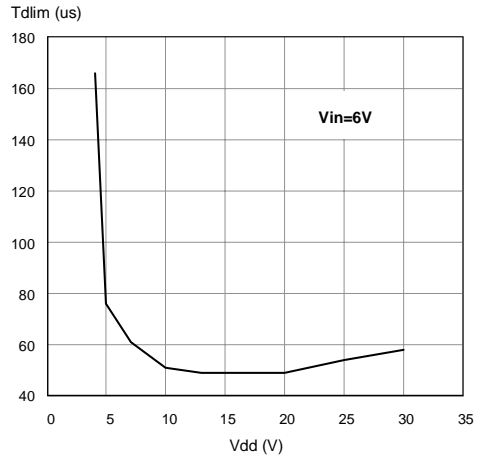
Normalized Input Threshold Voltage Vs. Temperature



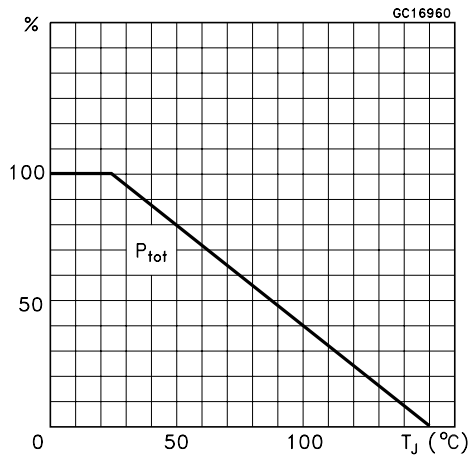
Current Limit Vs. Junction Temperature



Step Response Current Limit

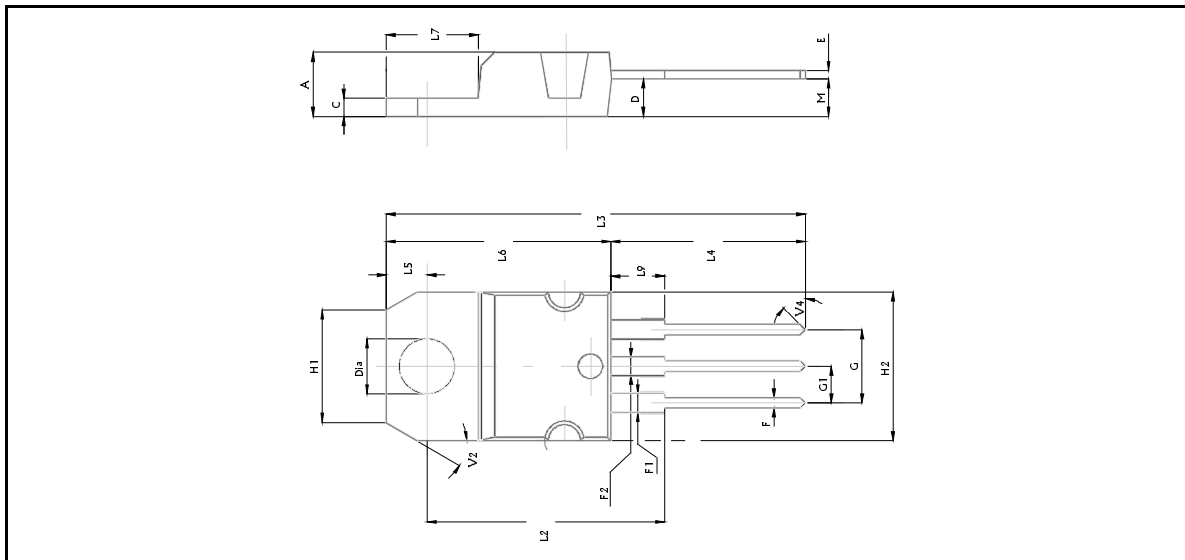


Derating Curve



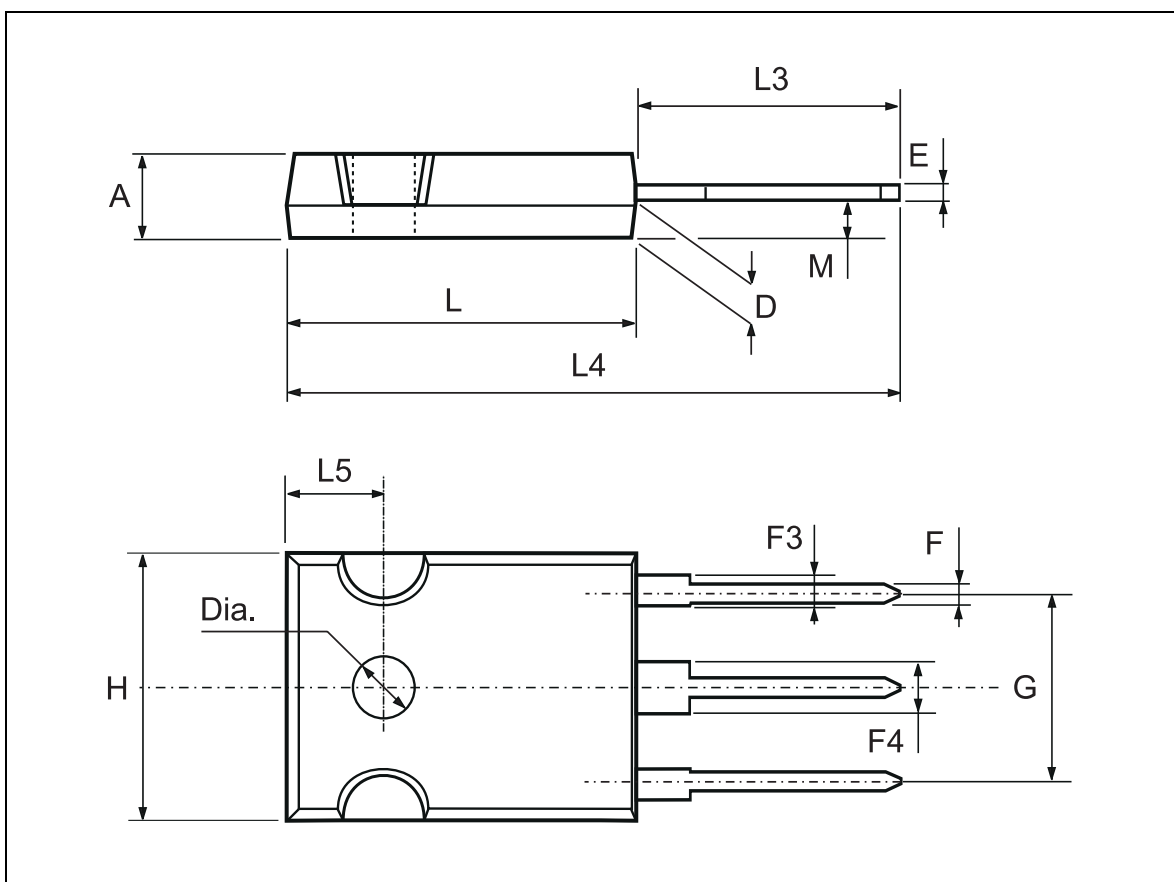
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137	0.154	
M		2.6			0.102	
DIA.	3.75		3.85	0.147		0.151



TO-247 MECHANICAL DATA

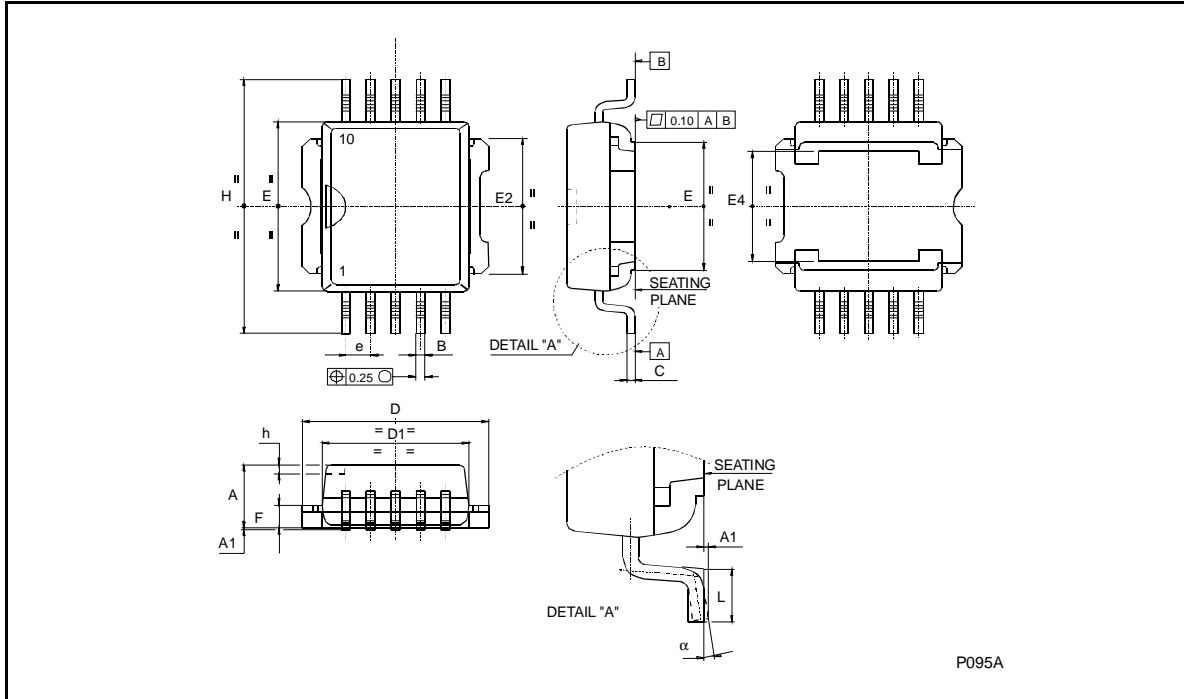
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118
Dia.	3.55		3.65	0.140		0.144



PowerSO-10™ MECHANICAL DATA

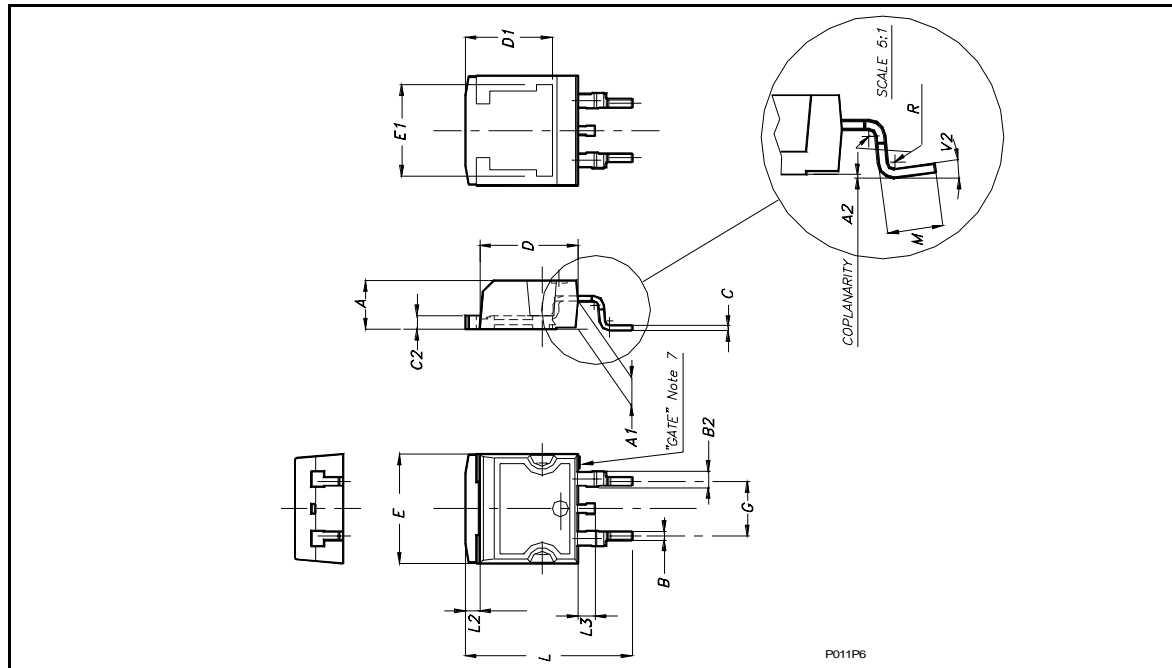
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

(*) Muar only POA P013P



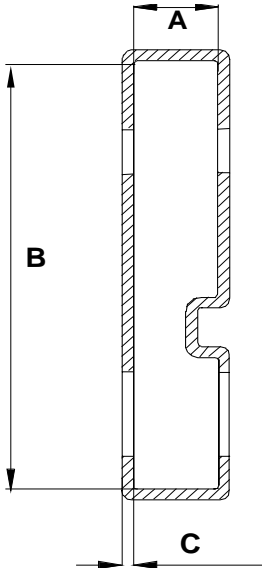
D²PAK MECHANICAL DATA

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.4		4.6
A1	2.49		2.69
A2	0.03		0.23
B	0.7		0.93
B2	1.14		1.7
C	0.45		0.6
C2	1.23		1.36
D	8.95		9.35
D1		8	
E	10		10.4
E1		8.5	
G	4.88		5.28
L	15		15.85
L2	1.27		1.4
L3	1.4		1.75
M	2.4		3.2
R		0.4	
V2	0°		8°



P011P6

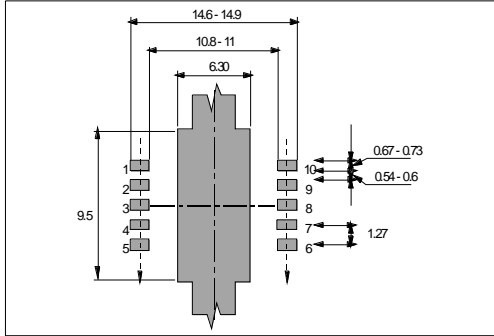
TO-220 TUBE SHIPMENT (no suffix)



Base Q.ty	50
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	5.5
B	31.4
C (± 0.1)	0.75

All dimensions are in mm.

PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (±0.5)	A	B	C (±0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")

REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

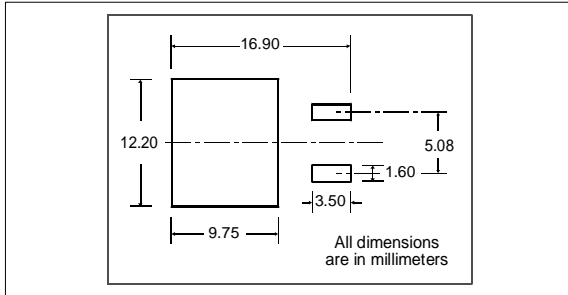
All dimensions are in mm.

TAPE DIMENSIONS
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

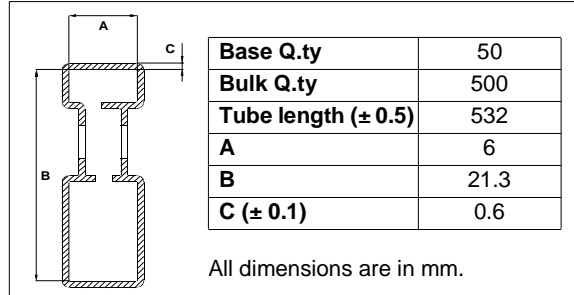
Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

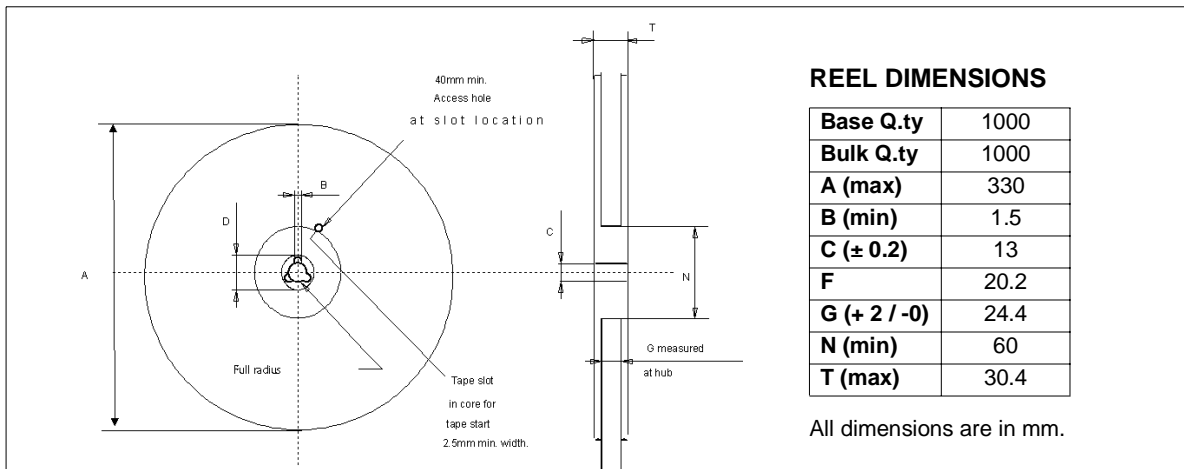
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)



TAPE AND REEL SHIPMENT (suffix "13TR")

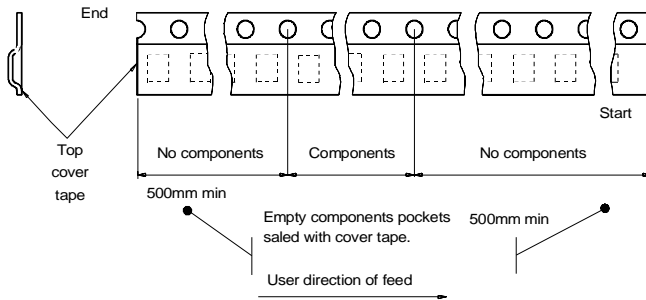
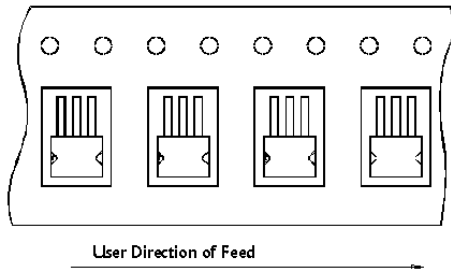
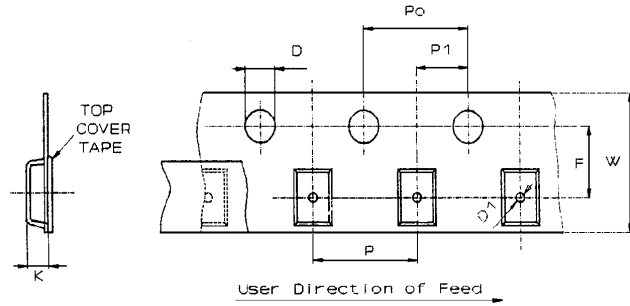


TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	16
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in ITALY- All Rights Reserved.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>

