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**Logic level TOPFET
SMD version of BUK118-50DL**

BUK129-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in **TOPFET2** technology assembled in a 3 pin surface mount plastic package.

APPLICATIONS

General purpose switch for driving

- lamps
- motors
- solenoids
- heaters

in automotive systems and other applications.

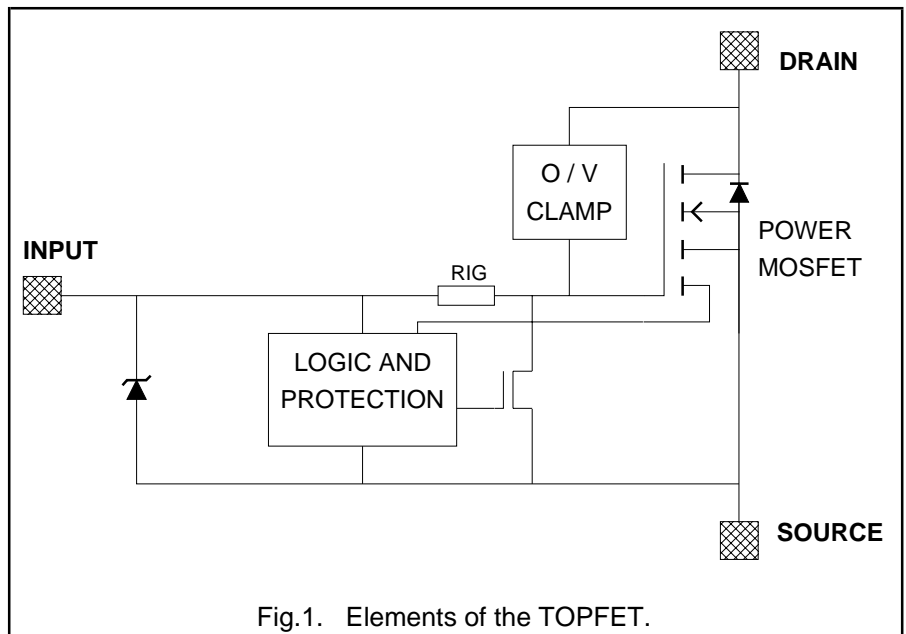
FEATURES

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	16	A
P_D	Total power dissipation	65	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	50	mΩ
I_{ISL}	Input supply current $V_{IS} = 5\text{ V}$	650	μA

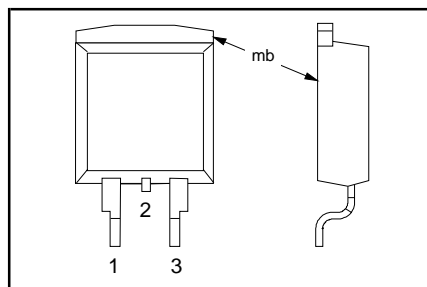
FUNCTIONAL BLOCK DIAGRAM



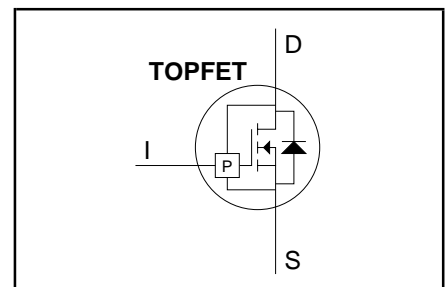
PINNING - SOT404

PIN	DESCRIPTION
1	input
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



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LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage ¹	-	-	50	V
I_D	Continuous drain current	$V_{IS} = 5 \text{ V}; T_{mb} = 25 \text{ }^\circ\text{C}$	-	self - limited	A
I_D	Continuous drain current	$V_{IS} = 5 \text{ V}; T_{mb} \leq 125 \text{ }^\circ\text{C}$	-	16	A
I_I	Continuous input current	-	-5	5	mA
I_{IRM}	Non-repetitive peak input current	$t_p \leq 1 \text{ ms}$	-10	10	mA
P_D	Total power dissipation	$T_{mb} \leq 25 \text{ }^\circ\text{C}$	-	65	W
T_{stg}	Storage temperature	-	-55	175	$^\circ\text{C}$
T_j	Continuous junction temperature ²	normal operation	-	150	$^\circ\text{C}$
T_{sold}	Case temperature	during soldering	-	260	$^\circ\text{C}$

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; $C = 250 \text{ pF}; R = 1.5 \text{ k}\Omega$	-	2	kV

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{DSM}	Inductive load turn-off Non-repetitive clamping energy	$I_{DM} = 16 \text{ A}; V_{DD} \leq 20 \text{ V}$ $T_{mb} \leq 25 \text{ }^\circ\text{C}$	-	200	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95 \text{ }^\circ\text{C}; f = 250 \text{ Hz}$	-	32	mJ

OVERLOAD PROTECTION LIMITING VALUE

With an adequate protection supply provided via the input pin, TOPFET can protect itself from two types of overload - overtemperature and short circuit load.

SYMBOL	PARAMETER	REQUIRED CONDITION	MIN.	MAX.	UNIT
V_{DS}	Drain source voltage ³	$4 \text{ V} \leq V_{IS} \leq 5.5 \text{ V}$	0	35	V

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th \text{ j-mb}}$	Thermal resistance Junction to mounting base	-	-	1.75	1.92	K/W
$R_{th \text{ j-a}}$	Junction to ambient	minimum footprint FR4 PCB	-	50	-	K/W

¹ Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

² A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

³ All control logic and protection functions are disabled during conduction of the source drain diode.

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OUTPUT CHARACTERISTICS
Limits are for $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$; typicals are for $T_{\text{mb}} = 25^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{CL})\text{DSS}}$	Off-state Drain-source clamping voltage	$V_{\text{IS}} = 0 \text{ V}$	50	-	-	V
		$I_{\text{D}} = 10 \text{ mA}$ $I_{\text{DM}} = 2 \text{ A}; t_{\text{p}} \leq 300 \mu\text{s}; \delta \leq 0.01$	50	60	70	V
I_{DSS}	Drain source leakage current	$V_{\text{DS}} = 40 \text{ V}$	-	-	100	μA
		$T_{\text{mb}} = 25^{\circ}\text{C}$	-	0.1	10	μA
$R_{\text{DS(ON)}}$	On-state Drain-source resistance	$I_{\text{DM}} = 6 \text{ A}; t_{\text{p}} \leq 300 \mu\text{s}; \delta \leq 0.01$	-	-	95	$\text{m}\Omega$
		$V_{\text{IS}} \geq 4.4 \text{ V}$	-	36	50	$\text{m}\Omega$
		$T_{\text{mb}} = 25^{\circ}\text{C}$	-	-	100	$\text{m}\Omega$
		$V_{\text{IS}} \geq 4 \text{ V}$	-	39	55	$\text{m}\Omega$

OVERLOAD CHARACTERISTICS
 $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{D}	Short circuit load Drain current limiting	$V_{\text{DS}} = 13 \text{ V}$	16	24	32	A
		$V_{\text{IS}} = 5 \text{ V};$ $4.4 \text{ V} \leq V_{\text{IS}} \leq 5.5 \text{ V}$	12	-	36	A
		$4 \text{ V} \leq V_{\text{IS}} \leq 5.5 \text{ V}$	8	-	36	A
$P_{\text{D(TO)}}$ T_{DSC}	Overload protection Overload power threshold Characteristic time	$V_{\text{IS}} = 5 \text{ V}; T_{\text{mb}} = 25^{\circ}\text{C}$	40	120	160	W
		device trips if $P_{\text{D}} > P_{\text{D(TO)}}$ which determines trip time ¹	200	350	600	μs
$T_{\text{j(TO)}}$	Overtemperature protection Threshold junction temperature ²		150	170	-	$^{\circ}\text{C}$

¹ Trip time $t_{\text{d,sc}}$ varies with overload dissipation P_{D} according to the formula $t_{\text{d,sc}} \approx T_{\text{DSC}} / \ln[P_{\text{D}} / P_{\text{D(TO)}}]$.

² This is independent of the dV/dt of input voltage V_{IS} .

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INPUT CHARACTERISTICS

The supply for the logic and overload protection is taken from the input.

Limits are for $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$; typicals are for $T_{\text{mb}} = 25^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{IS(TO)}}$	Input threshold voltage	$V_{\text{DS}} = 5 \text{ V}; I_{\text{D}} = 1 \text{ mA}$ $T_{\text{mb}} = 25^{\circ}\text{C}$	0.6	-	2.4	V
			1.1	1.6	2.1	V
I_{IS}	Input supply current	normal operation; $V_{\text{IS}} = 5 \text{ V}$ $V_{\text{IS}} = 4 \text{ V}$	100	220	400	μA
			80	195	330	μA
I_{ISL}	Input supply current	protection latched; $V_{\text{IS}} = 5 \text{ V}$ $V_{\text{IS}} = 3 \text{ V}$	200	400	650	μA
			130	250	430	μA
V_{ISR}	Protection reset voltage ¹	reset time $t_{\text{r}} \geq 100 \mu\text{s}$	1.5	2	2.9	V
t_{r}	Latch reset time	$V_{\text{IS1}} = 5 \text{ V}, V_{\text{IS2}} < 1 \text{ V}$	10	40	100	μs
$V_{\text{(CL)IS}}$	Input clamping voltage	$I_{\text{I}} = 1.5 \text{ mA}$	5.5	-	8.5	V
R_{IG}	Input series resistance ² to gate of power MOSFET	$T_{\text{mb}} = 25^{\circ}\text{C}$	-	33	-	$\text{k}\Omega$

SWITCHING CHARACTERISTICS

$T_{\text{mb}} = 25^{\circ}\text{C}$; $V_{\text{DD}} = 13 \text{ V}$; resistive load $R_{\text{L}} = 4 \Omega$. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{\text{d on}}$	Turn-on delay time	$V_{\text{IS}} = 5 \text{ V}$	-	15	30	μs
t_{r}	Rise time		-	30	60	μs
$t_{\text{d off}}$	Turn-off delay time	$V_{\text{IS}} = 0 \text{ V}$	-	70	140	μs
t_{f}	Fall time		-	35	70	μs

¹ The input voltage below which the overload protection circuits will be reset.

² Not directly measurable from device terminals.

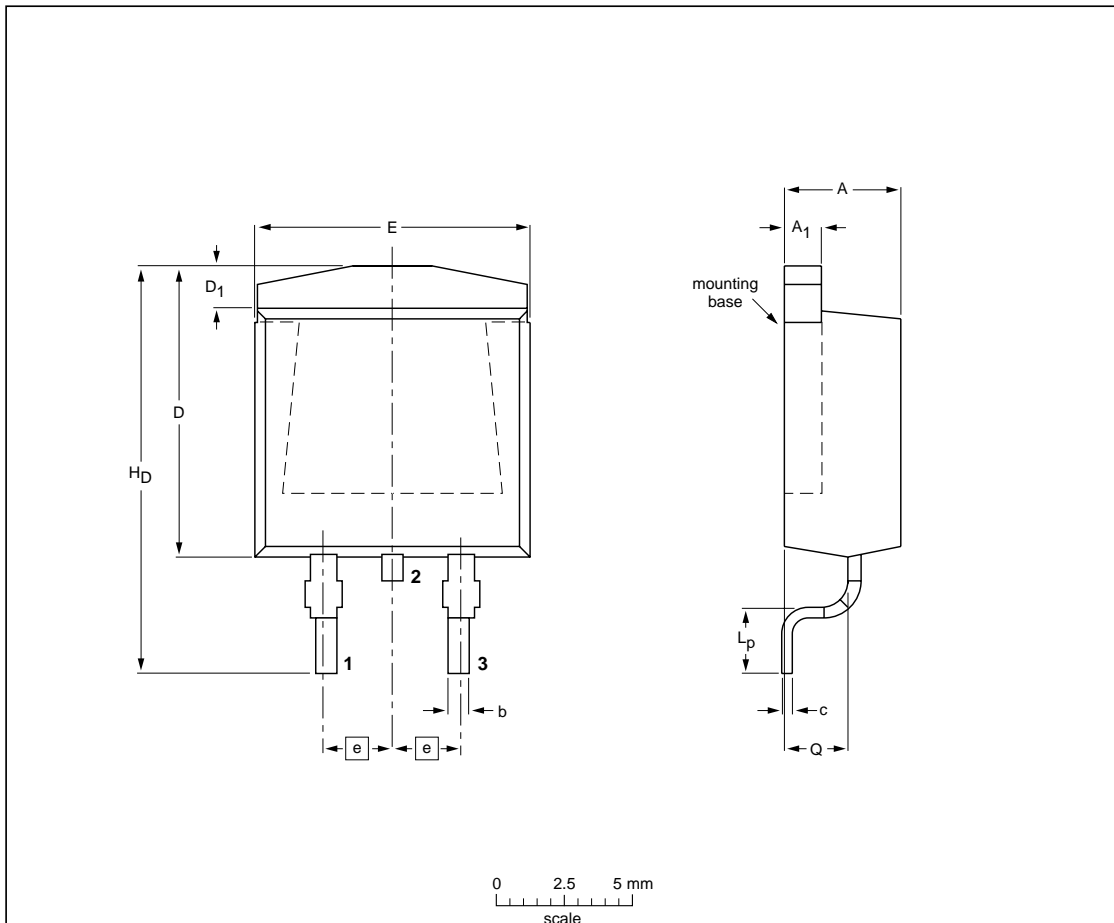
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MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.40 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT404					98-12-14 99-06-25

Fig.2. SOT404 surface mounting package¹, centre pin connected to mounting base.

¹ Epoxy meets UL94 V0 at 1/8". Net mass: 1.4 g

For soldering guidelines and SMD footprint design, please refer to Data Handbook SC18.

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DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS ¹	PRODUCT STATUS ²	DEFINITIONS
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