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Eight Channel Programmable High Voltage Ultrasound Transmit Beamformer

Features

- Eight channels with return to zero
- Up to ±70V output voltage
- ±3.0A output current
- Store up to four different patterns
- Independent programmable delays
- Single 11x11 QFN-80 package

Application

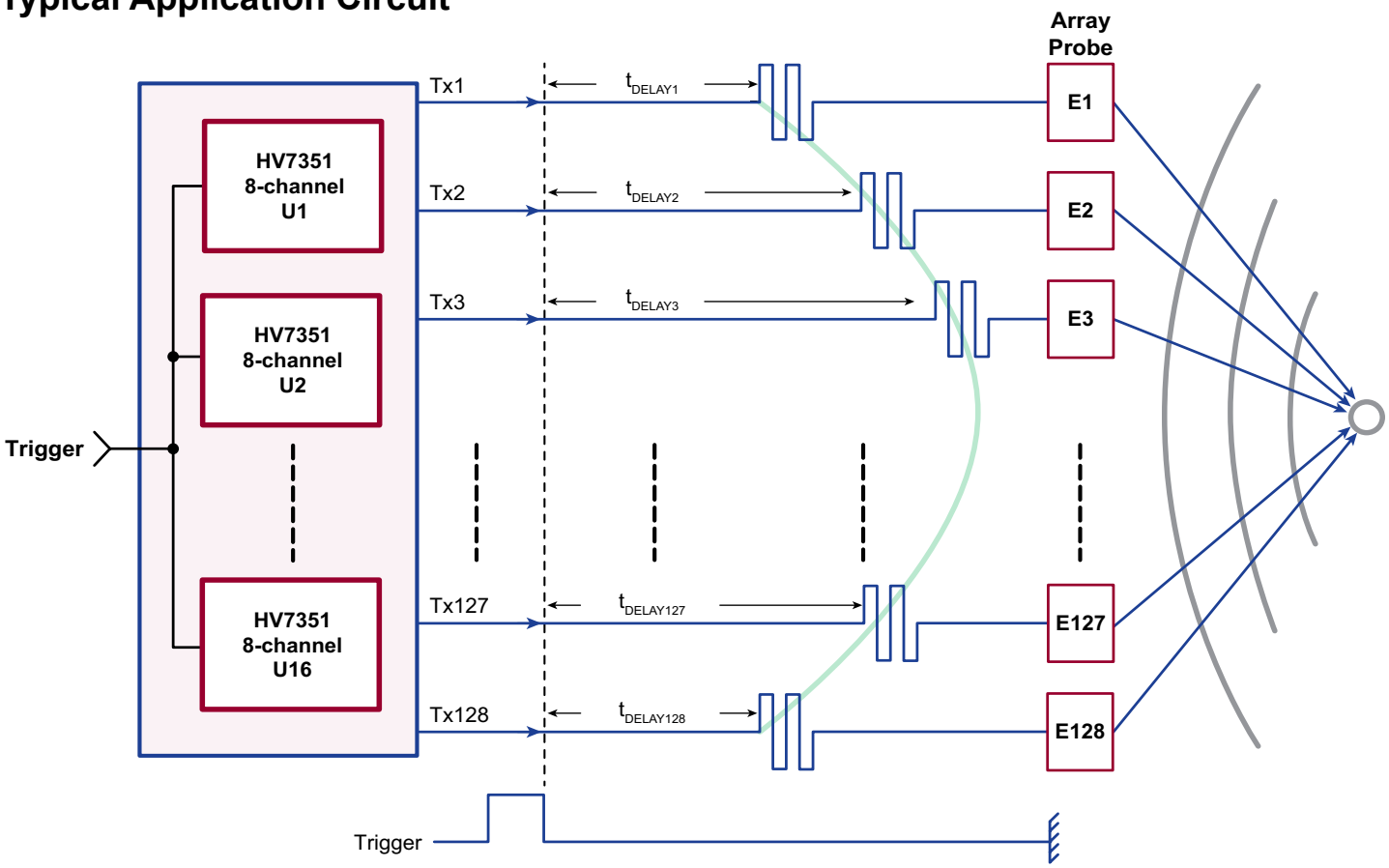
- Medical ultrasound imaging
- NDT, non-destructive testing
- Arbitrary pattern generator
- High speed PIN diode driver

General Description

The Supertex HV7351 is an 8-channel programmable high voltage ultrasound transmit beamformer. Each channel is capable of swinging up to ±70V with an active discharge back to 0V. The outputs can source and sink more than 3.0A to achieve fast output rise and fall times. The active discharge is also capable of sourcing and sinking 3.0A for a fast return to ground. The topology of the HV7351 will significantly reduce the number of I/O logic control lines needed.

Each pulser has four associated 64-bit shift registers for storing pre-determined transmit patterns and a 10-bit delay counter for controlling the transmit time. One of four arbitrary patterns can be transmitted with adjustable delay, depending on the data loaded into these shift registers and the delay counter. The delay counter can be clocked up to 200MHz, allowing incremental delays down to 5ns.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV7351K6-G	80-Lead QFN (11x11)	176/Tray

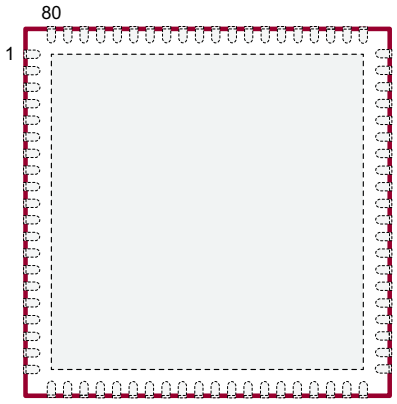
-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

Parameter	Value
V_{LL}, Positive logic supply	-0.5V to 5.5V
DV_{DD}, Positive logic supply voltage	-0.5V to 5.5V
PV_{DD}, Positive gate drive supply voltage	-0.5V to 5.5V
AV_{DD}, Positive analog supply voltage	-0.5V to 5.5V
PV_{SS}, Negative gate drive supply voltage	+0.5V to -5.5V
V_{PP}, High voltage positive supply voltage	-0.5V to +80V
V_{NN}, High voltage negative supply voltage	+0.5V to -80V
(V_{PP} - V_{NN}), Differential high voltage supply	+160V
V_{PF}, Positive floating supply voltage	V_{PP} - 6.0V to V_{PP}
V_{NF}, Negative floating supply voltage	V_{NN} to V_{NN} +6.0V
V_{RP}, Positive supply for V_{NF} regulator	0V to 15V
V_{RN}, Negative supply for V_{PF} regulator	0V to -15V
Operating temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



80-Lead QFN
(top view)

Package Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or 

80-Lead QFN

Typical Thermal Resistance

Package	θ_{ja}
80-Lead QFN	14°C/W

Operating Supply Voltages

(T_J = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	Positive high voltage supply	3.0	-	70	V	---
V_{NN}	Negative high voltage supply	-70	-	-3.0	V	---
V_{LL}	Logic interface voltage	2.85	3.30	3.6	V	---
AV_{DD}	Low voltage positive analog supply voltage	4.75	5.00	5.25	V	---
DV_{DD}	Low voltage positive digital supply voltage	4.75	5.00	5.25	V	---
PV_{DD}	Low voltage positive gate drive supply voltage	4.75	5.00	5.25	V	---
PV_{SS}	Low voltage negative gate drive supply voltage	-5.25	-5.00	-4.75	V	---

Operating Supply Voltages *(cont.)*

(T_J = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{RP}	Low voltage positive supply for VNF regulator	4.75	-	12	V	---
V_{RN}	Low voltage negative supply for VPF regulator	-12	-	-4.75	V	---
$\overline{TCK}$	Reference voltage logic trip point for TCK pin	$0.4V_{LL}$	$0.5V_{LL}$	$0.6V_{LL}$	V	---
$I_{\overline{TCK}}$	$\overline{TCK}$ input current	-	-	±10	µA	$V_{\overline{TCK}}$ = 0 to V_{LL}

Regulator Outputs

(Operating conditions unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_J =25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{PF}	Positive floating gate drive voltage	V_{PP} -5.25	V_{PP} -5.00	V_{PP} -4.00	V	4.0µF ceramic capacitor across V_{PF} and V_{PP}
V_{NF}	Negative floating gate drive voltage	V_{NN} +4.00	V_{NN} +5.00	V_{NN} +5.25	V	4.0µF ceramic capacitor across V_{NF} and V_{NN}

Electrical Characteristics

(Operating conditions unless otherwise specified, V_{LL} =3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_J = 25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{VLLQ}	V_{LL} quiescent current	-	384	500	µA	EN = Low, all inputs are static
I_{AVDDQ}	AV_{DD} quiescent current	-	12	30	µA	EN = Low, all inputs are static
I_{DVDDQ}	DV_{DD} quiescent current	-	12	30		
I_{PVDDQ}	PV_{DD} quiescent current	-	70	100		
I_{VRPQ}	V_{RP} quiescent current	-	0.3	6.0	µA	EN = Low, all inputs are static
I_{VRNQ}	V_{RN} quiescent current	-	-0.01	6.0		
I_{PVSSQ}	PV_{SS} quiescent current	-85	-45	-	µA	EN = Low, all inputs are static
I_{VPPQ}	V_{PP} quiescent current	-	2.6	6.0	µA	EN = Low, all inputs are static
I_{VNNQ}	V_{NN} quiescent current	-	-1.6	6.0		
I_{VLLEN}	V_{LL} enabled quiescent current	-	390	500	µA	EN = High, all inputs are static
I_{AVDDEN}	AV_{DD} enabled quiescent current	-	600	800	µA	EN = High, all inputs are static
I_{DVDDEN}	DV_{DD} enabled quiescent current	-	22	55		
I_{PVDDEN}	PV_{DD} enabled quiescent current	-	44	100	µA	EN = High, all inputs are static
I_{VRPEN}	V_{RP} enabled quiescent current	-	450	650	µA	EN = High, all inputs are static
I_{VRNEN}	V_{RN} enabled quiescent current	-650	-350	-		
I_{PVSSEN}	PV_{SS} enabled quiescent current	-100	-44	-	µA	EN = High, all inputs are static
I_{VPPEN}	V_{PP} enabled quiescent current	-	370	620	µA	EN = High, all inputs are static
I_{VNNEN}	V_{NN} enabled quiescent current	-620	-420	-		

Electrical Characteristics *(cont.)*

(Operating conditions unless otherwise specified, V_{LL} =3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_J = 25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{VLLCW}	V_{LL} current at TCK = 80MHz	-	500	-	µA	V_{PP} = +5.0V, V_{NN} = -5.0V, EN = High, CW = High, 80MHz on TCK, 0.5V_{LL} on $\overline{TCK}$, all 8 channels active at 5.0MHz, No load
I_{DVDDCW}	DV_{DD} current at CW = 5MHz	-	25	-	mA	
I_{VPPCW}	V_{PP} current at CW = 5MHz	-	141	-	mA	
I_{VNNCW}	V_{NN} current at CW = 5MHz	-	98	-	mA	

AC Electrical Characteristics

(Operating conditions unless otherwise specified, V_{LL} = 3.3V, AV_{DD} = DV_{DD} = PV_{DD} = V_{RP} = 5.0V, PV_{SS} = V_{RN} = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_J = 25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
f_{TCK}	Transmit clock frequency	0	-	200	MHz	---
f_{SCK}	Serial clock frequency	0	-	80	MHz	No daisy chain
		0	-	70		Daisy chained
t_{SU-DIN}	Set-up time data in to SCK	2.0	1.0	-	ns	---
t_{H-DIN}	Hold time SCK to data in	2.0	1.0	-	ns	---
$t_{SU-\overline{CS1}}$	Set-up time $\overline{CS1}$ low to SCK	2.0	-	-	ns	---
$t_{SU-\overline{CS2}}$	Set-up time $\overline{CS2}$ low to SCK	2.0	-	-	ns	---
$t_{SU-TRIG}$	Set-up time TRIG low to TCK	2.0	-	-	ns	---
t_{W-TRIG}	TRIG pulse width	2TCK	-	-	-	---
t_{LHDO}	SCK to data out low to high delay time	3.0	9.0	12	ns	For D_{OUT}1
		3.0	9.0	10		For D_{OUT}2
t_{HLDO}	SCK to data out high to low delay time	3.0	9.0	12	ns	For D_{OUT}1
		3.0	9.0	10		For D_{OUT}2
t_{WA1A0}	A1A0 pulse width	t_{W-TRIG} +40	-	-	ns	---
t_{SUA1A0}	Set-up time A1A0 to TRIG rising edge	-	20	-		
t_{HA1A0}	Hold time A1A0 to TRIG falling edge	-	20	-		
t_{EN-ON}	Device enable time	-	1.0	-	ms	1.0µF capacitor on every VPF and VNF pin.
t_{EN-OFF}	Device disable time	-	-	100	ns	---
t_{r1}	Output rise time from 0V to +HV	-	9.0	13	ns	Load = 330pF//2.5kΩ
t_{f1}	Output fall time from 0V to -HV	-	9.0	13		
t_{r2}	Damping output rise time from -HV to 0V	-	9.0	13		
t_{f2}	Damping output fall time from +HV to 0V	-	9.0	13		
t_{r3}	Output rise time from -HV to +HV	-	17	23		
t_{f3}	Output fall time from +HV to -HV	-	17	23		
t_{rcw}	CW output rise time	-	9.0	16	ns	V_{PP} = +5.0V, V_{NN} = -5.0V, Load = 330pF//2.5kΩ
t_{fcw}	CW output fall time	-	9.0	16		

AC Electrical Characteristics *(cont.)*

(Operating conditions unless otherwise specified, V_{LL} =3.3V, $AV_{DD} = DV_{DD} = PV_{DD} = V_{RP}$ = 5.0V, $PV_{SS} = V_{RN}$ = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_J = 25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
t_{dr1}	Output propagation delay rise time 1	10.85	13.35	15.85	ns	No Load.
t_{df1}	Output propagation delay fall time 1	11.35	13.85	16.35		
t_{dr2}	Output propagation delay rise time 2	11.25	13.75	16.25		
t_{df2}	Output propagation delay fall time 2	11.75	14.25	16.75		
t_{dr3}	Output propagation delay rise time 3	11.35	13.85	16.35		
t_{df3}	Output propagation delay fall time 3	11.45	13.95	16.45		
t_{dcwlh}	CW output propagation delay time from low to high	10.45	12.95	15.45	ns	V_{PP} = +5.0V, V_{NN} = -5.0V, No Load
t_{dcwhl}	CW output propagation delay time from high to low	10.35	12.85	15.35		
Δt_{dcwhl}	Delay time matching	-	±0.7	-	ns	P to N, channel-to-channel matching
t_{JCW}	Delay jitter on rise or fall	-	13	-	ps	V_{PP} = +5.0V, V_{NN} = -5.0V, Load = 50Ω
LAT	Latency	3.5TCK	3.5TCK	3.5TCK	-	---
Output P-channel MOSFET to V_{PP}, CW = 0						
I_{OUT}	Output saturation current	2.2	3.2	-	A	---
R_{ON}	Output ON-resistance	-	4.2	-	Ω	I_{OUT} = 100mA
C_{OSS}	Output capacitance	-	62	-	pF	V_{PP} - V_{OUT} = 25V, f = 1.0MHz
Output N-channel MOSFET to V_{NN}, CW = 0						
I_{OUT}	Output saturation current	-	-3.2	-2.2	A	---
R_{ON}	Output ON-resistance	-	2.4	-	Ω	I_{OUT} = -100mA
C_{OSS}	Output capacitance	-	50	-	pF	V_{NN} - V_{OUT} = -25V, f = 1.0MHz
Output P-channel MOSFET to V_{PP}, CW = 1						
I_{OUT}	Output saturation current	1.2	1.5	-	A	---
R_{ON}	Output ON-resistance	-	8.0	-	Ω	I_{OUT} = 100mA
C_{OSS}	Output capacitance	-	62	-	pF	V_{PP} - V_{OUT} = 25V, f = 1.0MHz
Output N-channel MOSFET to V_{NN}, CW = 1						
I_{OUT}	Output saturation current	-	-1.5	-1.2	A	---
R_{ON}	Output ON-resistance	-	6.6	-	Ω	I_{OUT} = -100mA
C_{OSS}	Output capacitance	-	50	-	pF	V_{NN} - V_{OUT} = -25V, f = 1.0MHz

AC Electrical Characteristics *(cont.)*

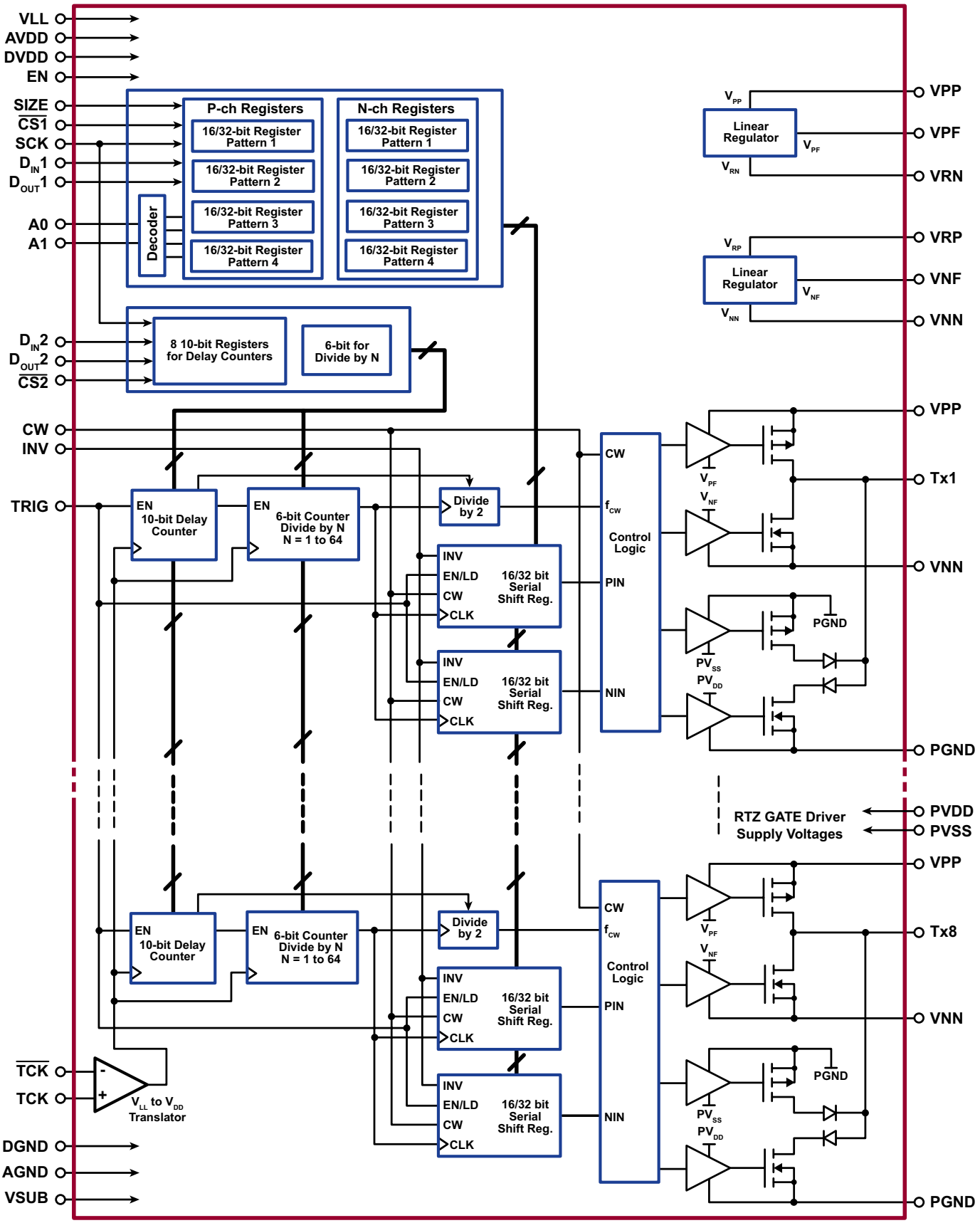
(Operating conditions unless otherwise specified, V_{LL} =3.3V, $AV_{DD} = DV_{DD} = PV_{DD} = V_{RP}$ = 5.0V, $PV_{SS} = V_{RN}$ = -5.0V, V_{PP} = +70V, V_{NN} = -70V, T_J = 25ºC)

Sym	Parameter	Min	Typ	Max	Units	Conditions
Damping P-channel MOSFET to PGND						
I_{OUT}	Output saturation current	2.2	3.2	-	A	---
R_{ON}	Output ON-resistance	-	4.0	-	Ω	I_{OUT} = 100mA
C_{OSS}	Output capacitance	-	62	-	pF	V_{PP} - V_{OUT} = 25V, f = 1.0MHz
Damping N-channel MOSFET to PGND						
I_{OUT}	Output saturation current	-	-3.2	-2.2	A	---
R_{ON}	Output ON-resistance	-	2.3	-	Ω	I_{OUT} = -100mA
C_{OSS}	Output capacitance	-	50	-	pF	V_{NN} - V_{OUT} = -25V, f = 1.0MHz
Logic Inputs						
$I_{\overline{TCK}}$	Input current for $\overline{TCK}$	-	±1.0	-	µA	$V_{\overline{TCK}}$ = 0 to V_{LL}
V_{IH}	Input logic high voltage for TCK	$\overline{TCK}$ +0.15	$\overline{TCK}$	V_{LL}	V	Only for $\overline{TCK}$ input, TCK = 0.5V_{LL}
V_{IL}	Input logic low voltage for TCK	0	$\overline{TCK}$	$\overline{TCK}$ -0.15	V	Only for $\overline{TCK}$ input, TCK = 0.5V_{LL}
V_{IH}	Input logic high voltage	0.8V_{LL}	-	V_{LL}	V	For all logic inputs except TCK
V_{IL}	Input logic low voltage	0	-	0.2V_{LL}	V	For all logic inputs except TCK
I_{IH}	Input logic high current	-	-	1.0	µA	---
I_{IL}	Input logic low current	-1.0	-	-	µA	---
V_{OL}	Output logic low voltage	0	-	0.7	V	I_{OUT} = 0 to -10mA
V_{OH}	Output logic high voltage	V_{LL} -0.7	-	V_{LL}	V	I_{OUT} = 0 to 10mA
C_{IN}	Input logic capacitance	-	-	5.0	pF	---

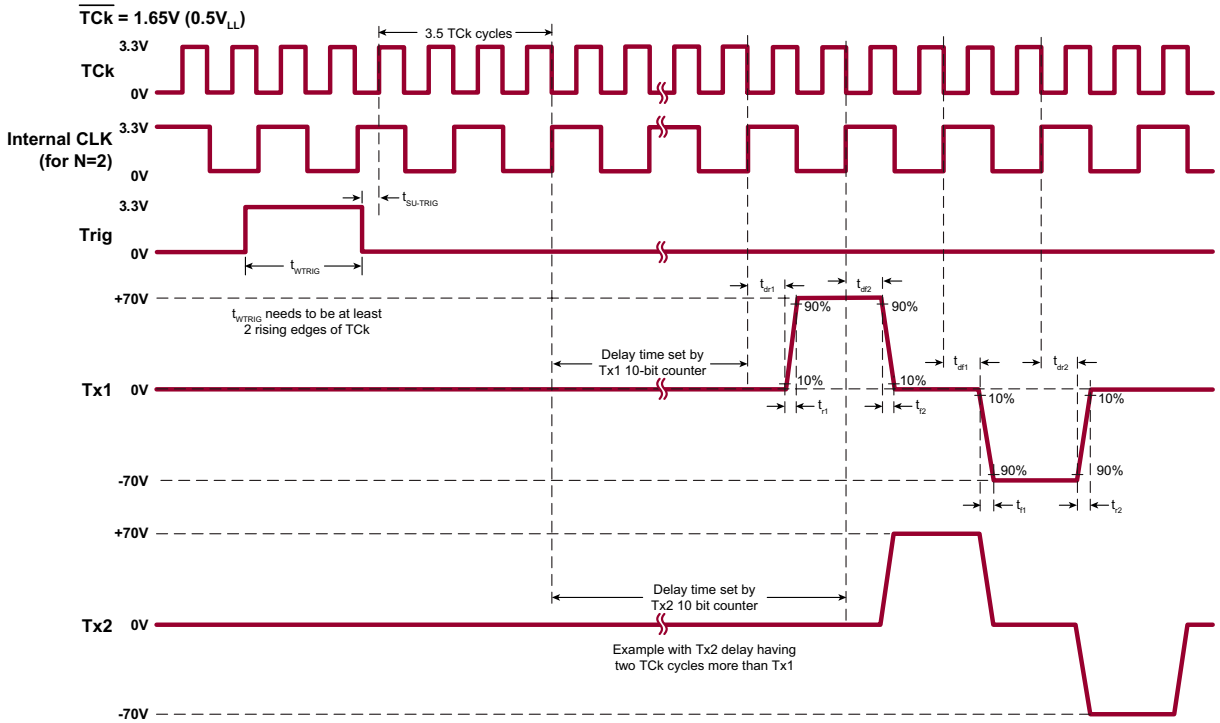
Logic Truth Table

Mode	Inputs						Outputs			Comments
	EN	CW	10-bit Counter	INV	NIN	PIN	N-ch	P-ch	RTZ	
Non-CW mode. Outputs not inverted. Outputs are controlled by data in the shift registers	1	0	X	X	0	0	OFF	OFF	ON	RTZ (return-to-zero) is activated when NIN and PIN are both low. Output is pulled to ground through a series diode.
	1	0	X	0	0	1	OFF	ON	OFF	Not inverted. Logic 1 in the P-channel register turns on the output P-channel MOSFET.
	1	0	X	0	1	0	ON	OFF	OFF	Not inverted. Logic 1 in the N-channel register turns on the output N-channel MOSFET.
	1	0	X	X	1	1	OFF	OFF	OFF	Avoids cross over current. A logic 1 in both P- and N-channel registers will put the output in a Hi-Z state.
Non-CW mode. Outputs are inverted. Outputs are controlled by data in the shift registers	1	0	X	1	0	1	ON	OFF	OFF	Inverted, for harmonic imaging
	1	0	X	1	1	0	OFF	ON	OFF	Inverted, for harmonic imaging
CW mode. Output follows fcw	1	X	All 1	X	X	X	OFF	OFF	OFF	Off channels are the ones with all 1's in their respective 10-bit counters. Output follows the f_{CW} signal. Shift registers for NIN and PIN should remain static to save power.
	1	1	Not all 1	X	X	X	OFF/ ON	ON/ OFF	OFF	
Device Disabled	0	X	X	X	X	X	OFF	OFF	OFF	Hi-Z state

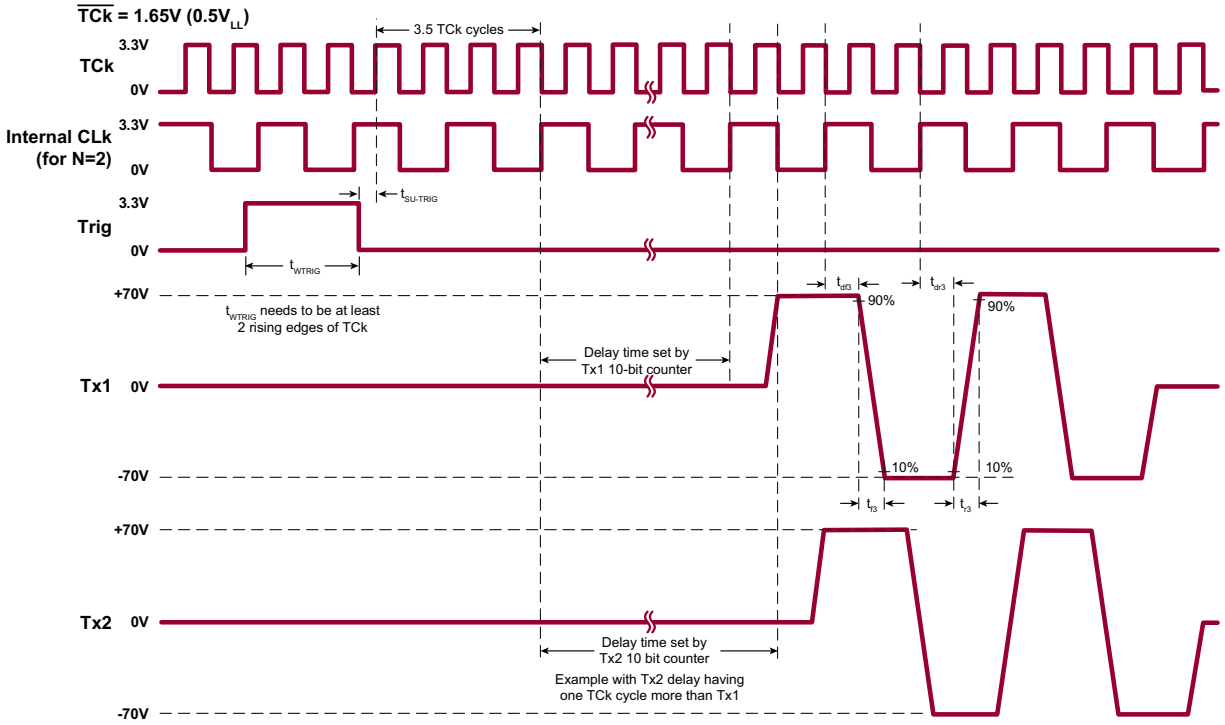
Block Diagram



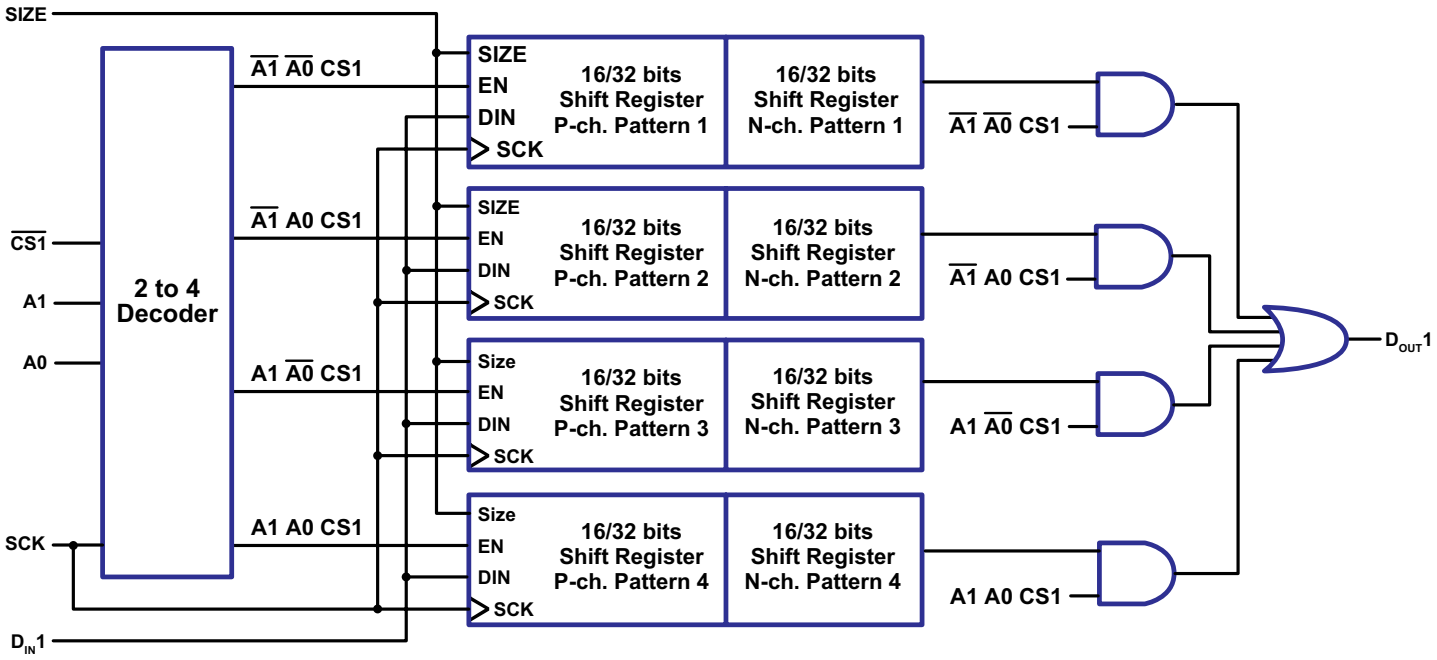
Timing Diagram 1



Timing Diagram 2



Pattern Register Circuit Diagram



Loading Data into the Four 16/32 bit Pattern Registers

A detailed circuit diagram of the pattern registers is shown above. There are 4 programmable patterns that can be stored. One of four patterns can be selected via the two input logic decoder pins, A1 and A0. Data can be loaded on the selected pattern. Each pattern can be either 16 or 32 bits wide. The SIZE pin determines whether they are 16 or 32 bits wide. SIZE = H will set the pattern to be 32 bits wide while SIZE = L will set it to 16 bits wide. $D_{IN}1$ is the input data for the register. When $\overline{CS1}$ is high, data will not be shifted in. Data is shifted in only when $\overline{CS1}$ is low.

With SIZE = H, the circuit is effectively a 64-bit serial shift register. The data first enters into the P-channel register and continues to be shifted though to the N-channel register. Data is clocked in during the rising edge of the clock. There is no activity during the falling edge of the clock. The data, $D_{IN}1$, enters from the P-channel register and exits from the N-channel register from $D_{OUT}1$.

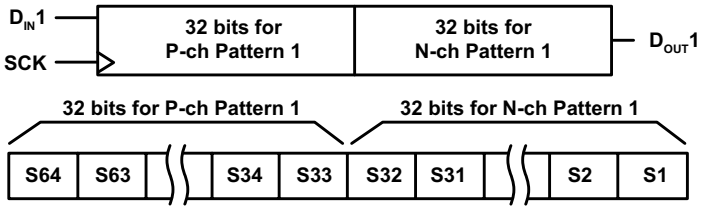
For size = High, 32 bits wide (size = Low, 16-bits wide)

A1 = A0 = Low, Pattern 1 selected

$\overline{CS1}$ = Low, data can be shifted in

64-bit serial shift register: 32 bits for the P-channel and 32 bits for the N-channel

Data is shifted in during the rising edge of the clock. S1 is the first bit shifted in, entering the P-channel register. After 64 clock cycles, S1 will be located in the N-channel register as shown below. It will also be clocked out to $D_{OUT}1$.



A 2-to-4 decoder is provided to select which of the four patterns is to be used for all of the outputs. Logic inputs A1 and A0 determine which patterns are selected per the decoder truth table shown below. Once A1 and A0 are set, a rising edge on the trigger logic input pin will automatically load the selected pattern to all of the outputs.

Decoder Truth Table

Logic Decoder Input		Pattern Selected
A1	A0	
0	0	1
0	1	2
1	0	3
1	1	4

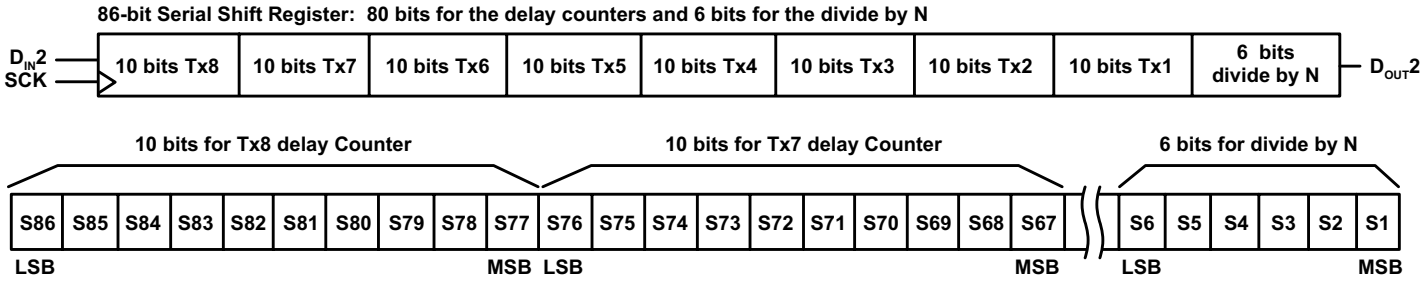
Loading Data into the Delay Counters and the Divide-by-N Counter

Each output channel, TX, has its own programmable 10-bit delay counter. For 8 channels, 80 bits are needed. A 6-bit divide-by-N counter is also provided to program the desired TX frequency. To program all the individual delay counters and the divide-by-N counter, an 86-bit serial shift register is provided. It uses the same clock input that the pattern registers uses. DIN2 is the input data for this register. When $\overline{CS2}$ is high, data will not be shifted in. Data is shifted in only when $\overline{CS2}$ is low.

As shown below, the data first enters into the 10-bit register for the TX8 delay counter and continues to be shifted though to the 6-bit register for the divide by N counter. Data is clocked in during the rising edge of the clock. There is no activity during the falling edge of the clock. The MSB bit in the 6-bit divide-by-N register is clocked out into DOUT2 for cascading multiple devices if desired.

10-Bit Delay Counter

The input clock for the 10-bit delay counter is the TCK pin. The TCK pin is the only pin that is capable of high frequency, 200MHz. This helps maximum delay time resolution. The counter counts upward. Please refer to the table below.



Delay Counter Table

MSB									LSB	Delay Time
0	0	0	0	0	0	0	0	0	0	1023 TCK cycles
0	0	0	0	0	0	0	0	0	1	1022 TCK cycles
0	0	0	0	0	0	0	0	1	0	1021 TCK cycles
0	0	0	0	0	0	0	0	1	1	1020 TCK cycles
I I I	I I I	I I I	I I I	I I I	I I I	I I I	I I I	I I I	I I I	I I I
1	1	1	1	1	1	1	1	0	0	3 TCK cycles
1	1	1	1	1	1	1	1	0	1	2 TCK cycles
1	1	1	1	1	1	1	1	1	0	1 TCK cycle
1	1	1	1	1	1	1	1	1	1	No trigger

6-Bit Divide-by-N Counter

The input clock for the 6-bit divide-by-N counter is the TCK pin. It generates the clock frequency for the 16/32 bit serial shift register for the output P- and N-channel patterns. Each clock cycle will set the TX output to be either at V_{PP}, V_{NN}, ground, or high impedance depending on what was preprogrammed in their corresponding registers.

MSB					LSB	Output Shift Register Clock Frequency
0	0	0	0	0	0	$f_{TCK} \div 64$
0	0	0	0	0	1	$f_{TCK} \div 63$
0	0	0	0	1	0	$f_{TCK} \div 62$
0	0	0	0	1	1	$f_{TCK} \div 61$
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	0	$f_{TCK} \div 4$
1	1	1	1	0	1	$f_{TCK} \div 3$
1	1	1	1	1	0	$f_{TCK} \div 2$
1	1	1	1	1	1	$f_{TCK} \div 1$

Pin Description

Pin	Name	Description
1	AVDD	Positive analog supply voltage (+5.0V).
2	DIN2	Serial data in for delay counters and frequency divider.
3	$\overline{CS2}$	Activates DIN2. Input logic high = off, input logic low = on.
4	SIZE	Sets pattern width to either 16-bits or 32-bits. Logic low = 16-bits, logic high = 32-bits.
5	INV	Inverts the TX output waveform. See logic truth table for details.
6	CW	Activates CW mode. Logic low = non-CW mode, logic high = CW mode. See logic truth table for details.
7	DOUT2	Data out for delay counters and frequency divider.
8	EN	Enables and disables device. Logic low = off, logic high = on.
9	SCK	Serial clock input for serial shift registers.
10	DVDD	Positive digital supply voltage (+5.0V).
11	DGND	Digital ground.
12	TRIG	Toggles all TX outputs to transmit. Needs to be high for 2 rising edges of TCK. Delay counters will start on the rising edge of the TCK pin right after the falling edge of the TRIG signal. See timing diagram for details.
13	TCK	Transmitter clock for the delay counters and input frequency for the divide by N. Can be CMOS, LVDS, or SSTL.
14	$\overline{TCK}$	Logic trip point TCK. Can be set to a DC value from $0.4V_{LL}$ to $0.6V_{LL}$ or driven differentially with TCK.
15	VLL	Logic interface supply voltage (3.0V or 3.3V).
16	$\overline{CS1}$	Activates DIN1. Input logic high = off, input logic low = on.
17	DOUT1	Data out for P-channel and N-channel pattern registers.

Pin Description *(cont.)*

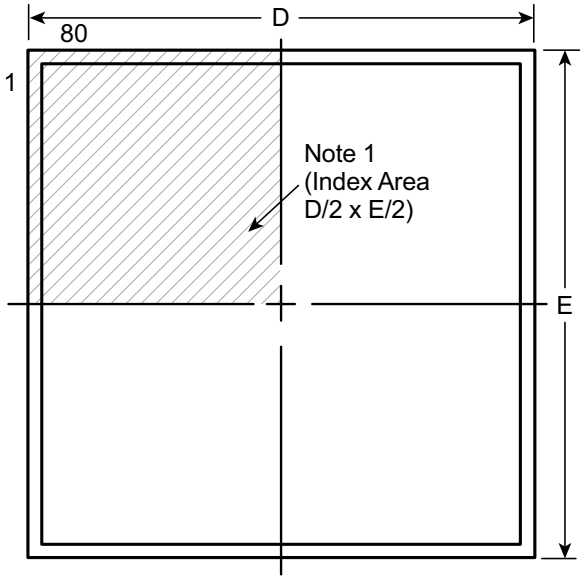
Pin	Name	Description
18	A0	Decoded to select 1 of 4 patterns to be loaded.
19	A1	
20	DIN1	Serial data in for P-channel and N-channel pattern registers.
21	VRN	Negative supply for VPF regulator (-5.0V).
22	PVDD	Positive gate drive supply voltage for RTZ output transistors (+5.0V).
23	PGND	Power ground path for RTZ output transistors.
24	PGND	
25	PVSS	Negative gate drive supply voltage for RTZ output transistors (-5.0V).
26	VPF	Linear regulator output gate drive voltage for the P-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VPF and VPP pin. There are four in total.
27	NC	No connection.
28	VNF	Linear regulator output gate drive voltage for the N-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VNF to VNN pins. There are four in total.
29	VNN	Negative high voltage supply (-3.0V to -70V).
30	TX1	Transmit pulser outputs for channel 1.
31	VPP	Positive high voltage supply (+3.0V to +70V).
32	VPP	
33	TX2	Transmit pulser outputs for channel 2.
34	VNN	Negative high voltage supply (-3.0V to -70V).
35	VNN	
36	TX3	Transmit pulser outputs for channel 3.
37	VPP	Positive high voltage supply (+3.0V to +70V).
38	VPP	
39	TX4	Transmit pulser outputs for channel 4.
40	VNN	Negative high voltage supply (-3.0V to -70V).
41	VNN	
42	VNF	Linear regulator output gate drive voltage for the N-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VNF to VNN pins. There are four in total.
43	DGND	Digital ground.
44	VPP	Positive high voltage supply (+3.0V to +70V).
45	VPF	Linear regulator output gate drive voltage for the P-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VPF and VPP pin. There are four in total.
46	PGND	Power ground path for RTZ output transistors.
47	PVSS	Negative gate drive supply voltage for RTZ output transistors (-5.0V).
48	PGND	Power ground path for RTZ output transistors.
49	PVDD	Positive gate drive supply voltage for RTZ output transistors (+5.0V).

Pin Description *(cont.)*

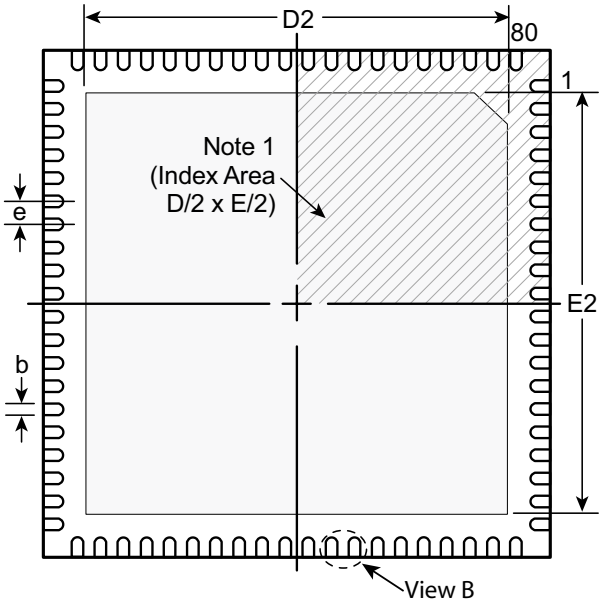
Pin	Name	Description
50	DVDD	Positive digital supply voltage (+5.0V).
51	DGND	Digital ground.
52	PVDD	Positive gate drive supply voltage for RTZ output transistors (+5.0V).
53	PGND	Power ground path for RTZ output transistors.
54	PVSS	Negative gate drive supply voltage for RTZ output transistors (-5.0V).
55	PGND	Power ground path for RTZ output transistors.
56	VPF	Linear regulator output gate drive voltage for the P-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VPF and VPP pin. There are four in total.
57	VPP	Positive high voltage supply (+3.0V to +70V).
58	DGND	Digital ground.
59	VNF	Linear regulator output gate drive voltage for the N-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VNF to VNN pins. There are four in total.
60	VNN	Negative high voltage supply (-3.0V to -70V).
61	VNN	
62	TX5	Transmit pulser outputs for channel 5.
63	VPP	Positive high voltage supply (+3.0V to +70V).
64	VPP	
65	TX6	Transmit pulser outputs for channel 6.
66	VNN	Negative high voltage supply (-3.0V to -70V).
67	VNN	
68	TX7	Transmit pulser outputs for channel 7.
69	VPP	Positive high voltage supply (+3.0V to +70V).
70	VPP	
71	TX8	Transmit pulser outputs for channel 8.
72	VNN	Negative high voltage supply (-3.0V to -70V).
73	VNF	Linear regulator output gate drive voltage for the N-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VNF to VNN pins. There are four in total.
74	NC	No connection.
75	VPF	Linear regulator output gate drive voltage for the P-channel output transistors. A low voltage 1.0µF ceramic capacitor needs to be connected across every VPF and VPP pin. There are four in total.
76	PVSS	Negative gate drive supply voltage for RTZ output transistors (-5.0V).
77	PGND	Power ground path for RTZ output transistors.
78	PGND	
79	PVDD	Positive gate drive supply voltage for RTZ output transistors (+5.0V).
80	VRP	Positive supply for VNF regulator (+5.0V).
VSUB		Exposed center pad. Needs to be externally connected to digital ground, DGND.

80-Lead QFN Package Outline (K6)

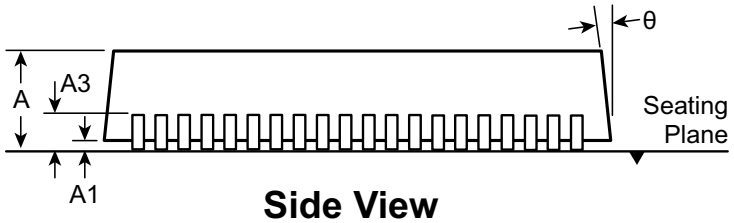
11.00x11.00mm body, 1.00mm height (max), 0.50mm pitch



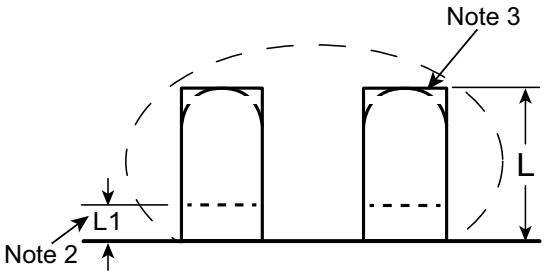
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	10.90	9.50	10.90	9.50	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	11.00	9.65	11.00	9.65		0.40	-	-
	MAX	1.00	0.05		0.30	11.10	9.75	11.10	9.75		0.50	0.15	14°

Drawings are not to scale.
Supertex Doc.#: *DSPD-80QFNK611X11P050, Version A111511*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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