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# ZNBG2000 ZNBG2001

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## FET BIAS CONTROLLER

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### DEVICE DESCRIPTION

The ZNBG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBS, PMR, cellular telephones etc. with a minimum of external components.

With the addition of two capacitors and a resistor the devices provide drain voltage and current control for 2 external grounded source FETs, generating the regulated negative rail required for FET gate biasing whilst operating from a single supply. This negative bias, at -3 volts, can also be used to supply other external circuits.

The ZNBG2000/1 contains two bias stages. A single resistor allows FET drain current to be set to the desired level. The series also offers the choice of drain voltage to be set for the FETs, the ZNBG2000 gives 2.2 volts drain whilst the ZNBG2001 gives 2 volts.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

In order to protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.5V to 0.7V. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The ZNBG2000/1 are available in MSOP10 packages for the minimum in devices size. Device operating temperature is -40 to 80°C to suit a wide range of environmental conditions.

### FEATURES

- Provides bias for GaAs and HEMT FETs
- Drives up to two FETs
- Dynamic FET protection
- Drain current set by external resistor
- Regulated negative rail generator requires only 2 external capacitors
- Choice in drain voltage
- Wide supply voltage range
- MSOP surface mount package

### APPLICATIONS

- Satellite receiver LNBS
- Private mobile radio (PMR)
- Single in single out C Band LNB
- Cellular telephones

# ZNBG2000 ZNBG2001

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.6V to 15V	Output Current	100mA
Supply Current	100mA	Operating Temperature	-40 to 80°C
Drain Current (per FET) (set by R <sub>CAL1</sub> and R <sub>CAL2</sub> )	0 to 15mA	Storage Temperature	-40 to 85°C
		<b>Power Dissipation (T<sub>amb</sub> 25°C)</b>	
		MSOP10	500mW

## ELECTRICAL CHARACTERISTICS TEST CONDITIONS (Unless otherwise

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNITS
			Min	Typ	Max	
V <sub>CC</sub>	Supply Voltage		5		12	V
I <sub>CC</sub>	Supply Current	I <sub>D1</sub> and I <sub>D2</sub> =0 I <sub>D1</sub> and I <sub>D2</sub> =10mA		5 24	10 30	mA mA
V <sub>SUB</sub>	Substrate Voltage (Internally generated)	I <sub>SUB</sub> = 0 I <sub>SUB</sub> = -200μA	-3.5	-2.8	-2 -2	V V
E <sub>ND</sub> E <sub>NG</sub>	Output Noise Drain Voltage Gate Voltage	C <sub>G</sub> =4.7nF, C <sub>D</sub> =10nF C <sub>G</sub> =4.7nF, C <sub>D</sub> =10nF			0.02 0.005	Vpkpk Vpkpk
f <sub>O</sub>	Oscillator Freq.		150	330	800	kHz

## DRAIN CHARACTERISTICS

I <sub>DO</sub>	Output Current Range	Set by R <sub>CAL1</sub>	0		15	mA
I <sub>D</sub>	Current		8	10	12	mA
ΔI <sub>DV</sub> ΔI <sub>DT</sub>	Current Change with V <sub>CC</sub> with T <sub>j</sub>	V <sub>CC</sub> =5 to 12V T <sub>j</sub> =-40 to +80°C		0.5 0.05		%/V %/°C
V <sub>D</sub>	Voltage ZNBG2000 ZNBG2001	I <sub>D1</sub> and I <sub>D2</sub> =10mA	2 1.8	2.2 2	2.4 2.2	V V
ΔV <sub>DV</sub> ΔV <sub>DT</sub>	Voltage Change with V <sub>CC</sub> with T <sub>j</sub>	V <sub>CC</sub> = 5 to 12V T <sub>j</sub> = -40 to +80°C		0.5 50		%/V ppm

## GATE CHARACTERISTICS

I <sub>GO</sub>	Output Current Range		-40		2000	μA
V <sub>OL</sub>	Output Voltage Output Low	I <sub>D1</sub> and I <sub>D2</sub> =12mA I <sub>G1</sub> and I <sub>G2</sub> =0	-3.5		-2	V
		I <sub>D1</sub> and I <sub>D2</sub> =12mA I <sub>G1</sub> and I <sub>G2</sub> = -10μA	-3.5		-2	V
V <sub>OH</sub>	Output High	I <sub>D1</sub> and I <sub>D2</sub> = 8mA I <sub>G1</sub> and I <sub>G2</sub> = 0	0.4		1	V

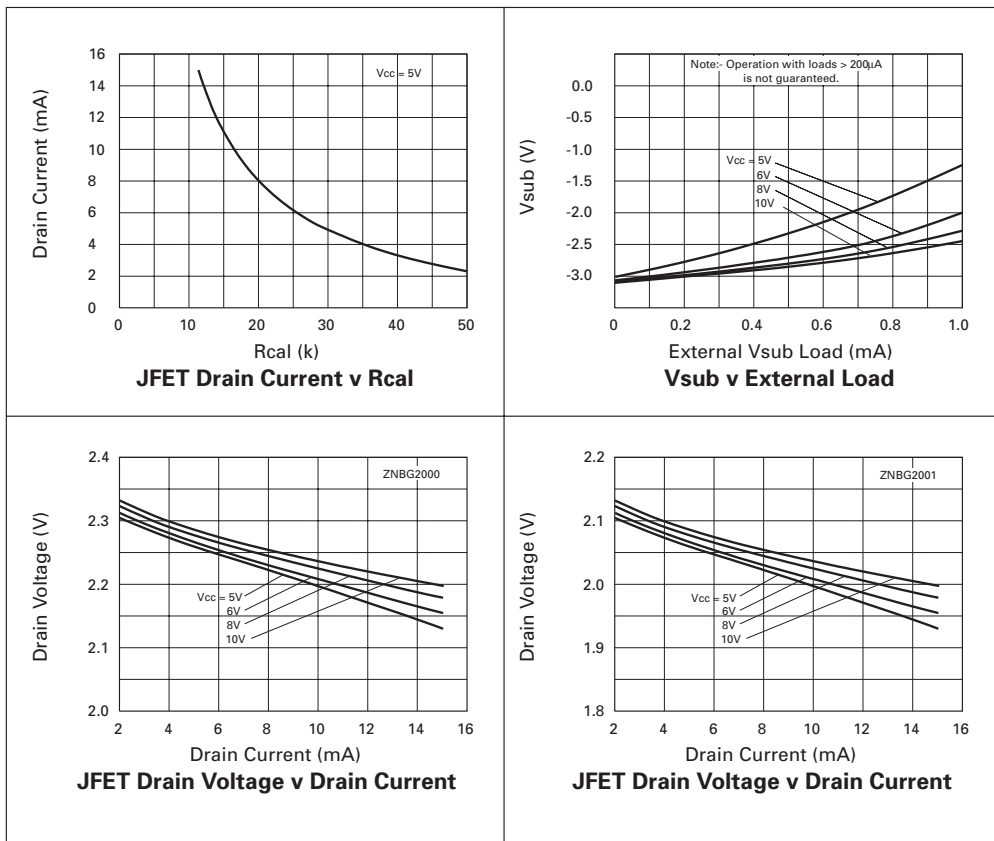
### Notes:

- The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, C<sub>NB</sub> and C<sub>SUB</sub>, of 47nF are required for this purpose.
- The characteristics are measured using an external reference resistors R<sub>CAL1</sub> of value 16kΩ wired from pin R<sub>CAL1</sub> to ground.
- Noise voltage is not measured in production.
- Noise voltage measurement is made with FETs and gate and drain capacitors in place on all outputs. C<sub>G</sub>, 4.7nF, are connected between gate outputs and



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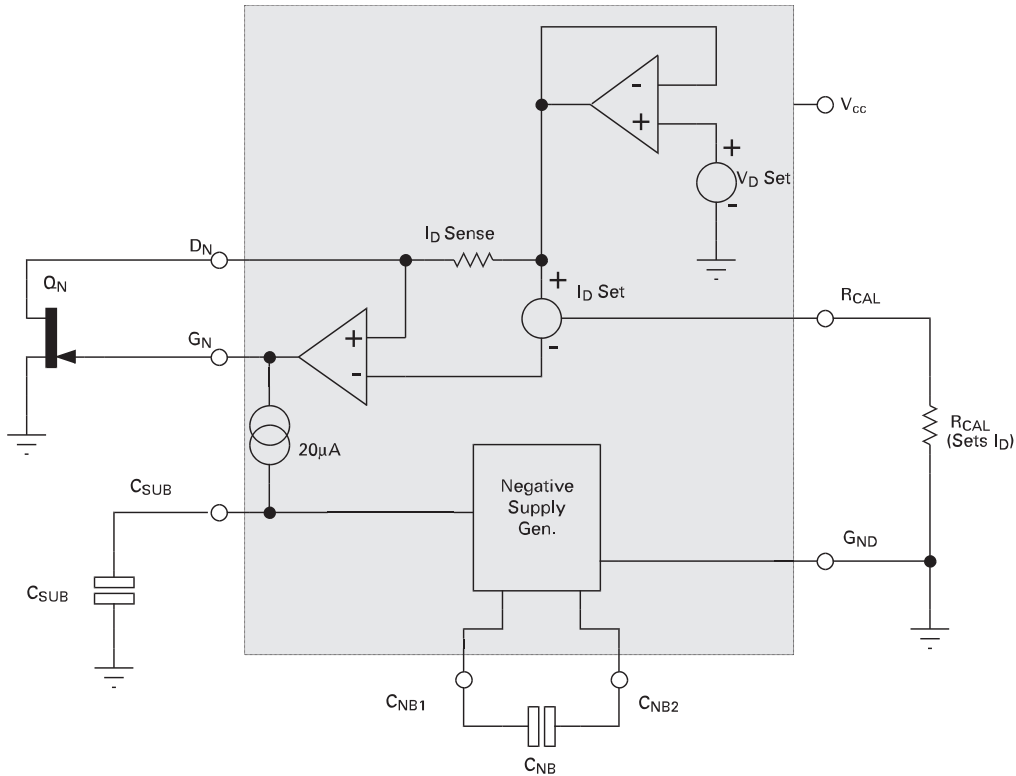
**TYPICAL CHARACTERISTICS**



# ZNBG2000 ZNBG2001

FUNCTIONAL DIAGRAM

FUNCTIONAL



## DESCRIPTION

The ZNBG devices provide all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage.

The diagram above shows a single stage from the ZNBG series. The ZNBG2000/1 contains 2 such stages.

The drain voltage of the external FET  $Q_N$  is set by the ZNBG device to its normal operating voltage. This is determined by the on board  $V_D$  Set reference, for the ZNBG2000 this is nominally 2.2 volts whilst the ZNBG2001 provides nominally 2 volts.

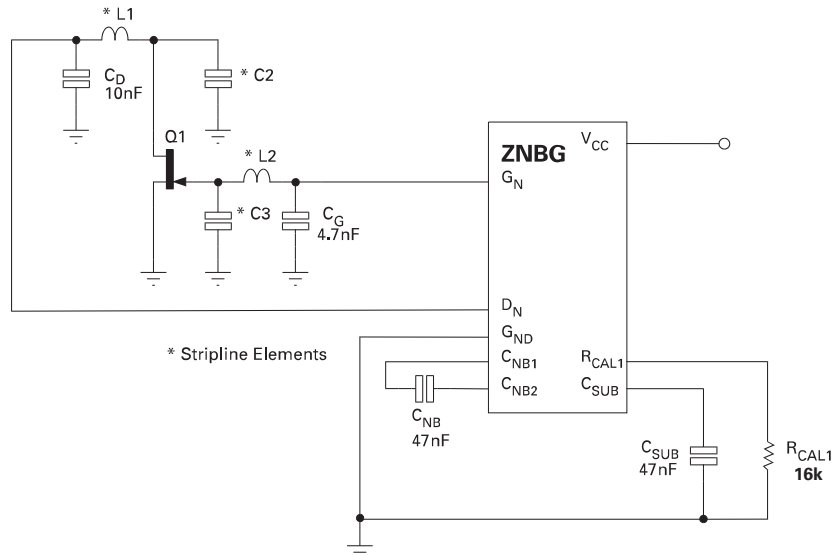
The drain current taken by the FET is monitored by the low value resistor  $I_D$  Sense. The amplifier driving the gate of the FET adjusts the gate voltage of  $Q_N$  so that the drain current taken matches the current called for by an external resistor  $R_{CAL}$ . Both ZNBG devices have the facility to program different drain currents into selected FETs.

Since the FET is a depletion mode transistor, it is usually necessary to drive its gate negative with respect to ground to obtain the required drain current. To provide this capability powered from a single positive supply, the device includes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors,  $C_{NB}$  and  $C_{SUB}$ .

# ZNBG2000 ZNBG2001

## TYPICAL APPLICATION CIRCUIT

## APPLICATIONS



## INFORMATION

The above is a partial application circuit for the ZNBG series showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate and drain capacitors in circuit.

Capacitors  $C_D$  and  $C_G$  ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the ZNBG device. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used.

The capacitors  $C_{NB}$  and  $C_{SUB}$  are an integral part of the ZNBGs negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors  $C_{NB}$  and  $C_{SUB}$  is 47nF. This generator produces a low current supply of approximately -3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the  $C_{SUB}$  pin.

Resistor  $R_{CAL1}$  sets the drain current at which all external FETs are operated. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits. If all FETs associated with a current setting resistor are omitted, the particular  $R_{CAL}$  should still be included. The supply current can be reduced, if required, by using a high value  $R_{CAL}$  resistor (e.g. 470k).

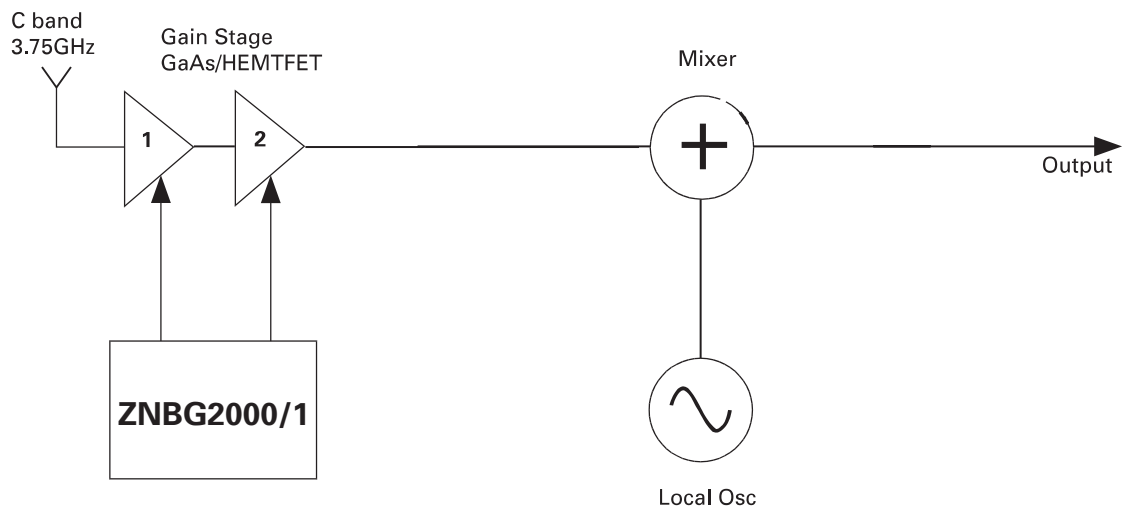
The ZNBG devices have been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3.5V to 0.7V, under any conditions including powerup and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

The following diagram show the ZNBG2000/1 in typical LNB applications.

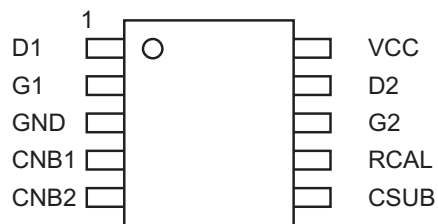
# ZNBG2000 ZNBG2001

## INFORMATION CONT.

## APPLICATIONS



ZNBG2000/01 Pinout For MSOP10  
Package Designator - X

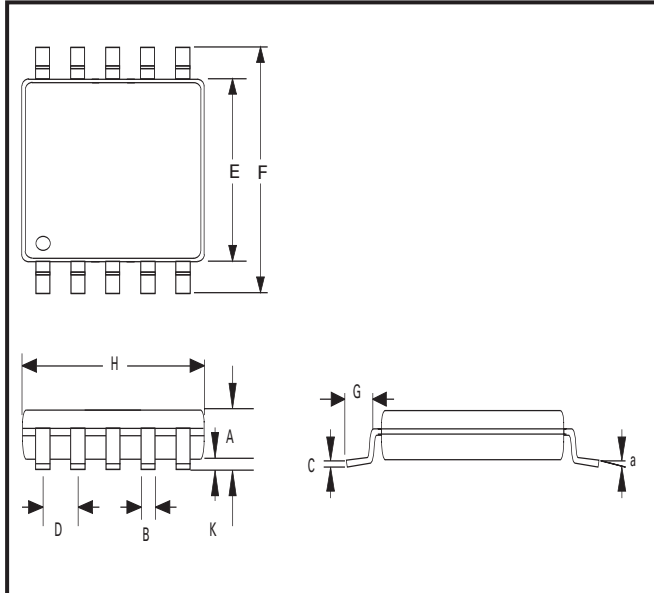


## ORDERING INFORMATION

Part Number	Package	Part Mark	QTY Reel
ZNBG2000X10	MSOP10	ZNBG2000	4000
ZNBG2001X10	MSOP10	ZNBG2001	4000

# ZNBG2000 ZNBG2001

## PACKAGE DIMENSIONS



DIM	Millimetres	tol.	DIM	Millimetres	tol.
A	1.10	MAX.	F	4.9	±0.15
B	0.23	+0.07 -0.08	G	0.55	±0.15
C	0.18	60.05	H	3.00	±0.1
D	0.50	BSC	K	0.10	±0.05
E	3.00	60.1	a	3.0	±3.0°

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