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LM3704,LM3705

LM3704/LM3705 Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output and Manual Reset

Literature Number: SNVS088D

September 2003

National Semiconductor

LM3704/LM3705
Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output and Manual Reset

General Description

The LM3704/LM3705 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3704/LM3705 series are available in MSOP-10 and 9-bump micro SMD packages.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

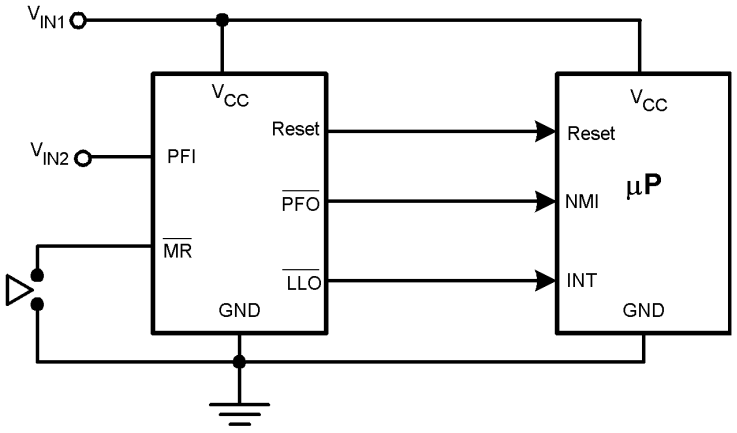
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ (LM3704) or RESET (LM3705) outputs
- Precision supply voltage monitor
- Factory programmable Reset Timeout Delay
- Separate Power Fail comparator
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

Typical Application



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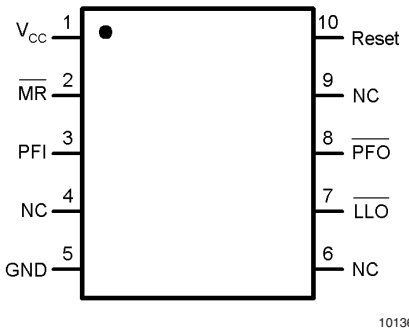
Connection Diagram

MSOP-10



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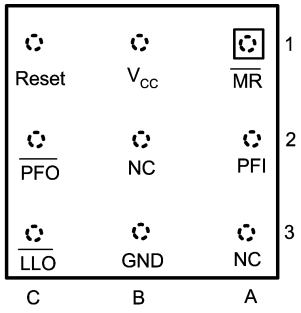
Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09



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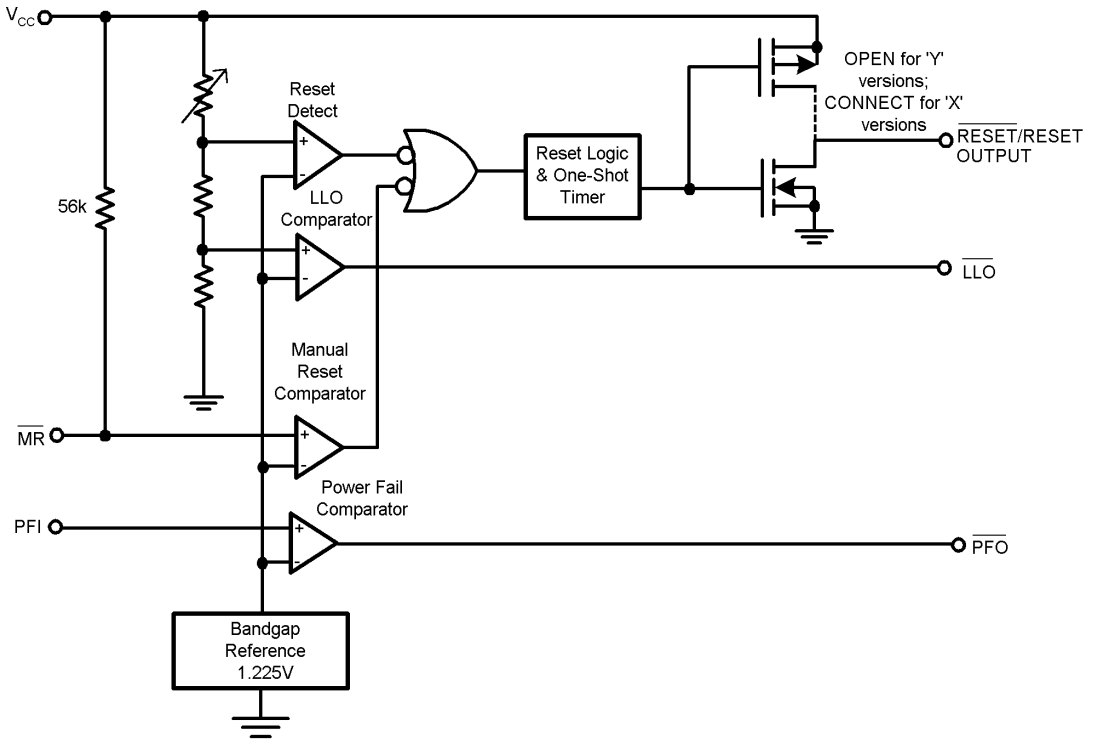
Pin Description

Pin No.		Name	Function
micro SMD	MSOP		
A1	2	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
B1	1	V_{CC}	Power Supply input.
C1	10	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3704 only).
		RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3705 only).
C2	8	$\overline{PFO}$	Power-Fail Logic Output. When PFI is below V_{PFT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
C3	7	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
B3	5	GND	Ground reference for all signals.
A3	4, 6	NC	No Connect.
A2	3	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
B2	9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram



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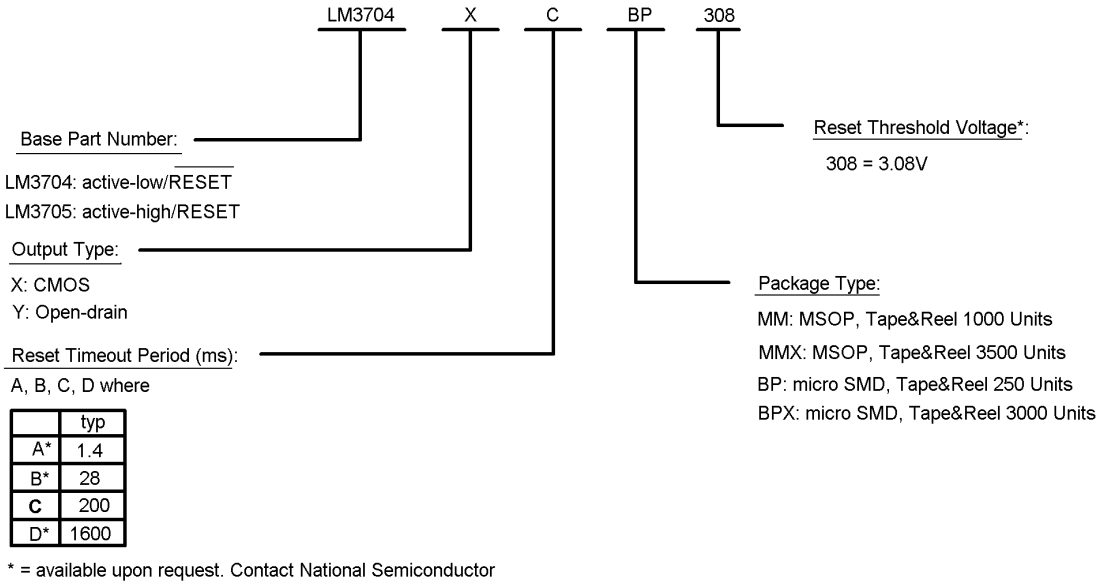
Ordering Information



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*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3704/LM3705

Part Number	Output	Reset Timeout Period	Package		Package Marking
			MSOP	micro SMD	
LM3704XBBP-232	totem-pole	28ms		x	%%I13
LM3704XBBPX-232	totem-pole	28ms		x	%%I13
LM3704XBBP-463	totem-pole	28ms		x	%%I27
LM3704XBBPX-463	totem-pole	28ms		x	%%I27
LM3704XBMM-232	totem-pole	28ms	x		R66B
LM3704XBMMX-232	totem-pole	28ms	x		R66B
LM3704XBMM-463	totem-pole	28ms	x		R27B
LM3704XBMMX-463	totem-pole	28ms	x		R27B
LM3704XCBP-308	totem-pole	200ms		x	%%I4
LM3704XCBPX-308	totem-pole	200ms		x	%%I4
LM3704XCMM-263	totem-pole	200ms	x		R79B
LM3704XCMMX-263	totem-pole	200ms	x		R79B
LM3704XCMM-308	totem-pole	200ms	x		R35B
LM3704XCMMX-308	totem-pole	200ms	x		R35B
LM3704XDBP-232	totem-pole	1600ms		x	%%I15
LM3704XDBPX-232	totem-pole	1600ms		x	%%I15
LM3704XDBP-463	totem-pole	1600ms		x	%%I17
LM3704XDBPX-463	totem-pole	1600ms		x	%%I17
LM3704XDMM-220	totem-pole	1600ms	x		R65B
LM3704XDMMX-220	totem-pole	1600ms	x		R65B
LM3704XDMM-232	totem-pole	1600ms	x		R67B
LM3704XDMMx-232	totem-pole	1600ms	x		R67B
LM3704XDMM-463	totem-pole	1600ms	x		R68B
LM3704XDMMX-463	totem-pole	1600ms	x		R68B
LM3704YAMM-308	open-drain	1.4ms	x		R78B
LM3704YAMMX-308	open-drain	1.4ms	x		R78B

Ordering Information (Continued)

LM3704/LM3705 (Continued)

Part Number	Output	Reset Timeout Period	Package		Package Marking
			MSOP	micro SMD	
LM3704YBMM-360	open-drain	28ms	x		R49B
LM3704YBMMX-360	open-drain	28ms	x		R49B
LM3704YCMM-232	open-drain	200ms	x		R76B
LM3704YCMMX-232	open-drain	200ms	x		R76B
LM3704YCMM-308	open-drain	200ms	x		R48B
LM3704YCMMX-308	open-drain	200ms	x		R48B
LM3705XBBP-232	totem-pole	28ms		x	%%I14
LM3705XBBPX-232	totem-pole	28ms		x	%%I14
LM3705XBBP-463	totem-pole	28ms		x	%%I33
LM3705XBBPX-463	totem-pole	28ms		x	%%I33
LM3705XBMM-232	totem-pole	28ms	x		R69B
LM3705XBMMX-232	totem-pole	28ms	x		R69B
LM3705XBMM-463	totem-pole	28ms		x	R44B
LM3705XBMMX-463	totem-pole	28ms		x	R44B
LM3705XCBP-463	totem-pole	200ms		x	%%I5
LM3705XCBPX-463	totem-pole	200ms		x	%%I5
LM3705XCMM-308	totem-pole	200ms	x		R36B
LM3705XCMMX-308	totem-pole	200ms	x		R36B
LM3705XDBP-232	totem-pole	1600ms		x	%%I16
LM3705XDBPX-232	totem-pole	1600ms		x	%%I16
LM3705XDBP-463	totem-pole	1600ms		x	%%I18
LM3705XDBPX-463	totem-pole	1600ms		x	%%I18
LM3705XDMM-232	totem-pole	1600ms	x		R70B
LM3705XDMMX-232	totem-pole	1600ms	x		R70B
LM3705XDMM-463	totem-pole	1600ms	x		R71B
LM3705XDMMX-463	totem-pole	1600ms	x		R71B

%% is the datecode and will vary with time.

Table of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Manual Reset	Power Fail Comparator	Low Line Output
LM3704	x		X, Y*	Customized	x	x	x
LM3705		x	X	Customized	x	x	x

* = available upon request. Contact National

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to 6.0V
All Other Inputs	−0.3V to V_{CC} + 0.3V
ESD Ratings (Note 2)	
Human Body Model	1.5kV
Machine Model	150V
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	−40˚C ≤ T_J ≤ 85˚C

LM3704/LM3705 Series Electrical Characteristics

Limits in the standard typeface are for T_J = 25˚C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range: V_{CC}	LM3704	**1.0**		**5.5**	V
		LM3705	**1.2**		**5.5**	
I_{CC}	V_{CC} Supply Current	All inputs = V_{CC}; all outputs floating		28	**50**	µA
RESET THRESHOLD						
V_{RST}	Reset Threshold	V_{CC} falling	−0.5 **−2**	V_{RST}	+0.5 **+2**	%
		V_{CC} falling: T_A = 0˚C to 70˚C	**−1.5**		**+1.5**	
V_{RSTH}	Reset Threshold Hysteresis			0.0032•V_{RST}		mV
t_{RP}	Reset Timeout Period	Reset Timeout Period = A	**1**	1.4	**2**	ms
		Reset Timeout Period = B	**20**	28	**40**	
		Reset Timeout Period = C	**140**	200	**280**	
		Reset Timeout Period = D	**1120**	1600	**2240**	
t_{RD}	V_{CC} to Reset Delay	V_{CC} falling at 1mV/µs		20		µs
RESET (LM3705)						
V_{OL}	RESET	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	RESET	V_{CC} > 1.2V, I_{SOURCE} = 50µA	**0.8 V_{CC}**			V
		V_{CC} > 1.8V, I_{SOURCE} = 150µA	**0.8 V_{CC}**			
		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
I_{LKG}	Output Leakage Current	V_{RESET} = 5.5V			**1.0**	µA
$\overline{\text{RESET}}$ (LM3704)						
V_{OL}	$\overline{\text{RESET}}$	V_{CC} > 1.0V, I_{SINK} = 50µA			**0.3**	V
		V_{CC} > 1.2V, I_{SINK} = 100µA			**0.3**	
		V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	$\overline{\text{RESET}}$	V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			

LM3704/LM3705 Series Electrical Characteristics (Continued)

Limits in the standard typeface are for T_J = 25˚C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PFI/$\overline{MR}$						
V_{PFT}	PFI Input Threshold		**1.200**	1.225	**1.250**	V
V_{MRT}	$\overline{MR}$ Input Threshold	$\overline{MR}$, Low			**0.8**	V
		$\overline{MR}$, High	**2.0**			
V_{PFTH}/ V_{MRTH}	PFI/$\overline{MR}$ Threshold Hysteresis	PFI/$\overline{MR}$ falling: V_{CC} = $V_{RST\ MAX}$ to 5.5V		0.0032•V_{RST}		mV
I_{PFI}	Input Current (PFI only)		**–75**		**75**	nA
R_{MR}	$\overline{MR}$ Pull-up Resistance		**35**	56	**75**	kΩ
t_{MD}	$\overline{MR}$ to Reset Delay			12		µS
t_{MR}	$\overline{MR}$ Pulse Width		**25**			µS
$\overline{PFO}$, $\overline{LLO}$						
V_{OL}	$\overline{PFO}$, $\overline{LLO}$ Output Voltage	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} – 1.5V**			
$\overline{LLO}$ OUTPUT						
V_{LLOT}	$\overline{LLO}$ Output Threshold ($V_{\overline{LLO}}$ – V_{RST}, V_{CC} falling)		**1.01•V_{RST}**	1.02•V_{RST}	**1.03•V_{RST}**	V
V_{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V_{RST}		mV
t_{CD}	Low-Line Comparator Delay	V_{CC} falling at 1mV/µs		20		µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

Note 2: The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

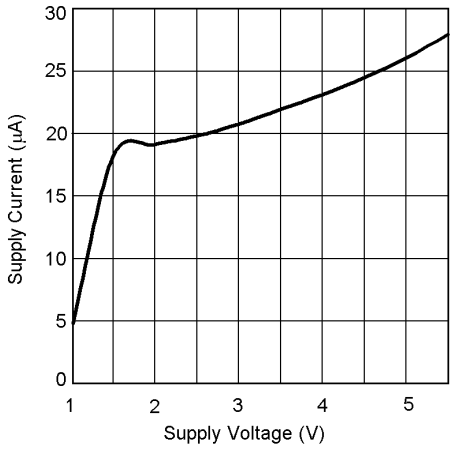
Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperture is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the MSOP-10 package is 195˚C/W in a typical PC board mounting and the micro SMD package is 220˚C/W.

Typical Performance Characteristics

Supply Current vs Supply Voltage



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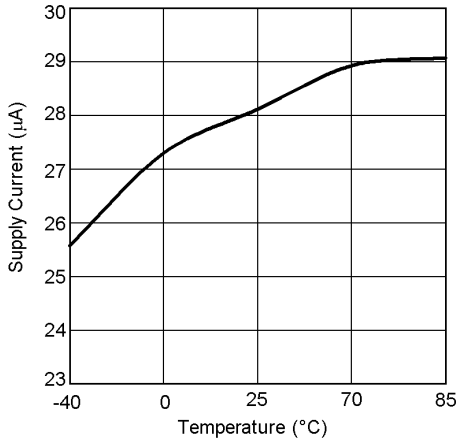
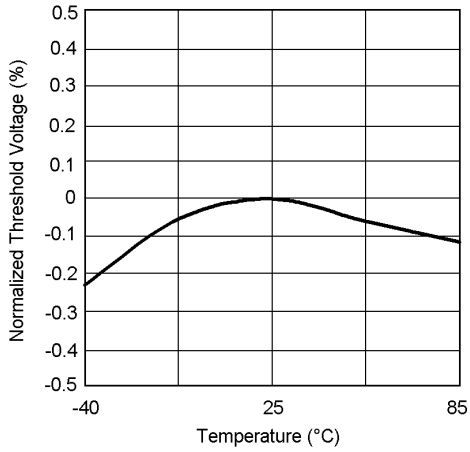
3.3V Supply Current vs Temperature



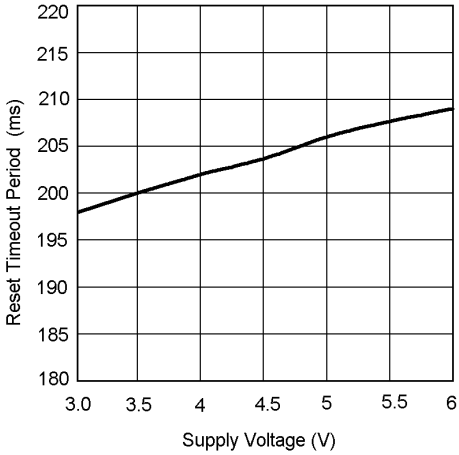
10136911

Normalized Reset Threshold Voltage vs Temperature



10136912

Reset Timeout Period vs V_{CC}



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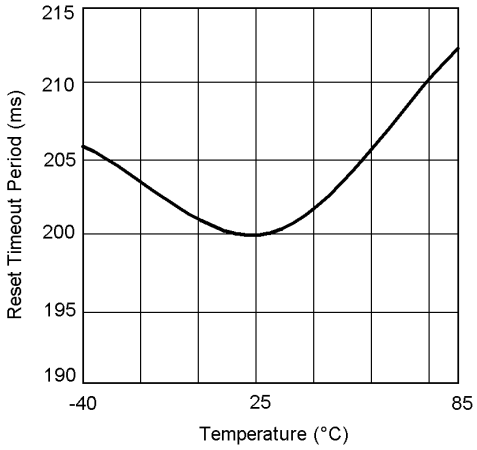
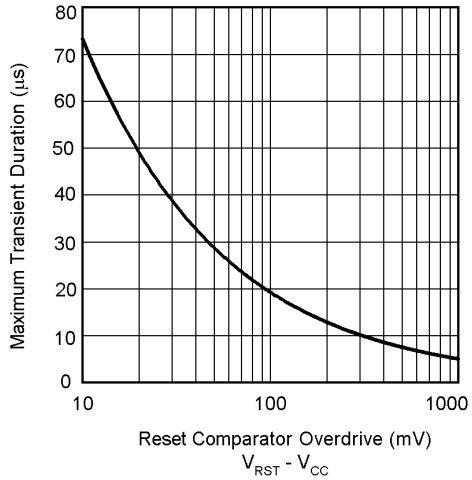
Reset Timeout Period vs Temperature



10136910

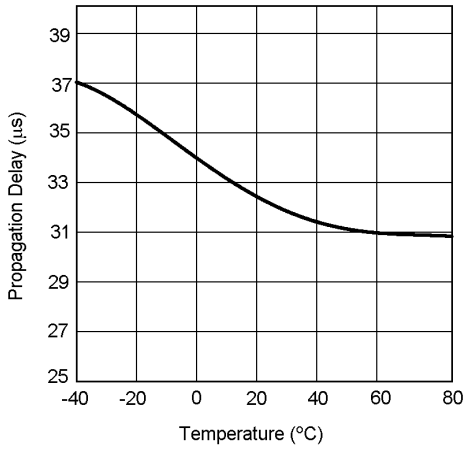
Max. Transient Duration vs Reset Comparator Overdrive (V_{CC} = 3.3V)



10136916

Typical Performance Characteristics (Continued)

Low-Line Comparator Propagation Delay vs Temperature



10136914

Circuit Information

RESET OUTPUT

The Reset input of a µP initializes the device into a known state. The LM3704/LM3705 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is guaranteed valid for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3704 offers an active-low $\overline{\text{RESET}}$; The LM3705 offers an active-high RESET.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset also. See the *Manual Reset Input* section.

RESET THRESHOLD

The LM3704/LM3705 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact National Semiconductor for details.

MANUAL RESET INPUT ($\overline{\text{MR}}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 kΩ pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 µs, reset is asserted after a typical delay of 12 µs. Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT}. Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

POWER-FAIL COMPARATOR (PFI/$\overline{\text{PFO}}$)

The PFI is compared to a 1.225V internal reference, V_{PFT}. If PFI is less than V_{PFT}, the Power Fail Output $\overline{\text{PFO}}$ drops low. The power-fail comparator signals a falling power supply, and is driven typically by an external voltage divider that senses either the unregulated supply or another system supply voltage. The voltage divider generally is chosen so the voltage at PFI drops below V_{PFT} several milliseconds before the main supply voltage drops below the reset threshold, providing advanced warning of a brownout.

The voltage threshold is set by R_1 and R_2 and is calculated as follows:

$$V_{PFT} = \left(\frac{R1 + R2}{R2}\right) \times 1.225V$$

Note this comparator is completely separate from the rest of the circuitry, and may be employed for other functions as needed.

LOW-LINE OUTPUT ($\overline{\text{LLO}}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a µP when V_{CC} begins falling. $\overline{\text{LLO}}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 • V_{RST}) with hysteresis of 0.0032 • V_{RST}.

SPECIAL PRECAUTIONS FOR THE MICRO SMD PACKAGE

As with most integrated circuits, the LM3704 and LM3705 are sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the micro SMD package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

MICRO SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note AN-1112. Referring to the section ***Surface Mount Technology (SMT) Assembly Considerations***, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

Timing Diagrams

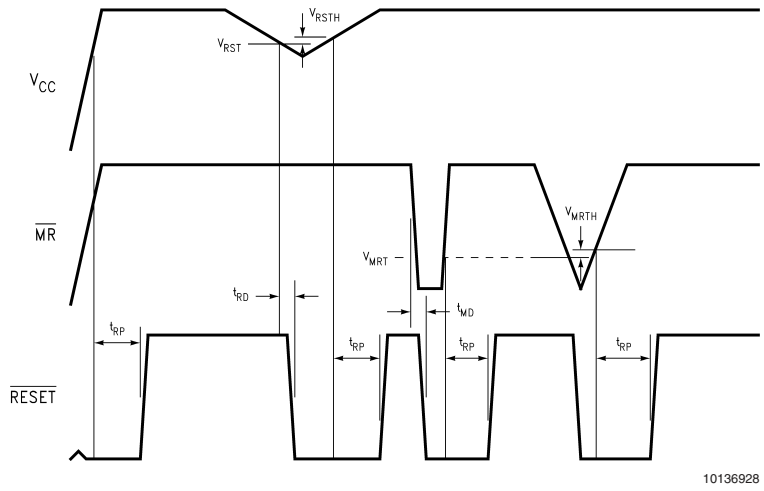


FIGURE 1. LM3704 Reset Time with $\overline{MR}$

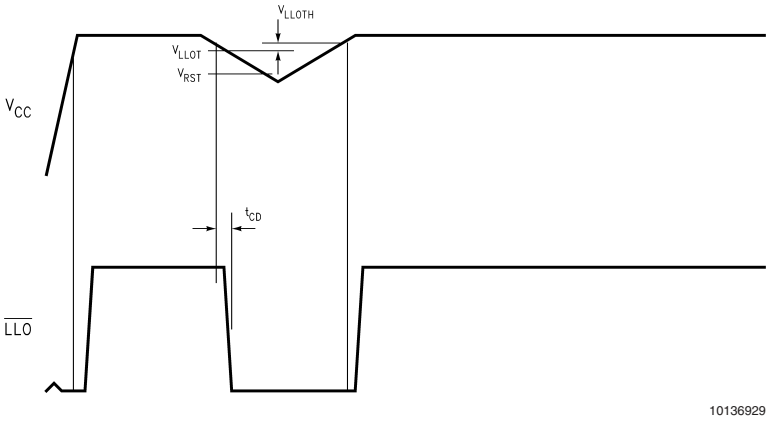


FIGURE 2. $\overline{LLO}$ Output

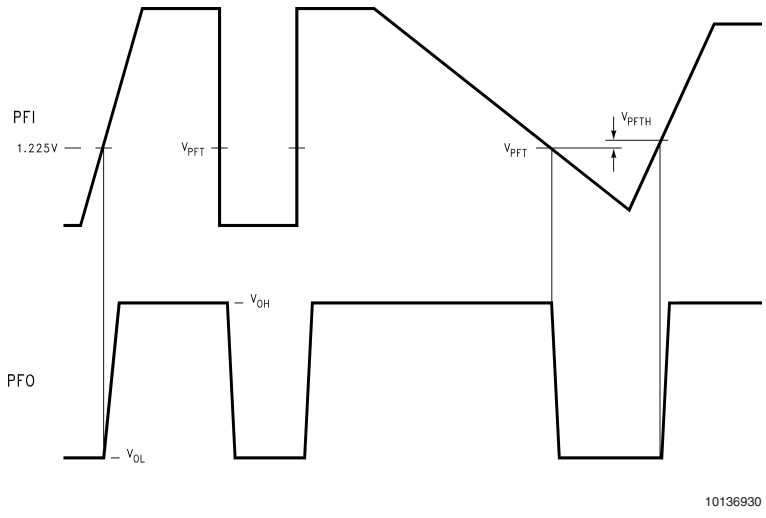


FIGURE 3. PFI Comparator Timing Diagram

Typical Application Circuits

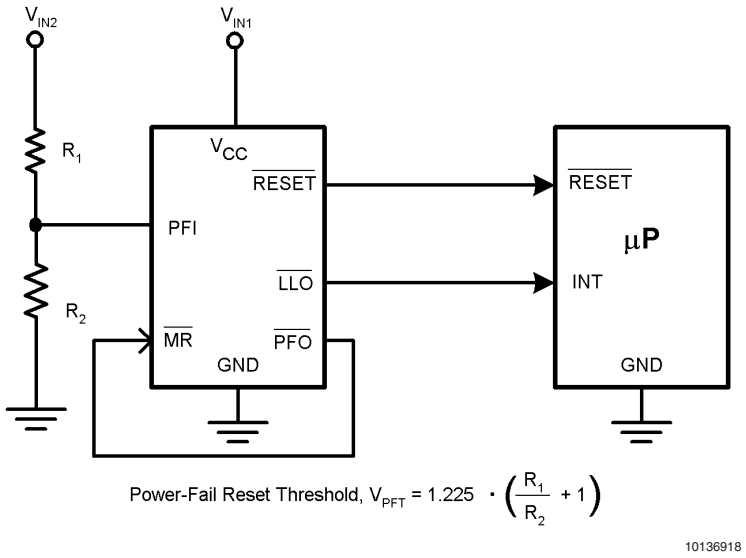


FIGURE 4. Monitoring Two Critical Supplies

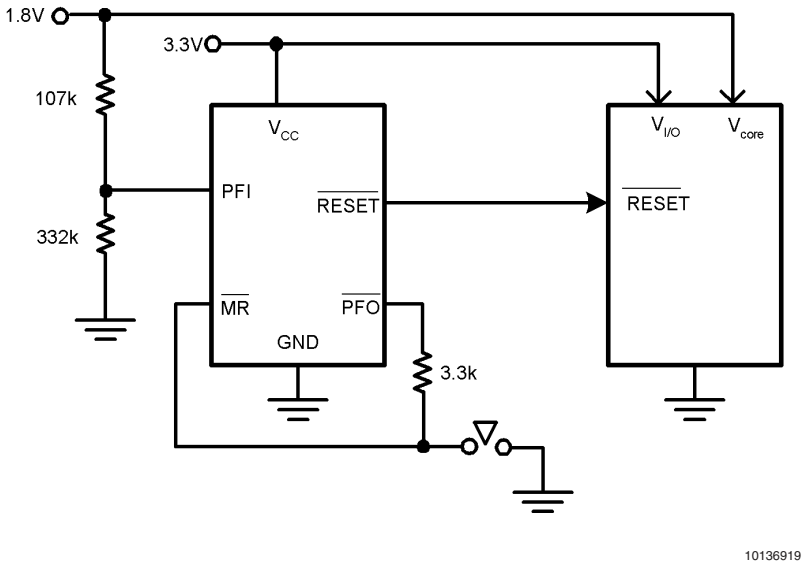


FIGURE 5. Monitoring Two Supplies plus Manual Reset

Typical Application Circuits (Continued)

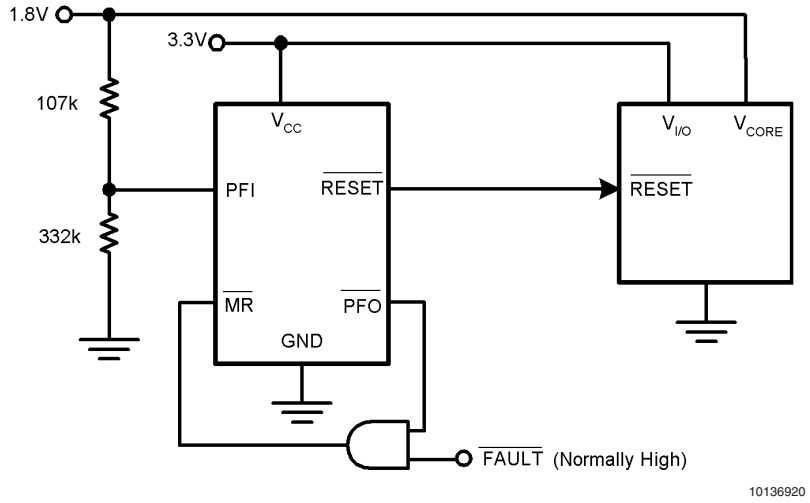
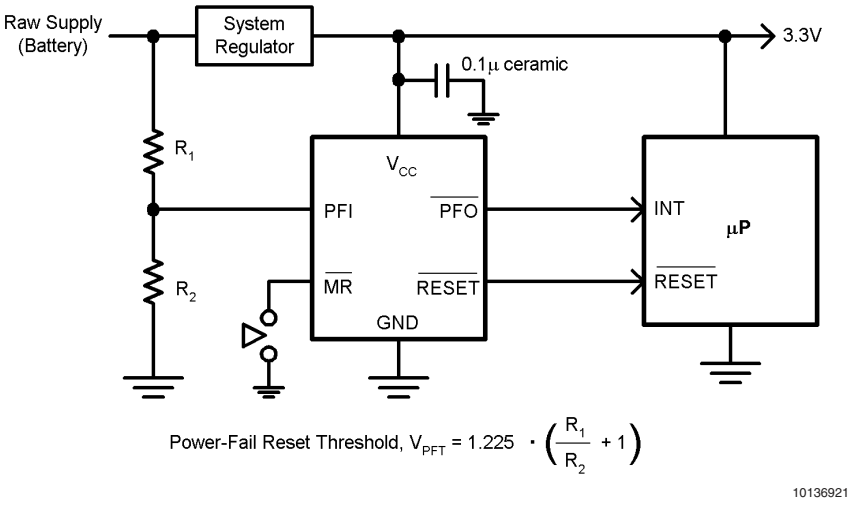


FIGURE 6. Monitoring Dual Supplies plus External Fault Input



Note: $\overline{MR}$ input with its 1.225V nominal threshold, may monitor an additional supply voltage. An internal 56 kΩ pull-up resistor is included on this input.

FIGURE 7. Microprocessor Supervisor with Early Warning Detector

Typical Application Circuits (Continued)

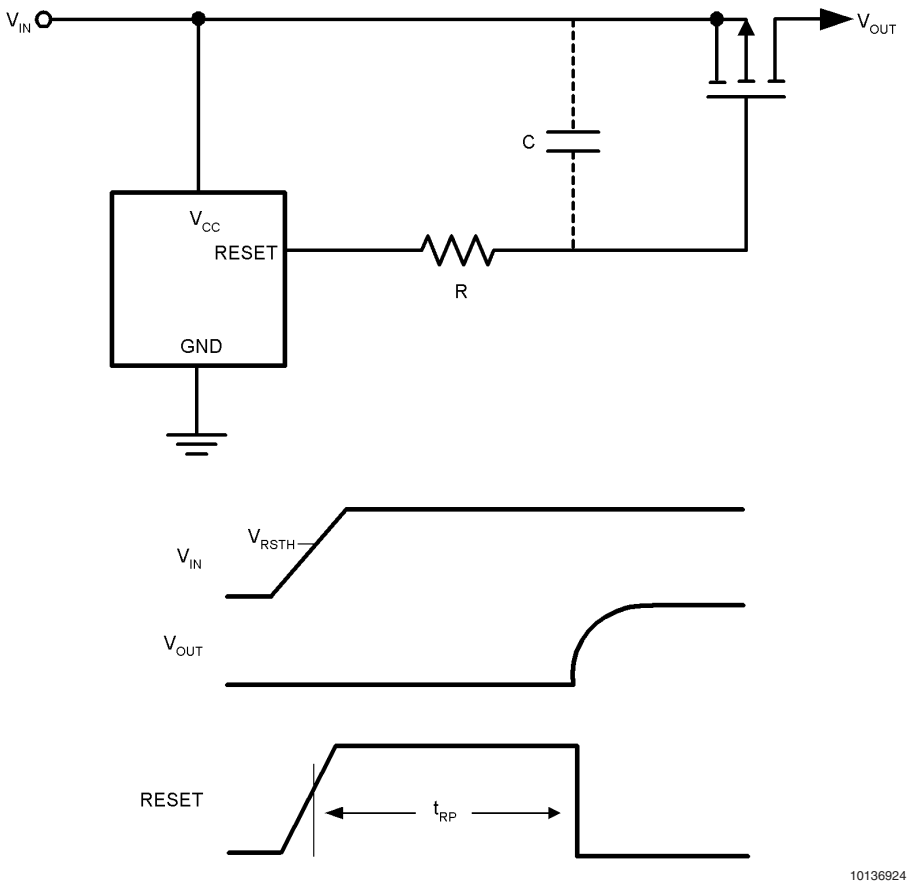


FIGURE 8. LM3705 Power-On Delay

Typical Application Circuits (Continued)

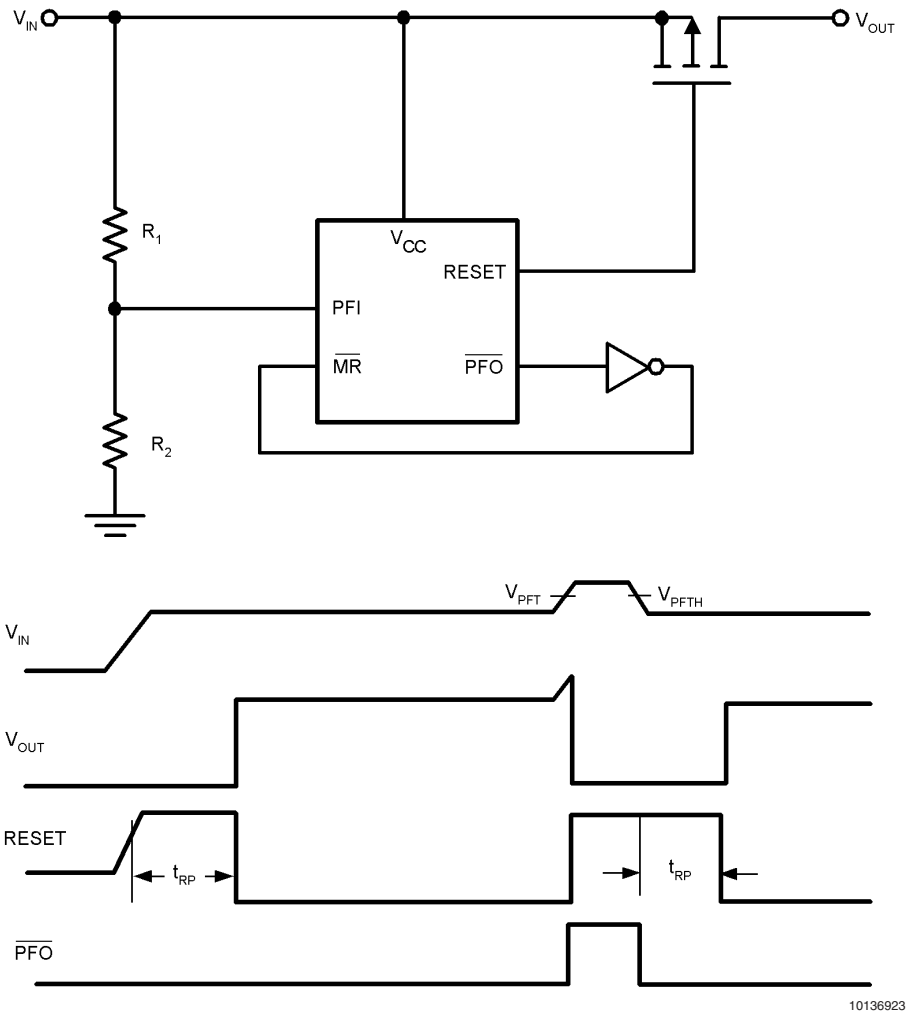


FIGURE 9. LM3705 Power-On Delay with Overvoltage Protection

Typical Application Circuits (Continued)

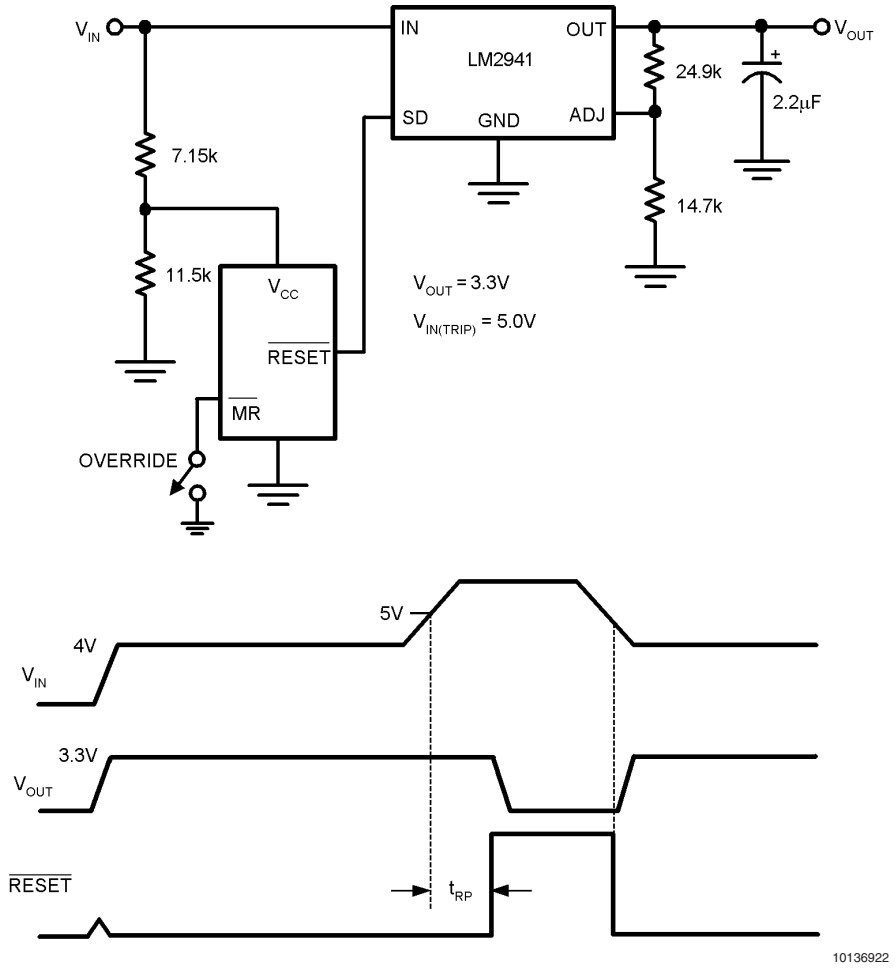


FIGURE 10. Regulator/Switch with Long-Term Overvoltage Lockout Prevents Overdissipation in Linear Regulator

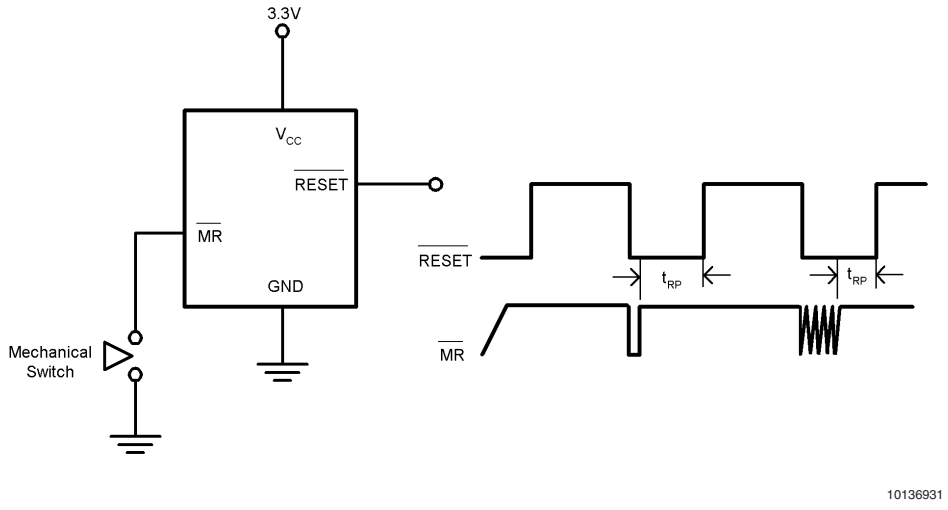
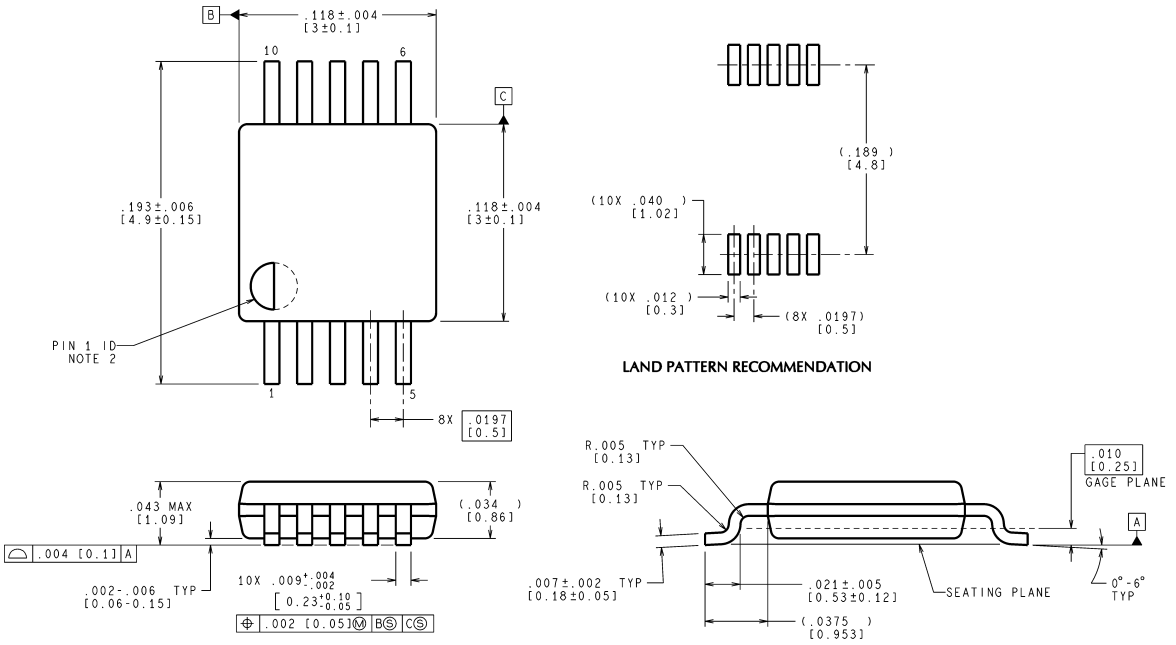


FIGURE 11. Switch Debouncer

Physical Dimensions inches (millimeters)

unless otherwise noted

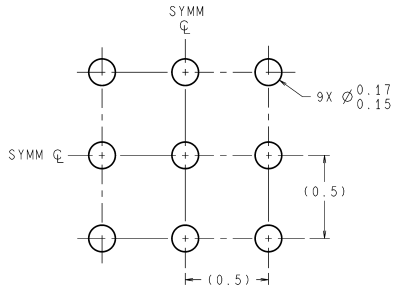


CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MUB10A (Rev B)

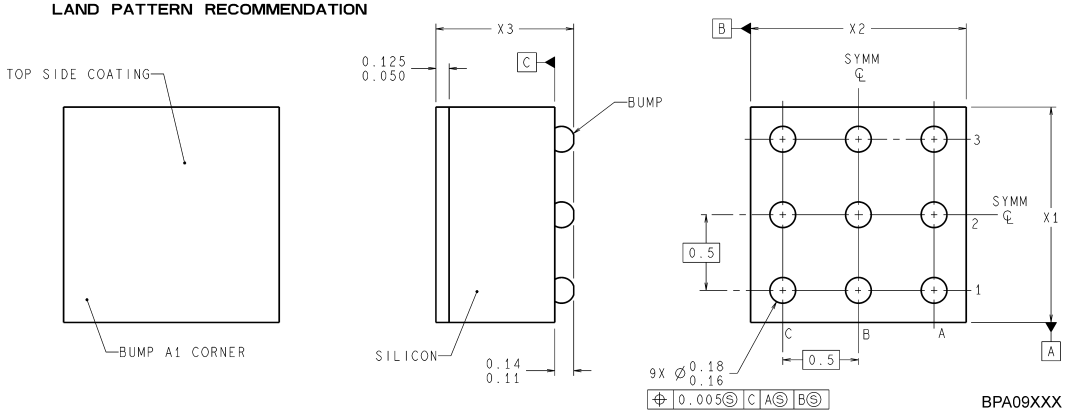
10 Lead MSOP Package
NS Package Number MUB10A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION



BPA09XXX (Rev D)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.
6. NO JEDEC REGISTRATION AS OF AUG.1999.

9 bump micro SMD Package
NS Package Number BPA09FFB
The dimensions of X1, X2 and X3 are given below
X1 = 1.412mm
X2 = 1.412mm
X3 = 0.850mm

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