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TPS3123-xx
TPS3124-xx, TPS3125-xx
TPS3126-xx, TPS3128-xx

SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

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# ULTRA-LOW VOLTAGE PROCESSOR SUPERVISORY CIRCUITS

## FEATURES

- **Minimum Supply Voltage of 0.75 V**
- **Supply Voltage Supervision Range:**
  - **– 1.2 V, 1.5 V, 1.8 V (TPS312x)**
  - **– 3 V (TPS3125 Devices Only)**
  - **– Other Versions on Request**
- **Power-On Reset Generator With Fixed Delay Time of 180 ms**
- **Manual Reset Input (TPS3123/5/6/8)**
- **Watchdog Timer Retriggers the $\overline{\text{RESET}}$ Output at $V_{DD} \geq V_{IT}$**
- **Supply Current of 14 µA (Typ)**
- **Small SOT23-5 Package**
- **Temperature Range of -40°C to 85°C**
- **Reset Output Available in Push-Pull (Active Low and High) and Open-Drain (Active-Low)**

## APPLICATIONS

- **Applications Using Low Voltage DSPs, Microcontrollers, or Microprocessors**
- **Portable/Battery-Powered Equipment**
- **Wireless Communication Systems**
- **Programmable Controls**
- **Industrial Equipment**
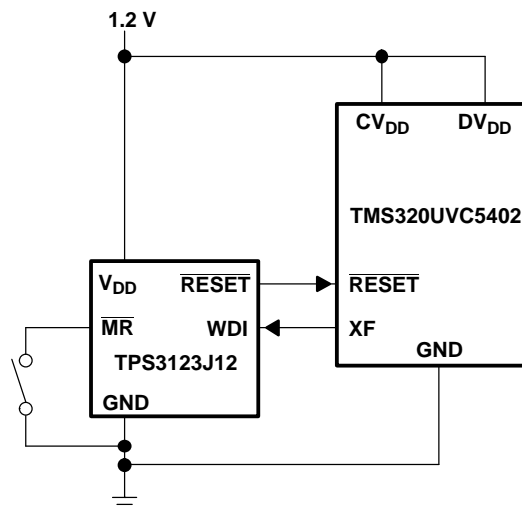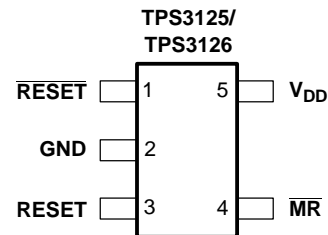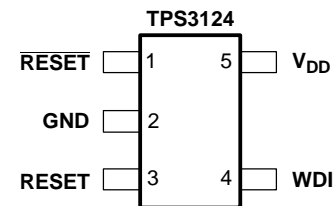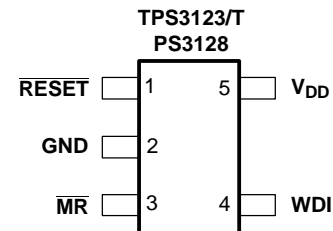- **Notebook/Desktop Computers**
- **Intelligent Instruments**

**DBV PACKAGE**
**(TOP VIEW)**

**TPS3123/T**
**PS3128**

| | | | |
|---|---|---|---|
| $\overline{\text{RESET}}$ | 1 | 5 | $V_{DD}$ |
| GND | 2 | | |
| $\overline{\text{MR}}$ | 3 | 4 | WDI |

**TPS3124**

| | | | |
|---|---|---|---|
| $\overline{\text{RESET}}$ | 1 | 5 | $V_{DD}$ |
| GND | 2 | | |
| RESET | 3 | 4 | WDI |

**TPS3125/**
**TPS3126**

| | | | |
|---|---|---|---|
| $\overline{\text{RESET}}$ | 1 | 5 | $V_{DD}$ |
| GND | 2 | | |
| RESET | 3 | 4 | $\overline{\text{MR}}$ |

Figure 1. Typical Low-Voltage DSP Application

**TPS3123-xx**
**TPS3124-xx, TPS3125-xx**
**TPS3126-xx, TPS3128-xx**

SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

## DESCRIPTION

The TPS312x family of ultralow voltage processor supervisory circuits provides circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage ($V_{DD}$) becomes higher than 0.75 V. Thereafter, the supply voltage supervisor monitors $V_{DD}$ and keeps $\overline{\text{RESET}}$ output active as long as $V_{DD}$ remains below the threshold voltage ($V_{IT}$). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_d$ = 180 ms, starts after $V_{DD}$ has risen above the threshold voltage ($V_{IT}$).

When the supply voltage drops below the threshold voltage ($V_{IT}$), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage ($V_{IT}$) set by a high precision internal voltage divider.

The TPS3123/5/6/8 devices incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. The TPS3124 devices do not have the input $\overline{\text{MR}}$, but include a high-level output RESET same as the TPS3125 and TPS3126 devices. In addition, the TPS3123/4/8 have a watchdog timer that needs to be triggered periodically by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval $t_{tout}$= 0.8 s, $\overline{\text{RESET}}$ output becomes active for the time period ($t_d$). This event also reinitializes the watchdog timer.

The circuits are available in a 5-pin SOT23-5 package. The TPS312x devices are characterized for operation over a temperature range of -40°C to 85°C.

### PACKAGE INFORMATION STANDARD VERSIONS[1]

| $T_A$ | DEVICE NAME | | THRESHOLD VOLTAGE | MARKING |
|---|---|---|---|---|
| -40°C to 85°C | TPS3123J12DBVR[2] | TPS3123J12DBVT[3] | 1.08 V | PBNI |
| | TPS3123G15DBVR[2] | TPS3123G15DBVT[3] | 1.40 V | PBOI |
| | TPS3123J18DBVR[2] | TPS3123J18DBVT[3] | 1.62 V | PBPI |
| | TPS3124J12DBVR[2] | TPS3124J12DBVT[3] | 1.08 V | PBQI |
| | TPS3124G15DBVR[2] | TPS3124G15DBVT[3] | 1.40 V | PBRI |
| | TPS3124J18DBVR[2] | TPS3124J18DBVT[3] | 1.62 V | PBSI |
| | TPS3125J12DBVR[2] | TPS3125J12DBVT[3] | 1.08 V | PBTI |
| | TPS3125G15DBVR[2] | TPS3125G15DBVT[3] | 1.40 V | PBUI |
| | TPS3125J18DBVR[2] | TPS3125J18DBVT[3] | 1.62 V | PBVI |
| | TPS3125L30DBVR[2] | TPS3125L30DBVT[3] | 2.64 V | PBXI |
| | TPS3126E12DBVR[2] | TPS3126E12DBVT[3] | 1.14 V | PFOI |
| | TPS3126E15DBVR[2] | TPS3126E15DBVT[3] | 1.43 V | PFPI |
| | TPS3126E18DBVR[2] | TPS3126E18DBVT[3] | 1.71 V | PFQI |
| | TPS3128E12DBVR[2] | TPS3128E12DBVT[3] | 1.14 V | PFRI |
| | TPS3128E15DBVR[2] | TPS3128E15DBVT[3] | 1.43 V | PFSI |
| | TPS3128E18DBVR[2] | TPS3128E18DBVT[3] | 1.71 V | PFTI |

(1)  Other versions available. Contact Texas Instruments for deetails, minimum order quantities apply.
(2)  The DBVR passive indicates tape and reel of 3000 parts.
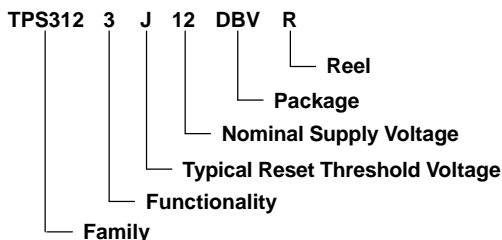(3)  The DBVT passive indicates tape and reel of 250 parts.

**TPS3123-xx**
**TPS3124-xx, TPS3125-xx**
**TPS3126-xx, TPS3128-xx**

SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

TPS312  3  J  12  DBV  R

- Reel
- Package
- Nominal Supply Voltage
- Typical Reset Threshold Voltage
- Functionality
- Family

## Table 1. Ordering Information Application Specific Versions [1]

| DEVICE NAME | NOMINAL SUPPLY VOLTAGE, $V_{NOM}$ | DEVICE NAME | TYPICAL RESET THRESHOLD VOLTAGE-$V_{IT-}$ |
|---|---|---|---|
| TPS312xx12DBV | 1.2 V | TPS312xAxxDBV | $V_{NOM}$-1% |
| TPS312xx15DBV | 1.5 V | TPS312xBxxDBV | $V_{NOM}$-2% |
| TPS312xx18DBV | 1.8 V | TPS312xCxxDBV | $V_{NOM}$-3% |
| TPS312xx30DBV | 3.0 V | TPS312xDxxDBV | $V_{NOM}$-4% |
| | | TPS312xExxDBV | $V_{NOM}$-5% |
| | | TPS312xFxxDBV | $V_{NOM}$-6% |
| | | TPS312xGxxDBV | $V_{NOM}$-7% |
| | | TPS312xHxxDBV | $V_{NOM}$-8% |
| | | TPS312xIxxDBV | $V_{NOM}$-9% |
| | | TPS312xJxxDBV | $V_{NOM}$-10% |
| | | TPS312xKxxDBV | $V_{NOM}$-11% |
| | | TPS312xLxxDBV | $V_{NOM}$-12% |
| | | TPS312xMxxDBV | $V_{NOM}$-13% |
| | | TPS312xNxxDBV | $V_{NOM}$-14% |
| | | TPS312xOxxDBV | $V_{NOM}$-15% |

(1)  For the application specific versions contact Texas Instruments for availability, lead time, and minimum order quantities.
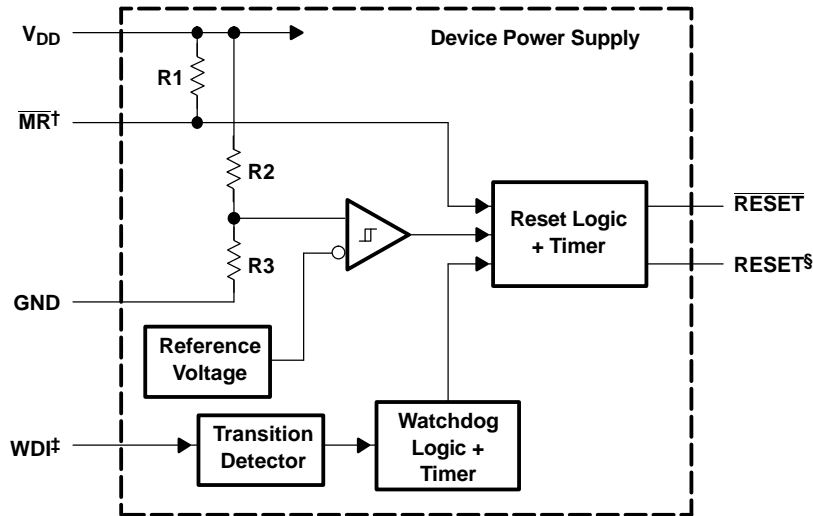
## Table 2. Function Tables

| \overline{MR} | VDD > $V_{IT}$ | \overline{RESET} | VDD > $V_{IT}$ | \overline{RESET} | RESET | \overline{MR} | VDD > $V_{IT}$ | \overline{RESET} | RESET |
|---|---|---|---|---|---|---|---|---|---|
| **TPS3123/8** | | | **TPS3124** | | | **TPS3125/6** | | | |
| L | 0 | L | 0 | L | H | L | 0 | L | H |
| L | 1 | L | 1 | H | L | L | 1 | L | H |
| H | 0 | L | | | | H | 0 | L | H |
| H | 1 | H | | | | H | 1 | H | L |

## Reset Topology

| DEVICES | OPEN DRAIN | PUSH-PULL |
|---|---|---|
| TPS3123 | | X |
| TPS3124 | | X |
| TPS3125 | | X |
| TPS3126 | X | |
| TPS3128 | X | |

**TPS3123-xx**
**TPS3124-xx, TPS3125-xx**
**TPS3126-xx, TPS3128-xx**

SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

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## FUNCTIONAL BLOCK DIAGRAM



† TPS3123/5/6/8
‡ TPS3123/4/8
§ TPS3124/5/6

## TIMING DIAGRAM TPS3123/5/6/8

TPS3123-xx
TPS3124-xx, TPS3125-xx
TPS3126-xx, TPS3128-xx
SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

**TIMING DIAGRAM TPS3123/4//8**



**Output Undefined**          **\* = WDI Disabled**
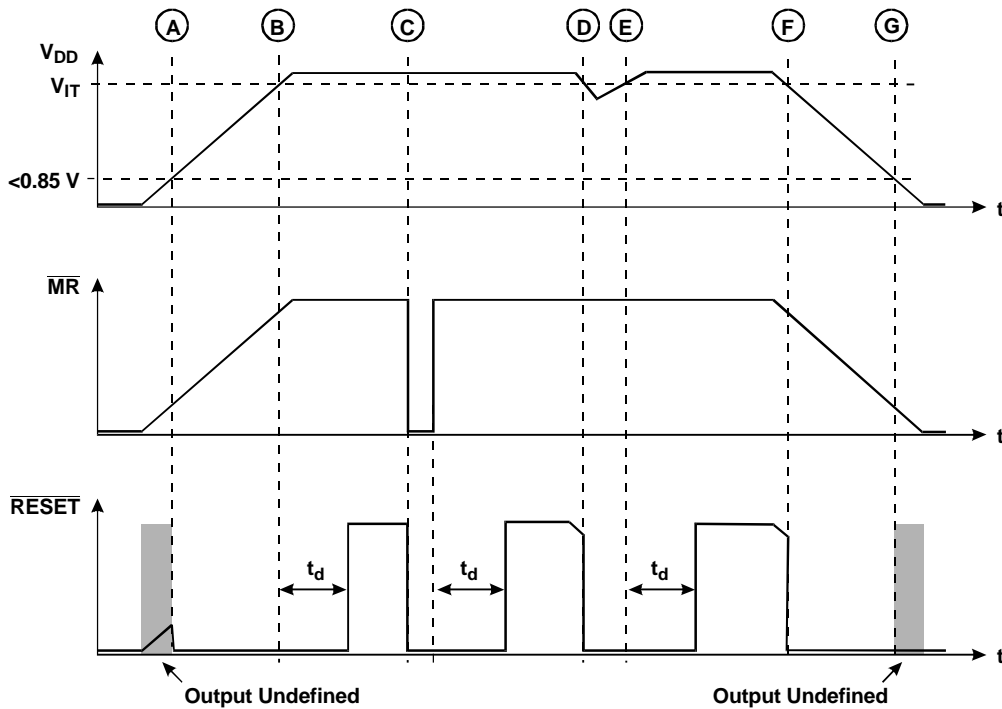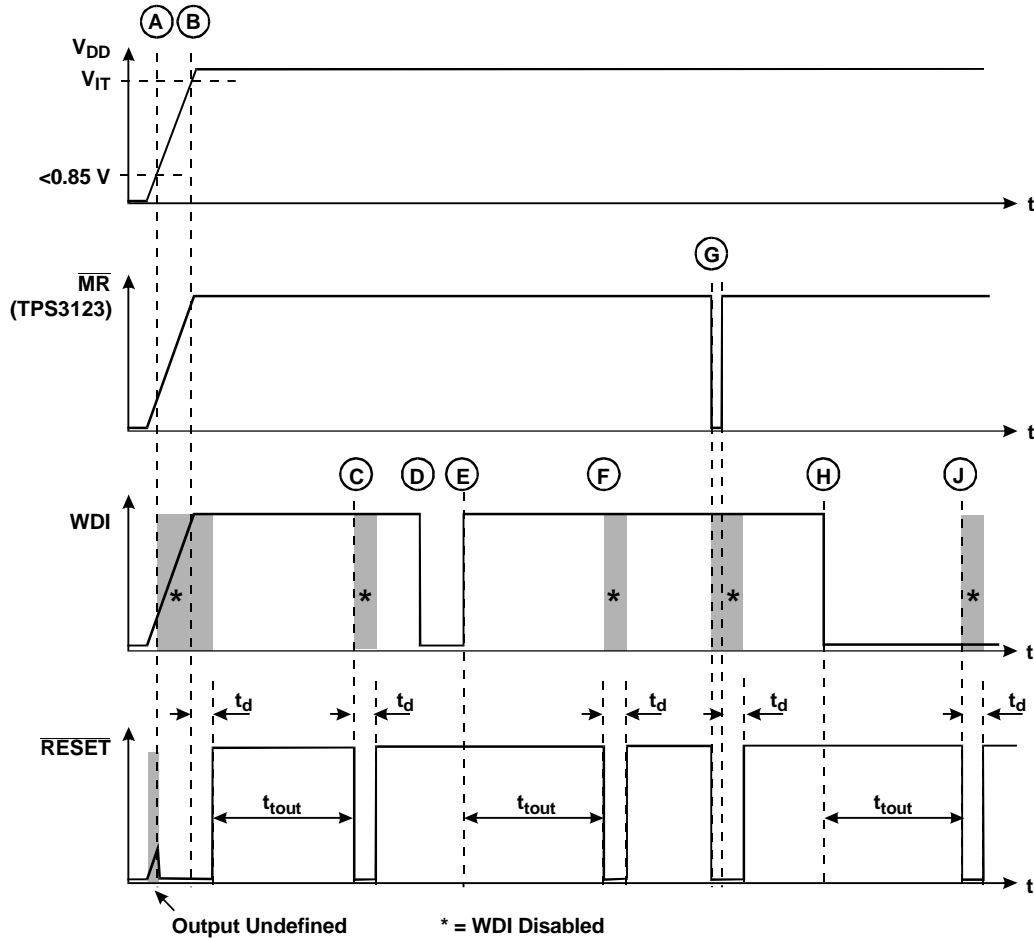
## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

|  | UNIT |
|---|---|
| Manual reset, $\overline{MR}$ | -0.3 V to $V_{DD}$ + 0.6 V |
| Supply voltage, $V_{DD}$ | 3.6 V |
| Watchdog input, WDI | -0.3 V to $V_{DD}$+ 6 V |
| Maximum low output current, $I_{OL}$ | 5 mA |
| Maximum high output current, $I_{OH}$ | -5 mA |
| Input clamp current, $I_{IK}$ ($V_I$< 0 or $V_I$ > $V_{DD}$) | ±10 mA |
| Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) | ±10 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, $T_A$ | -40°C to 85°C |
| Storage temperature range, $T_{stg}$ | -65°C to 150°C |
| Soldering temperature | 260°C |

(1)  Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TPS3123-xx
TPS3124-xx, TPS3125-xx
TPS3126-xx, TPS3128-xx
SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

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## DISSIPATION RATING TABLE

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| DBV | 437 mW | 3.5 mW/°C | 280 mW | 227 mW |

## RECOMMENDED OPERATING CONDITIONS

at specified temperature range

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | $T_A = 0°C$ to $85°C$ | 0.75 | 3.3 | V |
| | $T_A = -40°C$ to $85°C$ | 0.85 | 3.3 | |
| Manual reset voltage, $V_{DD}$ | | 0.0 | $V_{DD}$+0.3 | V |
| Watchdog input voltage, $V_{WD1}$ | | 0 | $V_{DD}$ +0.3 | V |
| High-level input voltage, $V_{IH}$ | | $0.7 \times V_{DD}$ | | V |
| Low-level input voltage, $V_{IL}$ | | | $0.3 \times V_{DD}$ | V |
| Input transition rise and fall rate at WDI, $\Delta t / \Delta V$ | | | 1 | µs/V |
| Operating free-air temperature range, $T_A$ | | 40 | 85 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\overline{MR}$ pullup resistor (internal) | | | | | 27 | | kΩ |
| $I_{IH}$ High-level input current | WDI | WDI = $V_{DD}$ = 3.3 V | | 1 | | 1 | µA |
| | $\overline{MR}$ | $\overline{MR} = 0.7 \times V_{DD}$, | $V_{DD}$ = 3.3 V | 20 | | 55 | |
| $I_{IL}$ Low-level input current | WDI | WDI = 0 V, | $V_{DD}$ = 3.3 V | 1 | | 1 | µA |
| | $\overline{MR}$ | $\overline{MR}$ = 0 V, | $V_{DD}$ = 3.3 V | 80 | | 170 | |
| $I_{OH}$ High-level output current (leakage into $\overline{RESET}$ pin) | TPS3126-xx, TPS3128-xx | $V_{DD} = V_{OH}$ = 3.3 V | | | | 200 | nA |
| $V_{OH}$ High-level output voltage (TPS3123/4/5 only) | $\overline{RESET}$ | $V_{DD}$ = 1.5 V, | $I_{OH}$ = -1 mA | $0.8 \times V_{DD}$ | | | V |
| | | $V_{DD}$ = 3.3 V, | $I_{OH}$ = -4.5 mA | | | | |
| | RESET | $V_{DD}$ = 0.75 V, | $I_{OH}$ = -8 µA | | | | |
| | | $V_{DD}$ = 1.5 V, | $I_{OH}$ = -1 mA | | | | |
| $V_{OL}$ Low-level output voltage | $\overline{RESET}$ | $V_{DD}$ = 0.75 V, | $I_{OL}$ = 15 µA | | | $0.2 \times V_{DD}$ | V |
| | | $V_{DD}$ = 1.5 V, | $I_{OL}$ = 1.4 mA | | | | |
| | RESET | $V_{DD}$ = 1.5 V, | $I_{OL}$ = 1.4 mA | | | | |
| | | $V_{DD}$ = 3.3 V, | $I_{OL}$ = 3 mA | | | 0.4 | |
| $V_{IT-}$ Negative-going input threshold voltage [1] | TPS312xJ12 | $T_A = -40°C$ to $85°C$ | | 1.04 | 1.08 | 1.12 | V |
| | TPS312xG15 | | | 1.35 | 1.40 | 1.45 | |
| | TPS312xJ18 | | | 1.56 | 1.62 | 1.68 | |
| | TPS312xL30 | | | 2.57 | 2.64 | 2.71 | |
| | TPS312xE12 | | | 1.10 | 1.14 | 1.18 | |
| | TPS312xE15 | | | 1.38 | 1.43 | 1.48 | |
| | TPS312xE18 | | | 1.65 | 1.71 | 1.77 | |
| $V_{hys}$ Hysteresis at $V_{DD}$ input | | 1 V < $V_{IT-}$ < 1.4 V | | | 15 | | mV |
| | | 1.4 V < $V_{IT-}$ <2 V | | | 20 | | |
| | | 2 V < $V_{IT-}$ < 3 V | | | 30 | | |

(1) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.

TPS3123-xx
TPS3124-xx, TPS3125-xx
TPS3126-xx, TPS3128-xx

SLVS227B−AUGUST 1999−REVISED FEBRUARY 2004

## ELECTRICAL CHARACTERISTICS  (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DD}$  Supply current | TPS3123-xx TPS3124-xx TPS3128-xx | WDI = $V_{DD}$, $\overline{MR}$ unconnected | $V_{DD}$ = 0.75 V | | 14 | | μA |
| | | | $V_{DD}$ = 3.3 V | | 22 | 30 | |
| | TPS3125-xx TPS3126-xx [(2)] | $\overline{MR}$ unconnected | $V_{DD}$ = 0.75 V | | 14 | | |
| | | | $V_{DD}$ = 3.3 V | | 18 | 25 | |
| $C_i$  Input capacitance at $\overline{MR}$, WDI | | $V_I$ = 0 V to 3.3 V | | | 5 | | pF |

(2)   The supply current during delay time $t_d$ is typical 5 μA higher.

## TIMING REQUIREMENTS

at $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_w$  Pulse width | At $V_{DD}$ | $V_{IH}$ = $V_{IT-}$ + 0.2 V, | $V_{IL}$ = $V_{IT-}$ -0.2 V | | 6 | | | μs |
| | At $\overline{MR}$ | $V_{DD} \geq V_{IT-}$ + 0.2 V, | $V_{IL}$ = 0.3 x $V_{DD}$, | $V_{IH}$ = 0.7 × $V_{DD}$ | 1 | | | |
| | At WDI | | | | 0.1 | | | |

## SWITCHING CHARACTERISTICS

at $R_L$ = 1 MΩ, $C_L$ = 50 pF, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{tout}$ | Watchdog time out | | $V_{DD} \geq V_{IT-}$ + 0.2 V, See timing diagram | 0.8 | 1.4 | 2.1 | s |
| $t_d$ | Delay time | | $V_{DD} > V_{IT-}$ + 0.2 V, See timing diagram | 100 | 180 | 260 | ms |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $\overline{MR}$ to $\overline{RESET}$ delay (TPS3123/5/6/8) | $V_{DD} \geq V_{IT-}$+ 0.2 V, $V_{IL}$ = 0.2 × $V_{DD}$, $V_{IH}$ = 0.8 × $V_{DD}$ | | | 0.1 | μs |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $\overline{MR}$ to RESET delay (TPS3125/6) | | | | 0.1 | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $V_{DD}$ to $\overline{RESET}$ delay | $V_{IL}$ = $V_{IT-}$ - 0.2 V, $V_{IH}$ = $V_{IT-}$ + 0.2 V | | | 10 | μs |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $V_{DD}$ to RESET delay (TPS3124/5/6) | | | | 10 | |

**TPS3123-xx**
**TPS3124-xx, TPS3125-xx**
**TPS3126-xx, TPS3128-xx**

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## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**



Figure 2.

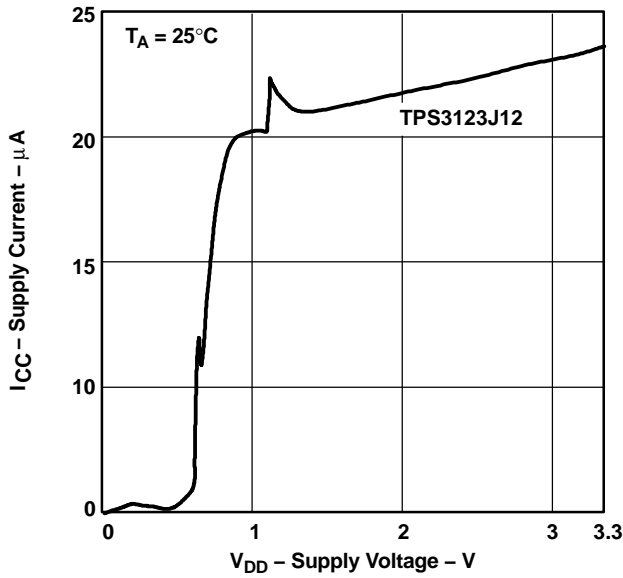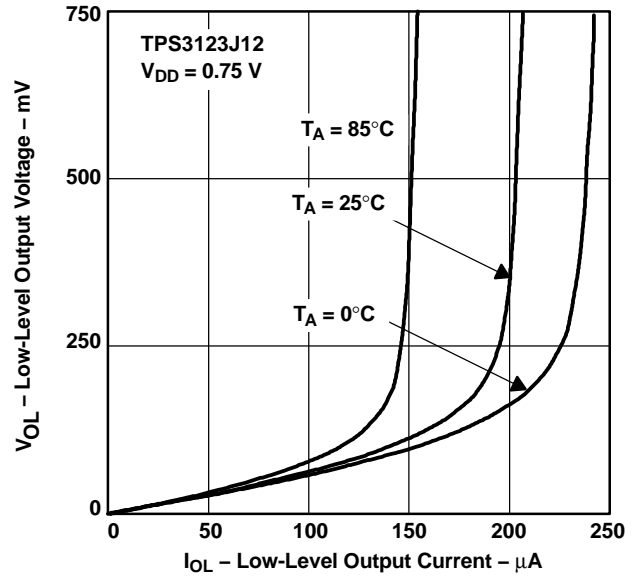**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**



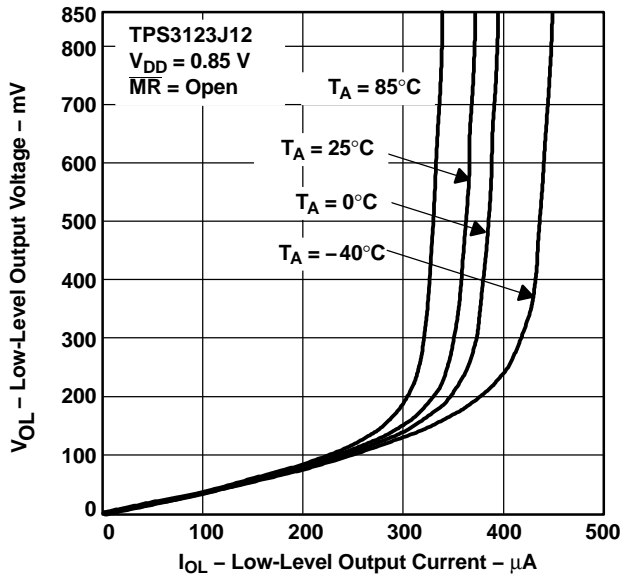Figure 3.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**



Figure 4.

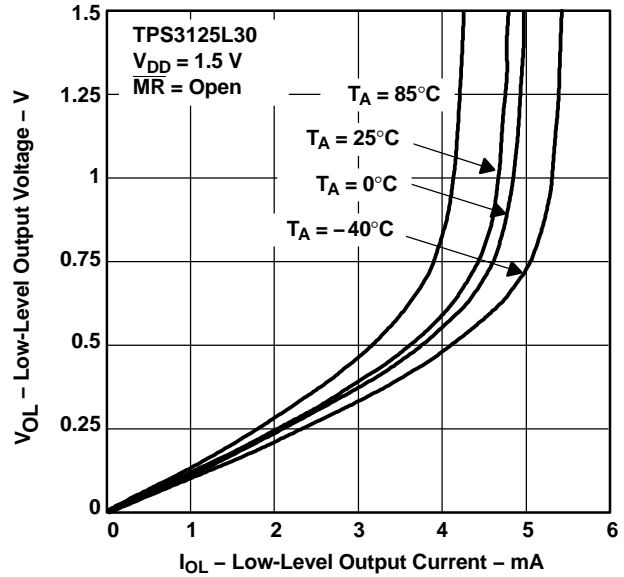**LOW-LEVEL OUTPUT VOLTAGE
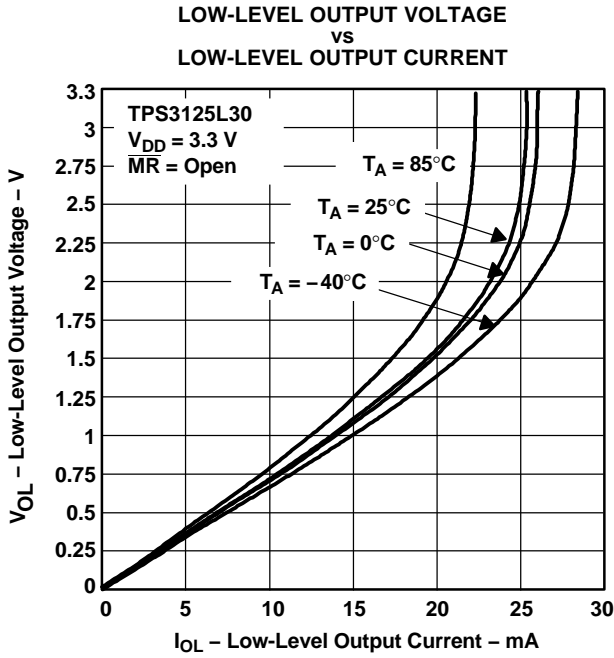vs
LOW-LEVEL OUTPUT CURRENT**



Figure 5.

TPS3123-xx
TPS3124-xx, TPS3125-xx
TPS3126-xx, TPS3128-xx
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## TYPICAL CHARACTERISTICS (continued)

**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**



Figure 6.

**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**



Figure 7.

**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**



Figure 8.

**NORMALIZED INPUT THRESHOLD VOLTAGE**
**vs**
**FREE-AIR TEMPERATURE**



Figure 9.

TPS3123-xx
TPS3124-xx, TPS3125-xx
TPS3126-xx, TPS3128-xx

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## TYPICAL CHARACTERISTICS (continued)

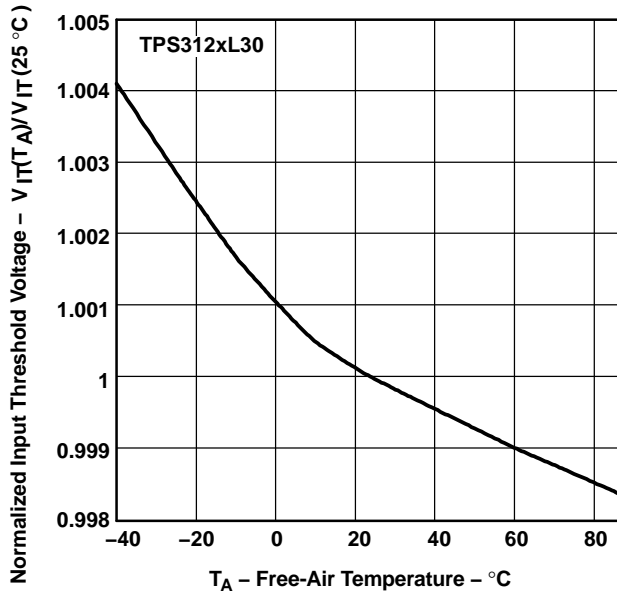NORMALIZED INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



Figure 10.

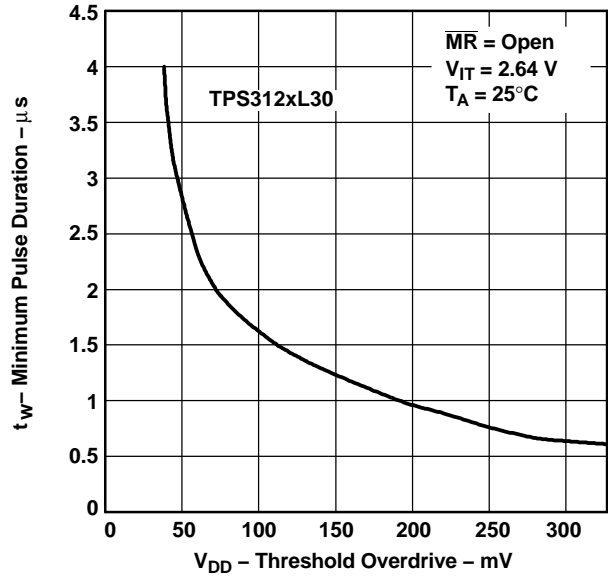MINIMUM PULSE DURATION
vs
THRESHOLD OVERDRIVE



Figure 11.

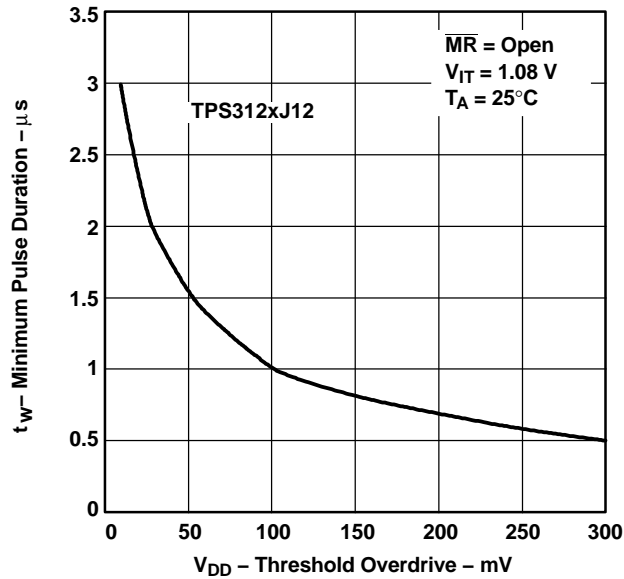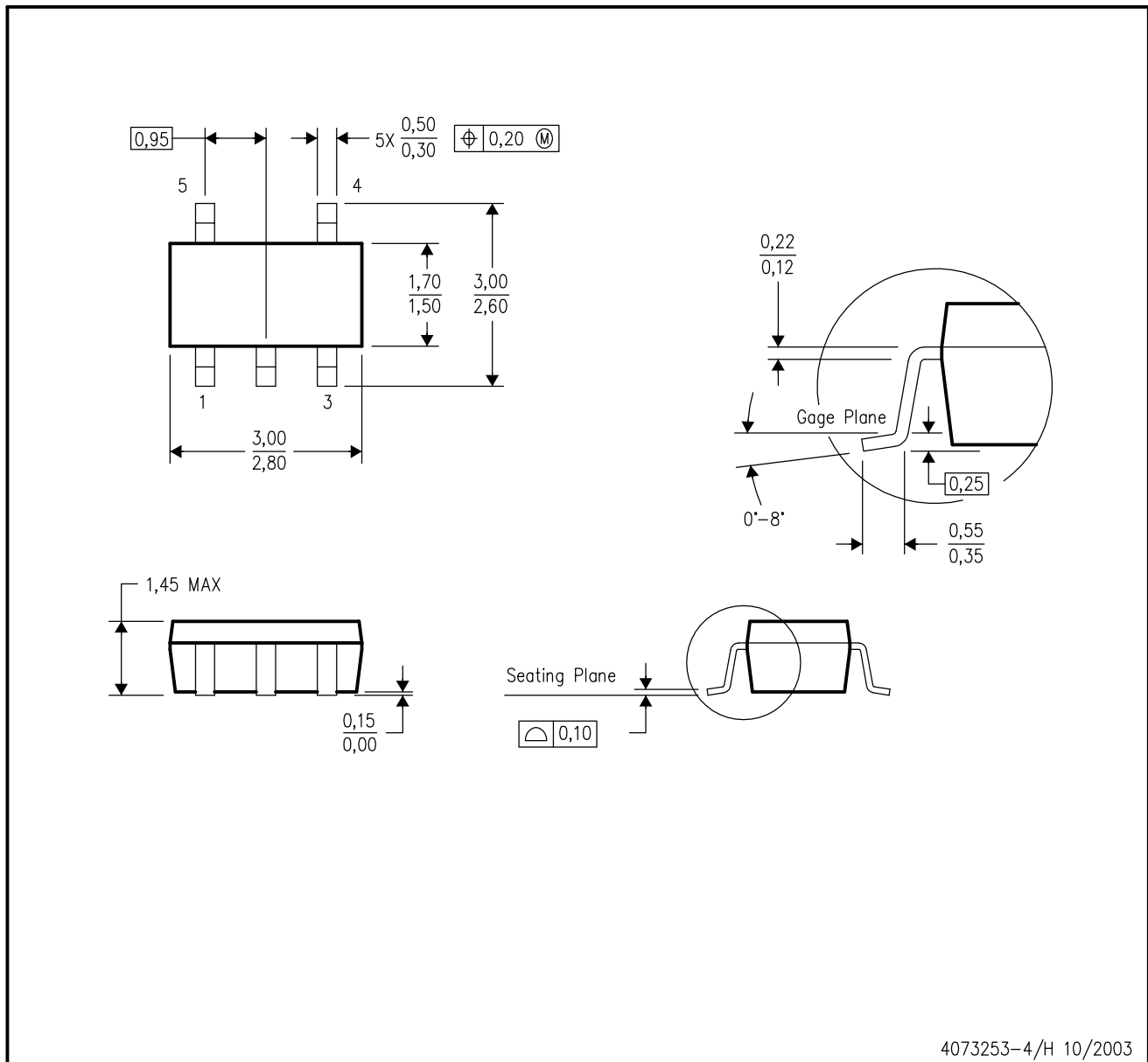MINIMUM PULSE DURATION
vs
THRESHOLD OVERDRIVE



Figure 12.

# DBV (R−PDSO−G5)    PLASTIC SMALL−OUTLINE PACKAGE

0,95

5X 0,50 / 0,30    0,20 (M)

5    4

1,70 / 1,50    3,00 / 2,60

1    3

3,00 / 2,80

0,22 / 0,12

Gage Plane

0,25

0°−8°

0,55 / 0,35

1,45 MAX

0,15 / 0,00

Seating Plane

0,10

4073253−4/H 10/2003

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO−178 Variation AA.

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