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W83791D/W83791G
Winbond H/W
Monitoring IC

W83791D/W83791G
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.			n.a.	All version before 0.50 are for internal use.
2	n.a.	01/Jan	0.5	n.a.	First publication.
3	P.7 P.34	01/Jan	0.51	n.a.	(1) Revise SLOTOCC# pin description. (2) Add SMI# /IRQ for Voltage/Fan description.
4	P.43/44	01/Mar	0.6	n.a.	Register Index 1Ah~1Fh revised.
5	P. 40 P. 42 P. 60/61 P. 58/59 P. 66 P. 66 P. 66 P. 87	01/May	0.7	n.a.	This update is for **C version** IC. 1) Add EVNTRAP1-5 polarity (Index Ah) 2) Add VID protection control bit (Index15h bit5) 3) Add FAN1-3/PWMOUT1-3 as GPIn data register. (Index 95h/97h) 4) SMARTFAN™ step up/down time registers exchanged. 5) Add a bit (Index A6 bit7) to know either speech or GPIO function did you use. 6) Pin44 (SMI#/LEDOUT) is a multi-function, it is programmable. 7) EVENTRAP can as GPIO by programming Index A6h bit0-4 . 8) Updated V0.17 schematics adding LEDOUT circuit for SMI# (Pin 44)
6	All pages	01/Aug	0.71	n.a.	Repaginate datasheet
7	n.a.	02/Apr	1.0	1.0	Change all version include version on web to 1.0
8	n.a.	06/Apr	1.1	1.1	Add lead-free package version

winbond

Table of Contents-

1. GENERAL DESCRIPTION

W83791D/G is an evolving version of the W83782D/G --- Winbond's most popular hardware status monitoring IC. Besides the conventional functions of W83782D/G, W83791D/G uniquely provides several innovative features such as speech function, ASF sensor compliant, SMBus 2.0 ARP command compatible, VID table selection trapping, and 5VID output control. Conventionally, W83791D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and efficiently. As for data access, W83791D/G provides slave SMBus 2.0 interface which can reply PEC (Packet Error Code) when as ASF sensor.

An 8-bit analog-to-digital converter (ADC) was built inside W83791D/G. W83791D/G can simultaneously monitor 10 analog voltage inputs (including power VDD/5VSB monitoring), 5 fan tachometer inputs, 3 remote temperatures, and one case open detection signal. The sense of remote temperature can be performed by thermistors, 2N3904 NPN-type transistors, or directly from Intel™ CPU with thermal diode output. W83791D/G provides 3 PWM (pulse width modulation) outputs for two modes of smart fan control-**"** Thermal Cruise™ **"** mode and **"**Speed Cruise**"** mode. Under **"** Thermal Cruise™ **"** mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. **"**Speed Cruise**"**, namely, is to keep the fan operate in the specific programmable r.p.m. As for warning mechanism, W83791D/G provides speech voice warning, beep tone warning, and SMI#, OVT#, IRQ signals for system protection events.

Additionally, 5 VID inputs are provided to read the VID of CPU (i.e. Pentium™ II/III) if applicable. These VID inputs provide the information of Vcore voltage that CPU expects. Furthermore, W83791D/G provides programmable VID output control to alter the voltage CPU consumes. W83791D/G also uniquely provides an optional feature: early stage (before BIOS was loaded) beep / speech warning to detect if the fatal elements present --- Vcore or +3.3V voltage fail and thus the system can not be boomed up. If the VSB power on setting refers to Intel VRM 9.x, the VID table within W83791D/G will be according to the new one. W83791D/G also has 2 specific pins to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C™ interface.

W83791D/G speech function is enabled by building in a programmable speech synthesizer with a 9-bit current DAC output as well as a connectable external flash memory for storing voice data. W83791D/G supports 1 CPU present or absent event trap, 5 external event traps, 17 hardware monitor event traps (10 analog voltage, 3 fan tachometer, 3 remote temperature, 1 case open) and 128 internal programmable event traps, amounting to 151 different speech outputs. If more than two events happen simultaneously, the priority set is: SLOTOCC# > EVNTRP1 > EVNTRP2 > EVNTRP3 > EVNTRP4 > EVNTRP5 > 128 Programmable events (Bank0 index 09h) > 17 Hardware status events. Voice data stored in the external flash memory interface with Winbond W55FXX is flexible to change by Winbond application software and **on-line** programming flash data is provided also. Besides, an external resistor is added to provide ring oscillator.

When you do not use the speech function, W83791D/G provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a pre-defined alternate function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.

W83791D/G can uniquely serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent state. Through W83791D/G compliance with ASF sensor spec, network server is able to monitor the environmental status of the client in OS-absent state by PET frame values returned from W83791D/G, such as temperatures, voltages, fan speed, and case open. Moreover, W83791D/G supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address to W83791D/G after W83791D/G's UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, Intel™ LDCM (LanDesk Client Management), or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable and maskable interrupts. An optional beep tone could be used as a warning signal when the monitored parameters are out of the preset range.

2. FEATURES

2.1 Monitoring Items

- 10 voltage inputs
  --- Typical for VCORE, +3.3V, +12V, -12V, +5V, -5V, +5VSB, VBAT, and two reserved
- 5 fan speed monitoring inputs
- 3 temperature inputs from remote thermistors, 2N3904 NPN-type transistors or Pentium™ II (Deschutes) thermal diode output
- Case open detection input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.2 Address Resolution Protocol (ARP) and Alert-Standard Forum (ASF)

- Support System Management Bus (SMBus) version 2.0 specification
- Comply with hardware sensor slave ARP (Address Resolution Protocol)
- Response sensor type ARP command
- Response ASF command --- Get Event Data , Get Event Status
- Comply with ASF sensors (Monitoring fan speed, voltage, temperature, and case open)

2.3 Speech Items

- Programmable speech synthesizer with new high fidelity synthesis algorithm
- Build in 8-bit current D/A converter
- 1 CPU present or absent trigger input
- 5 External trigger inputs
- 128 Internal programmable trigger inputs
- 17 H/W Monitor event trigger inputs
- Programmable 0-255 seconds timeout trigger inputs for firmware or software
- Instruction cycle is <= 400 uS typically
- Section control provided in each voice section
- External resistor for ring oscillator

2.4 Actions Enabling

- Beep tone warning separated speech output
- 5 PWM (pulse width modulation) outputs for fan speed control (1~3 support Smart Fan control) and 5 Fan speed inputs for monitoring --- Total up to 5 sets of fan speed monitoring and controlling
- Issue SMI#, OVT#, IRQ signals to activate system protection
- Warning signal pop-up in application software

2.5 Enhance Monitoring VID function

- CPU Voltage ID reading
- VID output control
- Enhance beep warning by detecting Intel VRM 9.0 VID

2.6 General

- I^2C^{TM} serial bus interface
- 5 VID input pins for CPU VCORE identification (for Pentium™ II/III)
- Initial power fault beep (for +3.3V, VCORE)
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C^{TM} interface

Winbond hardware monitoring application software (Hardware Doctor™) support, for both Windows 95/98/2000 and Windows NT 4.0/5.0

- Internal clock Oscillator with 3M Hz
- 5V VSB operation

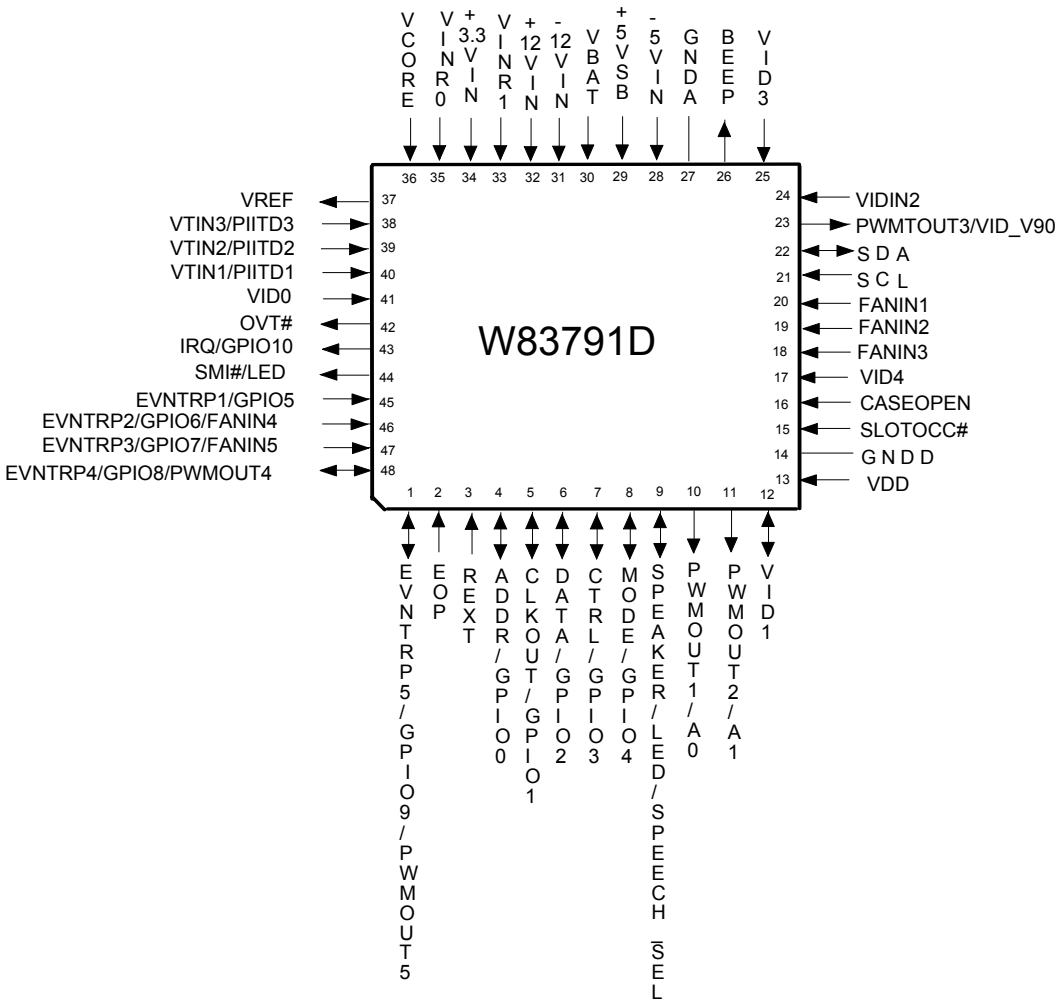
2.7 Package

- 48-pin LQFP

3. KEY SPECIFICATIONS

• Voltage monitoring accuracy	±1% (Max)
• Intel VRM 9.x Voltage monitoring accuracy	±0.5% (Max)
• Monitoring Temperature Range and Accuracy	
- 40°C to +120°C	± 3°C(Max)
• Supply Voltage	5V
• Operating Supply Current	5 mA typ.
• ADC Resolution	8 Bits

4. PIN CONFIGURATION



5. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts} - TTL level and schmitt trigger with 12 mA source-sink capability
I/O_{8ts} - TTL level and schmitt trigger with 8 mA source-sink capability
I/O_{6ts} - TTL level and schmitt trigger with 6 mA source-sink capability
I/OD_{12ts} - TTL level and schmitt trigger open drain output with 12 mA sink capability
OUT_{12} - Output pin with 12 mA source-sink capability
OD_{12} - Open-drain output pin with 12 mA sink capability
AOUT - Output pin (Analog)
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
AIN - Input pin (Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
EVNTRP5 /	1	I/O_{12t}	Event trapping to selection speech output sound. Default is high edge trigger.
GPIO9/ PWMOUT5			General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or PWMOUT Fan control can be selected by registers, but the PWMOUT can not support Smart Fan.
EOP	2	I	End of Process signal input from cascaded Flash.
GPIO11		I/OD_{12ts}	General purpose I/O function pin. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
REXT	3	I	Resistor (Rosc) connect to VSB used to adjust ring oscillator frequency.
ADDR /	4	OUT_{12}	Speech address pulse output, connect to W55FXX. When this pin translates from logic high to logic low, it will latch the data pin 6 and shift it into a speech flash address counter.
GPIO0		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
CLKOUT /	5	OUT_{12}	Speech clock output, for speech data read-out and write-in, connect to W55FXX. When this pin translates from logic high to logic low, the data pin 6 will be latched by this clock.
GPIO1		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
DATA /	6	I/O_{12t}	Serial data input/output, connect to W55FXX. The pin is latched by CLKOUT and ADDR acted as speech data and address respectively.
GPIO2		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
CTRL /	7	OUT_{12}	Output clock numbers of this pin decide which mode is selected. Connect to W55FXX.
GPIO3		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
MODE /	8	OUT_{12}	Output mode signal to W55FXX serial Flash.
GPIO4		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
SPEAKER	9	OUT_{12}	Current type output driving an external speaker. The function is only working in VDD 5V OK.
LED		OUT_{12}	LED output control. This is a multi-function pin with SPEAKER. When the LED_SEL register (Bank0 Index 17h) is set to 1, LED output function will be active. Otherwise, set to 0 (default), this pin serves as SPEAKER output.
SPEECH_SEL		IN_{ts}	During VSB 5V power on, this pin is used to trap whether using speech function or GPIO function. Trapping low means using speech function (i.e. pin45-48, pin1, pin4-8 are as speech function). Trapping high means using GPIO function (i.e. pin45-48, pin1, pin4-8 are as GPIO function). The I/O control and status is defined in BANK0 Index 13h~16h.
PWMOUT1/	10	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A0		IN_{ts}	I^2C device address bit0 trapping during 5VSB power on.
PWMOUT2 /	11	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A1		IN_{ts}	I^2C device address bit1 trapping during 5VSB power on.
VID1	12	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VDD (5V)	13	POWER	+5V VDD power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
GNDD	14	DGROUND	Internally connected to all digital circuitry.
SLOTOCC#	15	IN_{ts}	CPU presence signal. 0 means CPU is present. 1 means CPU is absent.
CASEOPEN	16	I/O_{6ts}	CASE OPEN detection. An active high input from an external device when case is Intruded. This signal can be latched in external circuit which power is supplied by VBAT, even if W83791D/G is power off.
VID4	17	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
FAN3IN-FAN1IN	18-20	IN_{ts}	0V to +5V amplitude fan tachometer input
SCL	21	IN_{ts}	Serial Bus Clock.
SDA	22	I/OD_{8ts}	Serial Bus bi-directional Data.
PWMOUT3 /	23	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
VID_V90		IN_{ts}	VID table selection trapping during RSMRST (0: Intel VRM 8.2/8.3; 1: Intel VRM 9.0). When the trapping pin get a logic 1, the beep warning function is according to Intel VRM 9.0 VID.
VID2	24	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
VID3	25	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
BEEP	26	OD_{12}	Alarm beep output. Normal, this pin is low. When abnormal event happens, this pin will output alarm frequency.
GNDA	27	AGROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-5VIN	28	AIN	0V to 4.096V FSR Analog Inputs.
+5VSB	29	POWER	This pin is power for W83791D/G. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
VBAT	30	POWER	This pin is power for W83791D/G.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
-12VIN	31	AIN	0V to 4.096V FSR Analog Inputs.
+12VIN	32	AIN	0V to 4.096V FSR Analog Inputs.
VINR1	33	AIN	0V to 4.096V FSR Analog Inputs.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
VINR0	35	AIN	0V to 4.096V FSR Analog Inputs.
VCORE	36	AIN	0V to 4.096V FSR Analog Inputs.
VREF	37	AOUT	Reference voltage.
VTIN3 / PIITD3	38	AIN	Thermistor 3 terminal input. (Default) Pentium™ II diode 3 input. This multi-functional pin is programmable.
VTIN2 / PIITD2	39	AIN	Thermistor 2 terminal input. (Default) Pentium™ II diode 2 input. This multi-functional pin is programmable.
VTIN1 / PIITD1	40	AIN	Thermistor 1 terminal input. (Default) Pentium™ II diode 1 input. This multi-functional pin is programmable.
VID0	41	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
OVT#	42	OD_{12}	Over temperature Shutdown Output for temperature sensor 1-3.
IRQ / GPIO10	43	OUT_{12} I/OD_{12ts}	Interrupt request. General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
SMI# / LED	44	OD_{12} OUT_{12}	System Management Interrupt (open drain). LED output control. This is a multi-function pin with SMI. When the register (Bank0 Index 17h bit7 and Index A6h bit 6) is set to 1, LED output function will be active. Otherwise, set to 0 (default), this pin serves as SMI#.
EVNTRP1/ GPIO5	45	I/O_{12ts}	Event trapping to selection speech output sound. Default is high edge trigger. General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this speech function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin can be selected by registers.

PIN DESCRIPTION, continued

PIN NAME	PIN NO.	TYPE	DESCRIPTION
EVNTRP2-3/	46-47	I/O_{12ts}	Event trapping to selection speech output sound. Default is high edge trigger.
GPIO6-7/ FANIN4-5		I/O_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this speech function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or FAN inputs can be selected by registers.
EVNTRP4/	48	I/O_{12ts}	Event trapping to selection speech output sound.
GPIO8/ PWMOUT4		I/O_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or PWMOUT Fan control can be selected by registers, but the PWMOUT can not support Smart Fan.

6. FUNCTION DESCRIPTION

6.1 General Description

The W83791D/G provides 10 analog positive inputs, 5 fan speed inputs , at most 5 sets for fan PWM (Pulse Width Modulation) control, 3 thermal inputs from remote thermistors, 2N3904 transistors or Pentium™ II/III (Deschutes) thermal diode outputs, case open detection and beep function output when the monitored values exceed preset ranges, including the voltage, temperature, and fan count. Moreover, W83791D/G uniquely provides several innovative and practical functions to make the whole system more efficient and compliant with future trend of network management, such as speech function, ASF sensor compliant, SMBus 2.0 ARP command compatible, VID table selection trapping, 5VID output control, and so forth. Once the monitoring function of W83791D/G is enabled, the watch dog machine will monitor every function and store the values to registers for comparison with preset ranges. If the monitoring value exceeds the limit value, the interrupt status will be set to 1 and W83791D/G will issue interrupt signals such as SMI# and IRQ if not masked..

6.2 Access Interface

The W83791D/G provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83791D/G, there are three serial bus addresses. Through the first address defined at CR [48h], all the registers can be read and written except CPUT1/CPUT2 temperature sensor registers. The read/write of the CPUT1/CPUT2 temperature sensor registers can be implemented through the second address (defined at CR [4Ah] bit2-0) and the third address (defined at CR [4Ah] bit6-4).

The first serial bus address of W83791D/G has 2 hardware setting bits set by pin10-11. The address is 001011[pin11], and [pin10]. Hence, the content of CR [48h] would be 00101110 if pin11=1 and pin10=0.

6.2.1 The first serial bus access timing

(a) Serial bus writes to internal address register followed by the data byte

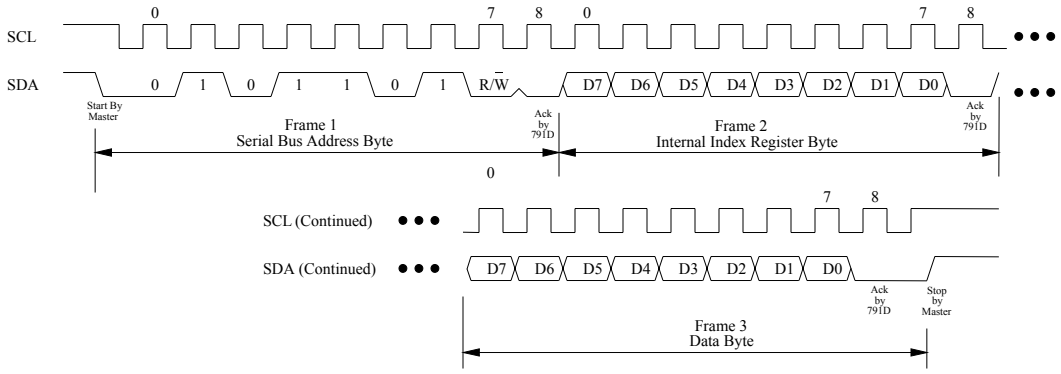


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

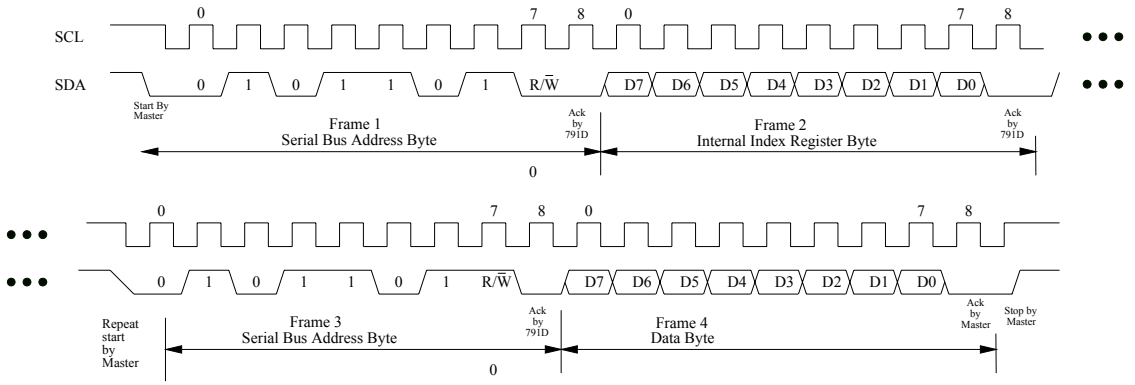


Figure 2. Serial Bus Read from Internal Address Register

6.3 Speech Function

6.3.1 General Description

The W83791D/G is a derivative of Winbond's *PowerSpeech*™ synthesizers. There are up to 5 hardware trigger inputs, 17 Hardware Monitor event and 128 programmable software event trigger inputs. If more than two events happen simultaneously, the priority set by the internal H/W is: SLOTOCC# > EVNTRAP1 > EVNTRAP2 > EVNTRAP3 > EVNTRAP4 > EVNTRAP5 > TRIGREG (Index 09h) 128 events > VIN0 > VIN1> others (VIN2 –VIN9, TEMP, FAN, case open). Software trigger is able to accommodate 128 event triggers, with timeout register (index 08h) enabled in advance for allowance of time on detecting devices. That is, once the system's power is on, BIOS can fill trigger event and speech voice will not be sent till the system fails owing to timeout. In addition, to prevent events from taking place simultaneously.

6.3.2 Event Trigger Queue

W83791D/G provides 8 byte FIFO queue to store event trigger, for example, the first 8 event can be served by speech and speech will clear FIFO queue after service. Coding of Speech program must assign correct CPU_MODE event vector to issue correct speech voices correspondent to speech trigger events. For example, CPU_MODE event vector =1 represents absence of CPU, then coding speech with CPU is absent voice. When W83791D/G detects no CPU exists, it will send vector = 1 to speech synthesizer and play this voice data. Following is the block diagram of the 8-Byte event trigger queue.

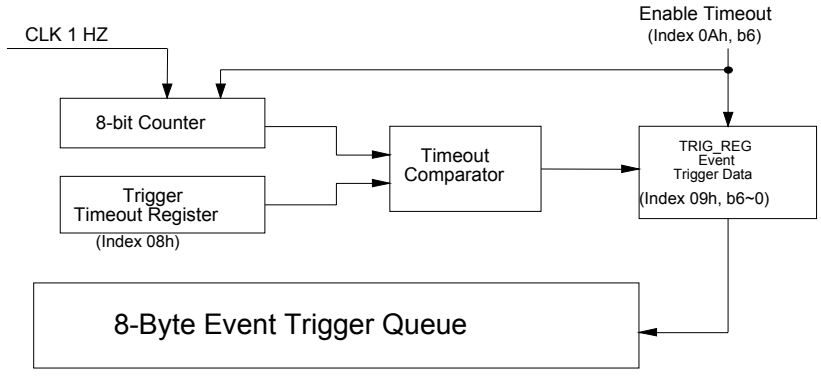


Figure 3. Event trigger Queue

As BIOS usually has POST (Power On Self Test) program, then it will test every item step by step if no failure takes place, however, if it detects a failure on a specific item, it will hang on there. Therefore, BIOS could write timeout value to register 08h and start timer setup speech trigger event (register 09h), then is BIOS test program started. Whenever the system is hang on specific item such as DRAM testing, W83791D would say “DRAM test fails” after the timeout previously set at CR [08h]. On the contrary, if DRAM test is ok, then BIOS could update the timeout value and proceed to the next test program.

Below is the speech CPU_MODE table of W83791D/G**:**

CPU_MODE ITEM	DEFINITION	VECTOR (H)
POI	Reserverd	0,32
SLOTOCC	CPU present or absent	1
EVNTRAP1(TG1)	Hardware trgger1	2
EVNTRAP2	Hardware trgger2	3
EVNTRAP3	Hardware trgger3	4
EVNTRAP4	Hardware trgger4	5
EVNTRAP5	Hardware trgger5	6
TRIGREG	I2C setting software trigger	80-FF
IN0	Vcore(VIN0) exceed limit	40
IN1	VINR0(VIN1) exceed limit	41
IN2	(+3.3VIN)VIN2 exceed limit	42
IN3	(5VDD)VIN3 exceed limit	43
IN4	(+12VIN)VIN4 exceed limit	44
IN5	(-12VIN)VIN5 exceed limit	45
IN6	(-5VIN)VIN6 exceed limit	46
IN7	VSB(VIN7) exceed limit	47
IN8	VBAT(VIN8) exceed limit	48
IN9	(VINR1)VIN9 exceed limit	49
TEMP1	VTIN1 exceed limit	4A
TEMP2	VTIN2 exceed limit	4B
TEMP3	VTIN3 exceed limit	4C
FAN1	FAN1 count over limit	4D
FAN2	FAN2 count over limit	4E
FAN3	FAN3 count over limit	4F
CHS_EV	Case open trigger	50

Table 1 CPU_MODE

6.3.3 Connection of EEPROM

As described previously the W83791D/G has connectable W55FXX to store voice data. To expand the storage capacity, users can select many W55FXX to connect with each other. The maximum capacity could be up to 16Mbit. Following is the connection chart of W55FX with W83791D/G.

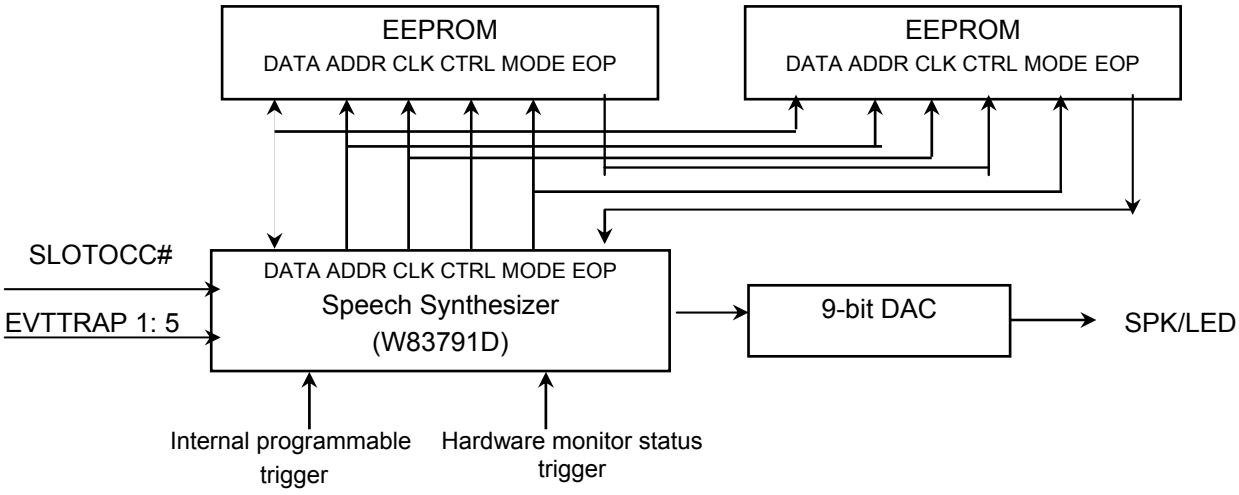


Figure 4 Speech Function Diagram

6.3.4 Speaker Output

Speech output pin is a 8 bit Current D/A converter, with which loading is needed. The resistor could range from 510~1K ohm and bipolar could be a low power NPN bipolar with β of 120 - 160. Usually, an 8050D transistor is appropriate. The spec of speaker is 8 Ω. Besides, SPK can also connect to AC97 codec chip Line_Out. C is decouple capacitor and is usually 200p- 0.01uF

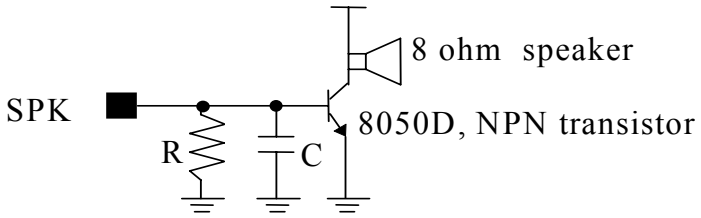


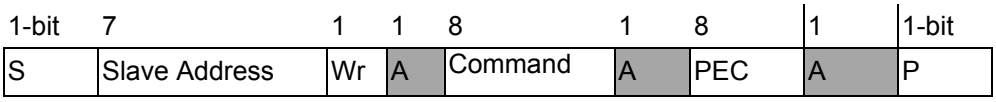
Figure. 5

6.4 Address Resolution Protocol (ARP) Introduction

As the W8791D/G is a slave device existing on the System Management Bus, it must have a unique address to prevent itself from conflicting with the other devices existing on the same bus. In order to solve the problem of address conflicts, SMBus version 2.0 introduces the concept of dynamically assigned address called Address Resolution Protocol (ARP). By such mechanism, each device existing on the SMBus will be given a unique slave address if it is a ARP-capable device. Thus, to meet the new spec, W83791D/G uniquely provides ARP compliant function to acquire a unique slave address.

The typical process of ARP contains several steps, including Prepare to ARP, Reset Device, Get UDID, Assign Address, and so on. Whenever the slave device accepts the command of ARP master, it must reply an Acknowledgement to the ARP master, thus the ARP master is able to carry on the next step. In order to provide a mechanism to isolate device for the purpose of address assignment, each device must implement a unique device identifier (UDID). The UDID is a 128-bit number comprised of several field, including Device Capabilities, Version Revision, Vendor ID, Device ID, Interface, Subsystem Vendor ID, Subsystem Device ID, and Vendor Specific ID. After the UDID of the device is sent to the ARP master, the ARP master will then assign a random address not in the Used Address Pool to the device

Generally speaking, there are eleven possible commands to read /write the data of SMBus device, and a slave device may use any or all of the eleven protocols to communicate. These protocols are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read word, Process Call, Block Write, and Block Write-Block Read Process Call. W83791D/G itself supports the Block Write-Block Read Process with PEC to communicate with ARP Master. Following is a description of the SMBus packet protocol diagrams element key. Not all protocol elements will be present in every command, that is, not all packets are required to include the Packet Error Code.



S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
A	Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P	Stop Condition
PEC	Packet Error Code
	Master-to-Slave
	Slave-to-Master

Relative command list:

SLAVE ADDRESS	COMMAND	DESCRIPTION
C2h	01h	Prepare to ARP
C2h	02h	Reset device (general)
C2h	03h	Get UDID (general)
C2h	04h	Assign address
C2h	Slave_Addr | 1	Direct Get UDID
C2h	Slave_Addr | 0	Direct Reset
C2h	05h-1Fh	Reserved.

Following is an example of the Block Write-Block Read Process Call. The Block Write-Block Read Process Call is a two-part message. It begins with a salve address and a write condition. After the command code the host issues a write count M that describes how many more bytes will be written in the first part of the message. The second part of the message is a block of read data beginning with a repeated start condition followed by thee salve address and a Read Bit. The next read byte count N indicates how many more data will be read in the second part of the message. Note that the combined data payload must not exceed 32bytes. Besides, W83791D/G also provides packet error code (PEC) to insure the accuracy during data transmission.

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	…

8	1	…	8	1	
Data Byte 2	A	…	Data Byte M	A	…

1	7	1	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Byte Count=N	A	Data Byte 1	A	…

8	1	…	8	1	8	1	1
Data Byte 2	A	…	Data Byte N	A	PEC	A	P

6.5 ASF (Alert Standard Format) Introduction

In order to implement network management in OS-absent, W83791D/G provides ASF Response Registers to meet ASF sensor spec. As a result, the network server is able to monitor several environmental status of the client in OS-absent by PET frame values returned from W83791D/G, including temperature, voltage, fan speed, and case open. In below is the ASF diagram:

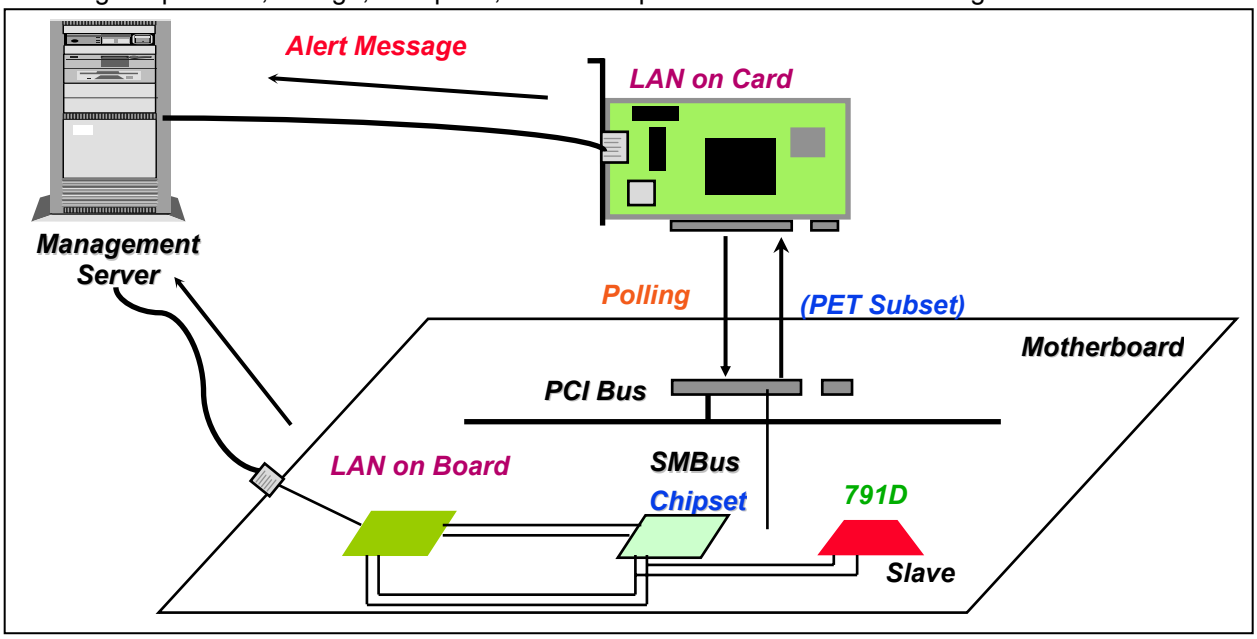


Figure 6. ASF Block Diagram

6.5.1 Platform Event Trap (PET)

PET is the ASF transmit protocol used to provide common fields for trap regardless of trap source. The variable bindings fields in a PET frame contain the system and sensor information for an event, such as event sensor type, event type, event offset, event source type, sensor device, sensor number, entity ID, entity instance, event status index, event status, and event severity. Each field has its definition and is described in the following table.

PET VARIABLE BINDING FIELD	DESCRIPTION
Event Sensor Type	The Event Sensor Type field indicates what types of events the sensor is monitoring. E.g. temperature, voltage, fan, etc.
Event Type	The Event Type indicates what type of transition/state change triggered the trap.
Event Offset	The Event Offset indicates which particular event occurred for a given Even Type.
Event source Type	The Event Source Type describes the originator of the event. It is ASF1.0 (68h) for all PET frames defined by this specification.

Platform Event Trap (PET), continued.

PET VARIABLE BINDING FIELD	DESCRIPTION
Sensor Device	The Sensor Device is the SMBus address of the sensor that caused the event for the PET frame.
Sensor Number	The Sensor Number is used to identify a given instance of a sensor relative to the Sensor Device.
Entity ID	The Entity ID indicates the platform entity the event is associated with. E.g. processor, system board, etc.
Entity Instance	The Entity Instance indicates which instance of the Entity the event is for. E.g. processor 1 or processor 2.
Event Status Index	The Event Status Index identifies a unique event monitored by the ASF-sensor. It is zero-based, sequential, continuous, and ranging form 0-37h.
Event Status	The Event Status indicates the event state of the ASF-sensor device associated with the message's Event Status Index.
Event Severity	The Event Severity gives the management station an indication of the severity of the event in the PET frame. Typical values are Monitor (0x01), Non Critical (0x08), or Critical Condition (0x10).

Following is the illustration of ASF SMBus command for Get Event Data.

1	7	1	1	8	1	8	1	
S	Slave Address	Wr	A	Command	A	Wr Byte Count	A	…
	ASF-sensor Address	0	0	Sensor Device 0000 0001	0	0000 0100	0	

8	1	8	1	8	1	8	1	
Wr Data 1	A	Wr Data 2	A	Wr Data 3	A	Wr Data 4	A	…
Sub Command Get Event Data 0001 0001	0	Version Number 0001 0000	0	Event Status Index 00ii iiii	0	Reserved 0000 0000	0	

1	7	1	1	8	1	
Sr	Slave Address	R	A	Rd Byte Count	A	…
	ASF-sensor Address	1	0	0000 1010 to 0000 1111	0	

1	8	1	8	1	8	1	
A	Rd Data 1	A	Rd Data 2	A	Rd Data 3	A	…
0	Status	0	Event Sensor Type	0	Event Type	0	

8	1	8	1	8	1	8	1	
Rd Data 4	A	Rd Data 5	A	Rd Data 6	A	Rd Data 7	A	…
Event Offset	0	Event Source Type	0	Event Severity	0	Sensor Device	0	

8	1	8	1	8	1	
Rd Data 8	A	Rd Data 9	A	Rd Data 10	A	…
Sensor Number	0	Entity	0	Entity Instance	0	

	8	1	1
…	PEC	A	P
From zero to five bytes of Event Data	[data dependent]	1	

6.6 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Actually, the application of the PC monitoring would most often be connected to power supply. The CPU V-core voltage, +3.3V and battery voltage can directly connect to these analog inputs. The –5V, –12V and +12V inputs should be reduced a factor with external resistors to meet the input range. As Figure 7 shows.

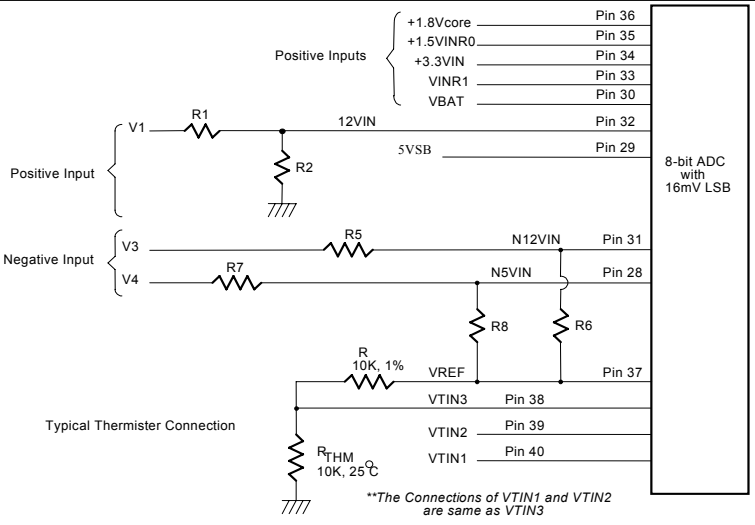


Figure 7.

6.6.1 Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as the following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN should be subject to under 4.096V for the maximum input range of the 8-bit ADC. The pin 13 and pin 29 are discretely connected to the power supply +5V and 5VSB. There are two functions in these pins with 5V. The first function is to supply internal analog power in the W83791D/G and the second one is that these voltages are all connected to internal serial resistors to monitor the +5V and 5VSB voltage.

6.6.2 Monitor negative voltage:

The negative voltage should be connected to two series resistors and a positive voltage VREF (equal to 3.6V). In the Figure 11, the voltage V3 and V4 are two negative voltages and are -12V and -5V respectively. The voltage V3 is connected to two serial resistors as well as another positive terminal VREF. Therefore, the voltage node N12VIN would be a positive voltage if the scale of the two serial resistors are carefully selected. It is recommended from Winbond that the scale of the two serial resistors are R5=232K ohms and R6=56K ohm. The input voltage of node -12VIN can be calculated by the following equation.

$$N12VIN = (VREF + |V_5|) \times (\frac{232K\Omega}{232K\Omega + 56K\Omega}) + V_5$$

where VREF is equal to 3.6V.

If the V_5 is equal to -12V then the voltage is equal to 0.567V and the converted hexdecimal data is set to 35h by the 8-bit ADC with 16mV-LSB.This monitored value should be converted to the real negative voltage and the express equation is shown as follows.

$$V_5 = \frac{N12VIN - VREF \times \beta}{1 - \beta}$$

Where β is 232K/(232K+56K). If the N2VIN is 0.567 then the V5 is approximately equal to -12V.

The other negative voltage input V6 (approximate -5V) can also be evaluated by the similar method and the serial resistors can be R7=120K ohms and R8=56K ohms by the Winbond recommended. The expression equation of V6 With -5V voltage is shown as follows.

$$V_6 = \frac{N5VIN - VREF \times \gamma}{1 - \gamma}$$

Where the γ is set to 120K/ (120K+56K). If the monitored ADC value in the N5VIN channel is 0.8635, VREF=3.6V and the parameter γ is 0.6818, then the negative voltage of V6 can be evaluated -5V.

6.7 FAN Speed Count and FAN Speed Control

6.7.1 Fan speed count

W83791D/G support 5 sets of fan counting. Fan inputs are provided for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and the maximum input voltage should not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to meet the input specification. The normal circuit and trimming circuits are shown as Figure 8.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, if the fan speed counter has been read from register CR [28] or CR [29] or CR [2A] or CR [BA] or CR [BB] , then the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. This provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, RPM, and count.

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	153	6160	9.74 ms
2 (default)	4400	13.64 ms	153	3080	19.48 ms
4	2200	27.27 ms	153	1540	38.96 ms
8	1100	54.54 ms	153	770	77.92 ms
16	550	109.08 ms	153	385	155.84 ms
32	275	218.16 ms	153	192	311.68 ms
64	137	436.32 ms	153	96	623.36 ms
128	68	872.64 ms	153	48	1246.72 ms

Table 2

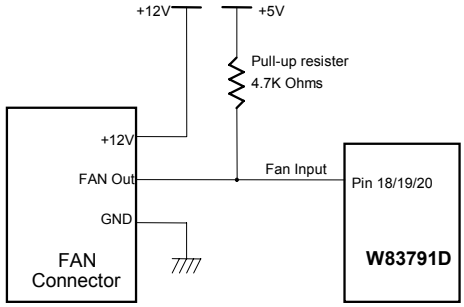


Figure 8-1. Fan with Tach Pull-Up to +5V

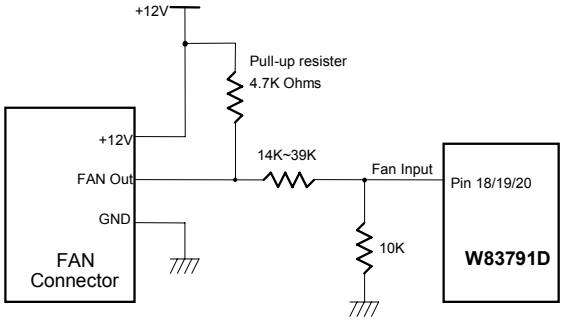


Figure 8-2. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator

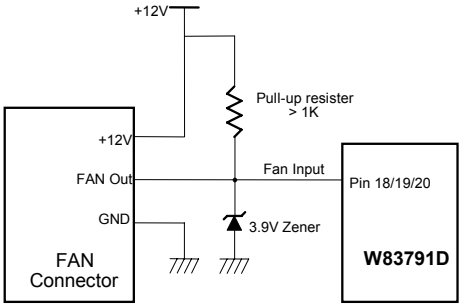


Figure 8-3. Fan with Tach Pull-Up to +12V and Zener Clamp

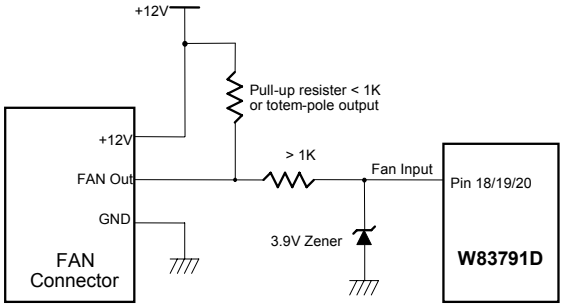


Figure 8-4. Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

6.7.2 Fan speed control

The W83791D/G provides five sets of PWM for fan speed control. The duty cycle of PWM can be programmed by a 8-bit registers defined in the Bank0 CR [81], CR [83], CR [94], CR [9E] and CR [9F]. The default duty cycle is set to 100%, that is, the default 8-bit register is set to 0xFFh. The expression of duty cycle can be represented as follows.

$$\text{Duty}-\text{cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

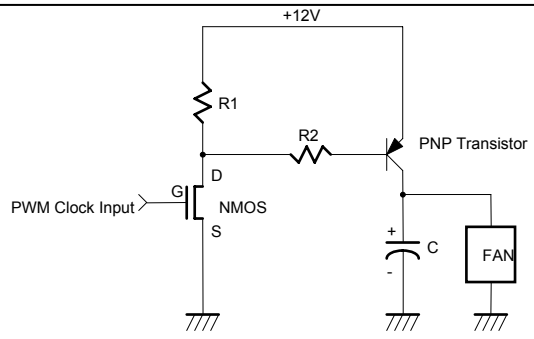


Figure 9.

6.7.3 Smart Fan Control

W83791D/G supports three Smart Fan function and mapping to temp1 (FAN1, PWMOUT1), temp2 (FAN2, PWMOUT2), temp3 (FAN3, PWMOUT3) .Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode.

6.7.3.1. Thermal Cruise mode

At this mode, W83791D/G provides the Smart Fan system to automatically control fan speed to keep the temperatures of CPU and the system within specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS and the fan speed will be lowered as long as the current temperature remains below the setting value. Once the temperature exceeds the high limit (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its full speed but the temperature still exceeds the high limit (ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but still above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target range (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset stop value until the temperature exceeds the low limit.

Figure 10-1, 10-2 gives an illustration of Thermal Cruise Mode.

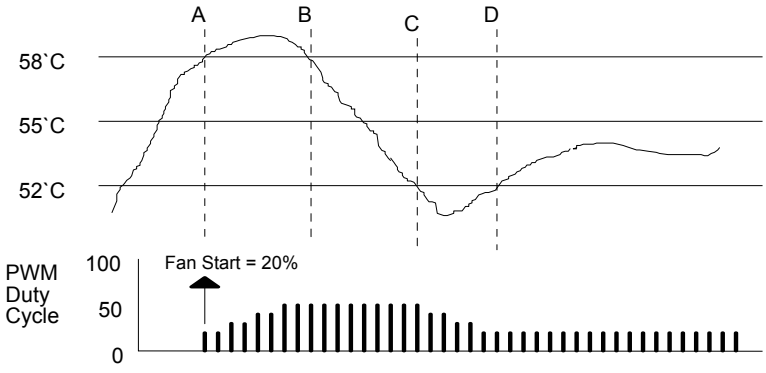


Figure 10-1

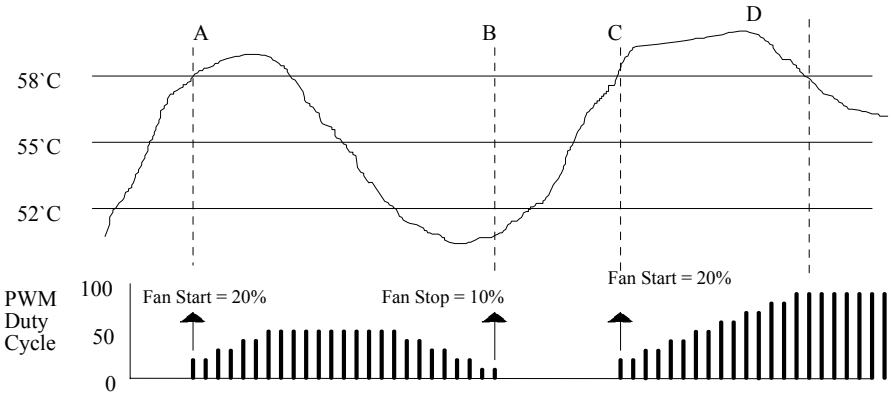


Figure 10-2

6.7.3.2. Fan Speed Cruise mode

At this mode, W83791D/G provides the Smart Fan system to automatically control the fan speed within a specific range. In the beginning, a wanted fan speed count and interval must be set (ex. 160± 10) by BIOS. As long as the fan speed count remains in the specific range, PWM duty cycle will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), PWM duty cycle will be increased to make the count under the high limit. On the other hand, if current fan speed count is less than the low limit (ex. 160-10), PWM duty cycle will be decreased to make the count higher than the low limit. See Figure 10-3 example.

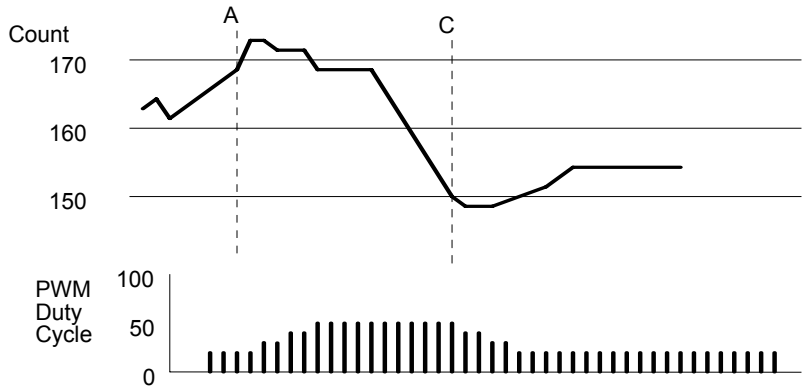


Figure 10-3

Of course, Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

6.8 Temperature Measurement Machine

The temperature data format is 8-bit two-complement for sensor 1 and 9-bit two-complement for sensor 2/3. The 8-bit temperature data can be obtained by reading the CR [27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the bank0 CR [C0/ C8h] and the LSB from the bank0 CR [C1/C9h] bit 7. The format of the temperature data is show in Table 3.

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 3

6.8.1 Monitor temperature from thermistor:

The W83791D/G can connect three thermistors to measure three different environmental temperatures. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 11, the themistor is connected by a serial resistor with 10K Ohms (1% error), then connect to VREF (Pin 37).

6.8.2 Monitor temperature from Pentium IITM thermal diode or bipolar transistor 2N3904

The W83791D/G can alternate the thermistor to Pentium II/III™ thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 11. The pin of Pentium II/III™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin PIITDx in the W83791D/G. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

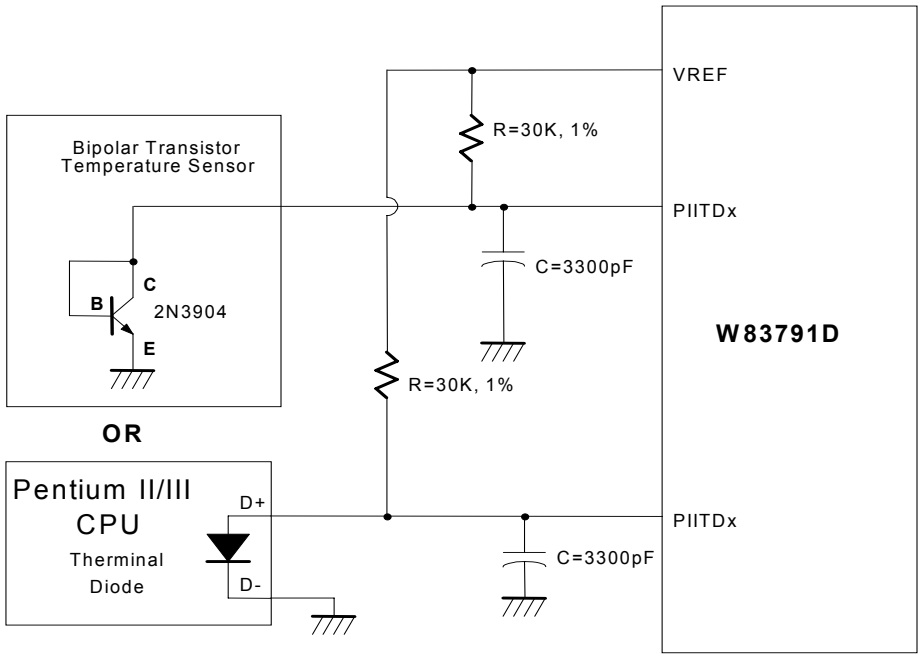


Figure 11.

6.8.3 SMI# interrupt for W83791D Voltage

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 12-1)

6.8.4 SMI# interrupt for W83791D Fan

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit (set at value ram index 3Bh and 3Ch), will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 12-2)

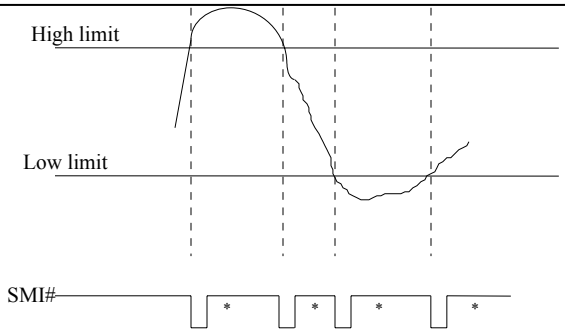
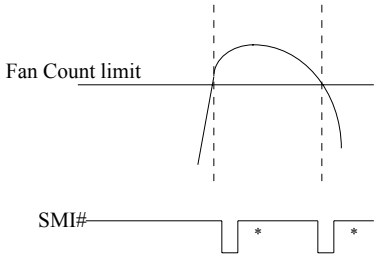


Figure 12-1. Voltage SMI# Mode



*Interrupt Reset when Interrupt Status Registers are read

Figure 12-2. Fan SMI# Mode

6.8.5 SMI# interrupt for W83791D/G temperature sensor 1/2/3

(1) Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O but has not been reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 12-3)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 12-4)

(3) One-Time interrupt mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O. (Figure 12-5)

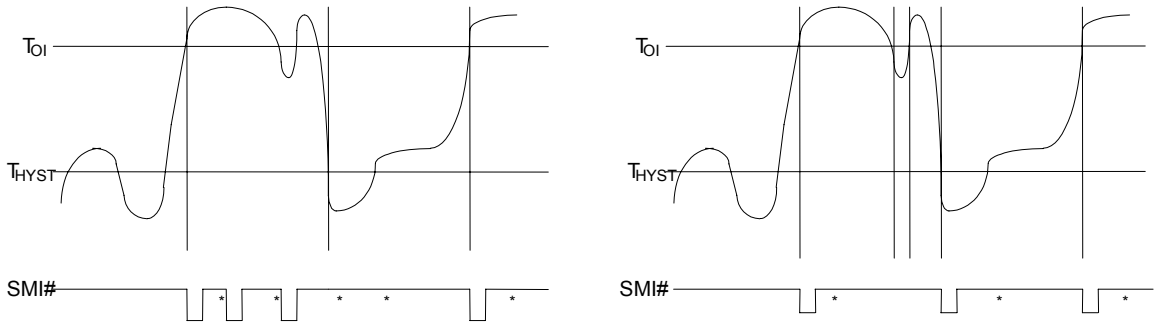


Figure 12-3. Comparator Interrupt Mode

Figure 12-4. Two-Times Interrupt Mode

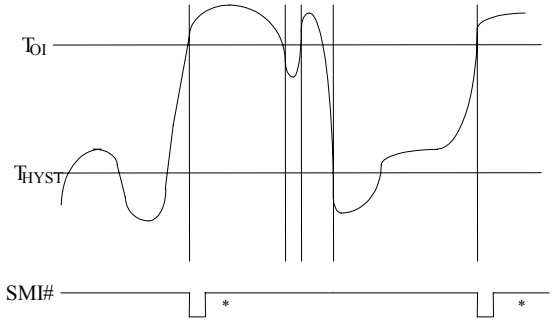


Figure 12-5. One-Time Interrupt Mode

Note. The IRQ interrupt action like SMI#, but the IRQ is level signal.

6.8.6 Over-Temperature (OVT#) for W83791D/G temperature sensor 1/2/3

(1) Comparator Mode:

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 13)

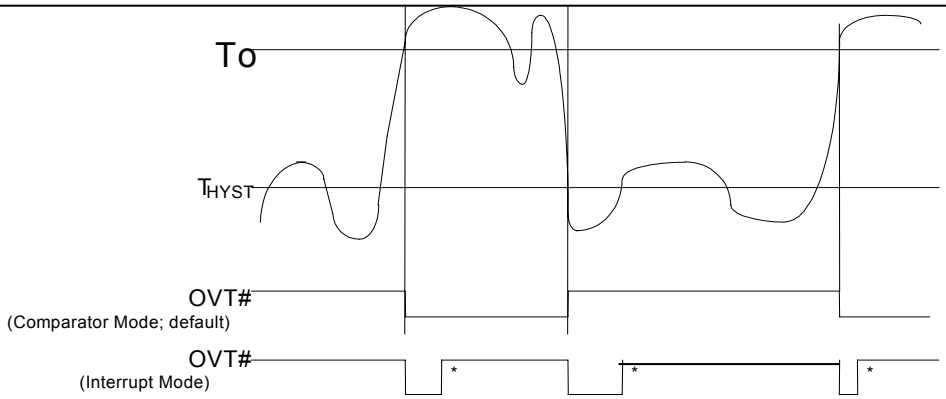
(2) Interrupt Mode:

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor 1 or sensor 2 or sensor 3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor 1 or sensor 2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again. (Figure 13)

(3) ACPI Mode

At this mode, temperature exceeding one level of temperature separation, starting from 0 degree, causes the OVT# output activated. OVT# will be activated again once temperature exceeds the next level. OVT# output will act the same manner when temperature goes down. (Figure 13-1)

The granularity of temperature separation between each OVT# output signal can be programmed at Bank0 CR [4Ch] bit 4-5.



*Interrupt Reset when Temperature 1/2/3 is read

Figure 13 Over-Temperature Response Diagram

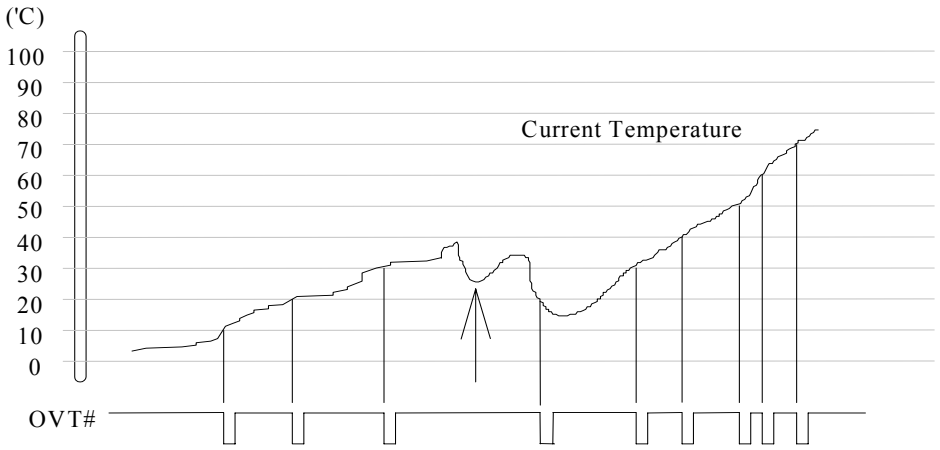


Figure 13-1. ACPI Mode

7. CONTROL AND STATUS REGISTER

7.1 Speech Flash Memory Address Registers — Index 00h-02h (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
00h	SPEECHA 0	R/W	**Speech Flash Address 0.** Set speech flash programming address bits [7:0].
01h	SPEECHA 1	R/W	**Speech Flash Address 1.** Set speech flash programming address bits [15:8].
02h	SPEECHA 2	R/W	**Speech Flash Address 2.** Set speech flash programming address bits [23:16].

7.2 Speech Flash Memory Data Registers — Index 03h-06h (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
03h	SPEECHD0	R/W	**Speech Flash Data 0.** Set speech flash programming data bits [7:0].
04h	SPEECHD1	R/W	**Speech Flash Data 1.** Set speech flash programming data bits [15:8].
05h	SPEECHD2	R/W	**Speech Flash Data 2.** Set speech flash programming data bits [23:16].
06h	SPEECHD3	R/W	**Speech Flash Data 3.** Set speech flash programming data bits [31:24].

7.3 Speech Flash Memory Control Register — Index 07h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PROG_ACTIVE	R/W	**Program Active Command.** If set this bit to 1, the serial flash will be active according the Flash Program Mode. Reading this bit, the bit will return a Serial Flash Busy (SER_BUSY). And this is pulse, if read this bit show “0”
6:4	Reserved		**Reserved.**
3:0	PROGMODE	R/W	**Flash Program Mode**

FLASHCTRL[3:0]	
0000b	No action
0001b	Program mode
0010b	Erase all
0011b	Page code
0100b	Erase 4K bytes
0101b	Erase 16K bytes
0110b	Page code read out
0111b	Read flash data

Program procedure:

1. Set Flash address (3-bytes)
2. Set Flash Data (4-bytes)
3. Set Flash control "Program mode"
4. Set program command active (PROG_ACTIVE)

Erase 4K:

1. Set Flash Address (must be 4K address boundary)
2. Set Flash control register

7.4 Event Trigger Timeout Register — Index 08h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:0	TRIG_TIME	R/W	**Event Trigger Timeout Timer Setting.** When software or firmware write trigger event, that don't write to speech queue until this register is timeout. This unit is Second. Default is 00, that is, the software event doesn't need to wait then write to sound event queue. Note that, this function is controlled by Speech Input Property (Index 0Ah).

7.5 Speech Programmable Trigger Register — Index 09h (Bank 0)

Power on default: 80h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TR_RDY	RO	**Programmable Trigger Register Ready.** If return to 1, the software or firmware can write next event to trigger register. If return to 0, the software or firmware cannot write trigger event to event queue, that is, the timer is not timeout yet.
6:0	TRIG_REG	R/W	**Speech Programmable Trigger Register.** The software or firmware can set these bits to trigger speech sound. The vectors of sound trigger are shown as follows. If the bit of trigger register ready is logic 0, this trigger register will be ignored. Therefore, the bit of the trigger ready should be read before programming this register.

TRIG_REG<6:0>	Speech Sound Vector
00h	Vector 80h (1000_0000b) (=80h+00h)
01h	Vector 81h (1000_0001b) (=80h+01h)
02h	Vector 82h (1000_0010b) (=80h+02h)
:	:
N	Vector (80h+*n*)
:	:
7Eh	Vector FEh (1111_1110b) (=80h+7Eh)
7Fh	Vector FFh (1111_1111b) (=80h+7Fh)

7.6 Speech Input Trigger Property Register — Index 0Ah (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	En_Program	R/W	Enable W83791D to program external serial flash memory and change GPIO pin to Speech mode pin.
6	En_Timeout	WO	**Enable Software/Firmware Trigger Timeout Function.** This bit sets the Event Trigger Timeout Function in Index 08h.
5	Busy	RO	If read this bit return "1" means SPKOUT is in busy.
4:0	EVNTRAP5-1 Polarity	R/W	Write '0' the EVNTRAP5-1 will positive edge trigger. Write '1' will negative edge trigger.Default is '0'.

7.7 Reserved Register — Index 0Bh (Bank 0)

7.8 VID and VCORE voltage Property Register — Index 0Ch (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:1	Reserved		Reserved.
0	VRM_check	Read only	If read 1, the power on VCORE checking will be according to Intel VRM9.x . This bit is powered VSB.

7.9 Speech Flash Memory Read Data Registers — Index 0Dh-0Eh (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
0Dh	SPEECHRD0	RO	**Speech Flash Read Data 0.** Speech flash reading data bits [7:0].
0Eh	SPEECHRD1	RO	**Speech Flash Read Data 1.** Speech flash reading data bits [15:8].

7.10 Reserved Register — Index 0Fh (Bank 0)

7.11 VID Control/Status Register — Index 10h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	EN_VIDOUT	R/W	**Enable VID Output.**
6:5	Reserved		Reserved.
4:0	VID_DATA	R/W	**VID Output Data.** Read this register will return programmed data of VID_DATA.

7.12 Entry Disable VID Output Control Register — Index 11h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:0	Entry_Dis	Write	**Entry Disable VID Output Control.** When write a serial pattern: 5Ah, 73h, B2h, E0h, the VID output control will enable. If write a serial pattern: A5h, 4Ch, D9h, 8Ah, the VID output control will disable.

7.13 VID Output Tolerance/Limit Register — Index 12h (Bank 0)

Power on default: 60h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:5	VID_limit	R/W	VID +/- Tolerance/Limit. Default is 3.
4:0	VID_PIN	Read Only	VID Pin Data Reading.

7.14 GPIO Control Register I — Index 13h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	GPIO7	R/W	**GPIO7 Control Bit.** Set to 1, GPIO7 serves as output. Set to 0, GPIO7 serves as input. Default is input.
6	GPIO6	R/W	**GPIO6 Control Bit.** Set to 1, GPIO6 serves as output. Set to 0, GPIO6 serves as input. Default is input.
5	GPIO5	R/W	**GPIO5 Control Bit.** Set to 1, GPIO5 serves as output. Set to 0, GPIO5 serves as input. Default is input.
4	GPIO4	R/W	**GPIO4 Control Bit.** Set to 1, GPIO4 serves as output. Set to 0, GPIO4 serves as input. Default is input.
3	GPIO3	R/W	**GPIO3 Control Bit.** Set to 1, GPIO3 serves as output. Set to 0, GPIO3 serves as input. Default is input.
2	GPIO2	R/W	**GPIO2 Control Bit.** Set to 1, GPIO2 serves as output. Set to 0, GPIO2 serves as input. Default is input.
1	GPIO1	R/W	**GPIO1 Control Bit.** Set to 1, GPIO1 serves as output. Set to 0, GPIO1 serves as input. Default is input.
0	GPIO0	R/W	**GPIO0 Control Bit.** Set to 1, GPIO0 serves as output. Set to 0, GPIO0 serves as input. Default is input.

7.15 GPIO Data/Status Register I — Index 14h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	GPIO7	R/W	**GPIO7 Data/Status Register.** Write this bit, the data will response to GPIO7, set to output mode. If read this register, will return this pin data that can input or output in this pin.
6	GPIO6	R/W	**GPIO6 Data/Status Register.** Write this bit, the data will response to GPIO6, set to output mode. If read this register, will return this pin data that can input or output in this pin.
5	GPIO5	R/W	**GPIO5 Data/Status Register.** Write this bit, the data will response to GPIO5, set to output mode. If read this register, will return this pin data that can input or output in this pin.
4	GPIO4	R/W	**GPIO4 Data/Status Register.** Write this bit, the data will response to GPIO4, set to output mode. If read this register, will return this pin data that can input or output in this pin.
3	GPIO3	R/W	**GPIO3 Data/Status Register.** Write this bit, the data will response to GPIO3, set to output mode. If read this register, will return this pin data that can input or output in this pin.
2	GPIO2	R/W	**GPIO2 Data/Status Register.** Write this bit, the data will response to GPIO2, set to output mode. If read this register, will return this pin data that can input or output in this pin.
1	GPIO1	R/W	**GPIO1 Data/Status Register.** Write this bit, the data will response to GPIO1, set to output mode. If read this register, will return this pin data that can input or output in this pin.
0	GPIO0	R/W	**GPIO0 Data/Status Register.** Write this bit, the data will response to GPIO0, set to output mode. If read this register, will return this pin data that can input or output in this pin.

7.16 GPIO Control Register II — Index 15h (Bank 0)

Power on default: 10h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	EN_GPIO10	R/W	Set to 1, pin 43 will serve as a general purpose I/O, GPIO10 is stand along with other GPIO pin.
6	Reserved		Reserved.
5	VID_Protect	R/W	Write '1' means programmed VID output value as you wish. Default is '0'. **Note: Programmed VID must be carefully, it may cause CPU damaged.**
4	SEL_GPIO	R/W	Set to 0, FAN4/5, PWM4/5 pin switch to GPIO6-GPIO9. Set to 1 is FAN4/5 and PWM4/5. Default is 1.

GPIO Control Register II — Index 15h (Bank 0) , continued .

BIT	NAME	ATTRIBUTE	DESCRIPTION
3	GPIO11	R/W	**GPIO11 Output Control Bit.** Set to 1, GPIO11 serves as output. Set to 0, GPIO11 serves as input. Default is input.
2	GPIO10	R/W	**GPIO10 Output Control Bit.** Set to 1, GPIO10 serves as output. Set to 0, GPIO10 serves as input. Default is input.
1	GPIO9	R/W	**GPIO9 Output Control Bit.** Set to 1, GPIO9 serves as output. Set to 0, GPIO9 serves as input. Default is input.
0	GPIO8	R/W	**GPIO8 Output Control Bit.** Set to 1, GPIO8 serves as output. Set to 0, GPIO8 serves as input. Default is input.

7.17 GPIO Output Data and Status Register II — Index 16h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:4	Reserved		Reserved.
3	GPIO11	R/W	**GPIO11 Data/Status Register.** Write this bit, the data will response to GPIO11, set to output mode. If read this register, will return this pin data that can input or output in this pin.
2	GPIO10	R/W	**GPIO10 Data/Status Register.** Write this bit, the data will response to GPIO10, set to output mode. If read this register, will return this pin data that can input or output in this pin.
1	GPIO9	R/W	**GPIO9 Data/Status Register.** Write this bit, the data will response to GPIO9, set to output mode. If read this register, will return this pin data that can input or output in this pin.
0	GPIO8	R/W	**GPIO8 Data/Status Register.** Write this bit, the data will response to GPIO8, set to output mode. If read this register, will return this pin data that can input or output in this pin.

7.18 LED Control Register — Index 17h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	LED_SEL	R/W	This bit sets to 1, the LED function will be active on the pin 9 (SPEAKER/LED). Set to 0 (default), select SPEAKER output function.
6:3	Reserved		Reserved.

LED Control Register — Index 17h (Bank 0) , continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
2:0	LED_CLK	R/W	**LED Flashed Time Control.**

LED_CLK	Description
000b	LED off. Always drive logical low in LED pin. (Default)
001b	4 Hz, 4 times for 1 second.
010b	2 Hz, 2 times for 1 second.
011b	1 Hz, 1 times for 1 second.
100b	1/2 Hz, 1 time for 2 seconds.
101b	1/4 Hz, 1 time for 4 seconds.
110b	1/8 Hz, 1 time for 8 seconds.
111b	LED on. Always drive logical high in LED pin if LED function is active.

7.19 User Defined Registers — Index 18h-1Ch (Bank 0)

User defined registers. Write a data to the mapped register will return a prior written data when read this mapped register.

7.20 Speech Control Register 1 — Index 1Dh (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	EN_FAN2_SPK	R/W	Enable SPEECH output from FAN 2 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
6	EN_FAN1_SPK	R/W	Enable SPEECH output from FAN 1 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
5	EN_T2_SPK	R/W	Enable SPEECH output from Temperature Sensor 2 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
4	EN_T1_SPK	R/W	Enable SPEECH output from Temperature Sensor 1 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
3	EN_V5_SPK	R/W	Enable SPEECH output from VDD (5V) if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
2	EN_V33_SPK	R/W	Enable SPEECH output from 3.3V if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
1	EN_T3_SPK	R/W	Enable SPEECH output from Temperature Sensor 3 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
0	EN_V25A_SPK	R/W	Enable SPEECH output from Vcore if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.

7.21 Speech Control Register 2 — Index 1Eh (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved	Reserved	Reserved
6	EN_VR1_SPK	R/W	Enable SPEECH output from VINR1 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
5	EN_VR0_SPK	R/W	Enable SPEECH output from VINR0 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
4	EN_CASO_SPK	R/W	Enable SPEECH output from case open if the signal has gone high. Write 1, enable SPEECH output. Default 0.
3	EN_FAN3_SPK	R/W	Enable SPEECH output from FAN 3 if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
2	EN_NV5_SPK	R/W	Enable SPEECH output from -5V if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
1	EN_NV12_SPK	R/W	Enable SPEECH output from -12V if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
0	EN_V12_SPK	R/W	Enable SPEECH output from +12V if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.

7.22 Speech Control Register 3 — Index 1Fh (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Dis_SLOC_SPK	R/W	Disable SPEECH output from SLOTOCC# if the CPU is absent. Write 1, disable SPEECH output. Default 0.
6	Dis_ET5_SPK	R/W	Disable SPEECH output from EVNTRP5 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
5	Dis_ET4_SPK	R/W	Disable SPEECH output from EVNTRP4 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
4	Dis_ET3_SPK	R/W	Disable SPEECH output from EVNTRP3 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
3	Dis_ET2_SPK	R/W	Disable SPEECH output from EVNTRP2 if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
2	Dis_ET1_SPK	R/W	Disable SPEECH output from EVNTRP1if a transition occurs at pin. Write 1, disable SPEECH output. Default 0.
1	EN_VSB_SPK	R/W	Enable SPEECH output from VSB if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.
0	EN_VBAT _SPK	R/W	Enable SPEECH output from VBAT if the monitor value exceeds the limit value. Write 1, enable SPEECH output. Default 0.

7.23 Value RAM — Index 20h- 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
20h	VCOREA reading
21h	VINR0 reading
22h	+3.3VIN reading
23h	VDD 5V reading
24h	+12VIN reading
25h	-12VIN reading
26h	-5VIN reading
27h	Temperature reading
28h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	FAN3 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Bh	VCOREA High Limit, default value is defined by Vcore Voltage +0.2v.
2Ch	VCOREA Low Limit, default value is defined by Vcore Voltage -0.2v.
2Dh	VINR0 High Limit.
2Eh	VINR0 Low Limit.
2Fh	+3.3VIN High Limit
30h	+3.3VIN Low Limit
31h	VDD 5V High Limit
32h	VDD 5V Low Limit
33h	+12VIN High Limit
34h	+12VIN Low Limit
35h	-12VIN High Limit
36h	-12VIN Low Limit
37h	-5VIN High Limit
38h	-5VIN Low Limit
39h	Temperature sensor 1 (VTIN1) High Limit
3Ah	Temperature sensor 1 (VTIN1) Hysteresis Limit

Value RAM — Index 20h- 3Fh (Bank 0), continued.

ADDRESS A6-A0	DESCRIPTION
3Bh	FAN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	FAN2 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	FAN3 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3E- 3Fh	Reserved

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupts will never be generated except the case when voltages go below the low limits.

7.24 Configuration Register — Index 40h (Bank 0)

Power on default <7:0> = 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Initialization	R/W	Set one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.
6	IRQ output	R/W	Set 0, IRQ output level signal. Set 1, output pulse signal. Default is 0, but when set the IRQ as pulse output, it become to low pulse.
5	IRQ Polarity	R/W	When set to 0, IRQ active high. Set to 1, IRQ active low. Default is 0.
4	Reserved		Reserved
3	INT_Clear	R/W	A one disables the SMI# and IRQ# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit. Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.
2	EN_IRQ	R/W	A one enables the IRQ Interrupt output.
1	EN_SMI#	R/W	A one enables the SMI# Interrupt output.
0	START	R/W	A one enables startup of monitoring operations; a zero puts the part in standby mode. **Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

7.25 Interrupt Status Register 1 — Index 41h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN2	Read Only	A one indicates the fan count limit of FAN2 has been exceeded.
6	FAN1	Read Only	A one indicates the fan count limit of FAN1 has been exceeded.
5	TEMP2	Read Only	A one indicates a high limit of VTIN2 has been exceeded from temperature sensor 2.
4	TEMP1	Read Only	A one indicates a high limit of VTIN1 has been exceeded from temperature sensor 1.
3	5VDD	Read Only	A one indicates a high or low limit of power 5VDD has been exceeded.
2	+3.3VIN	Read Only	A one indicates a high or low limit of +3.3VIN has been exceeded.
1	VINR0	Read Only	A one indicates a high or low limit of VINR0 has been exceeded.
0	Vcore	Read Only	A one indicates a high or low limit of Vcore has been exceeded.

7.26 Interrupt Status Register 2 — Index 42h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved
6	VINR1	Read Only	A one indicates a high or low limit of VINR1 (pin33) has been exceeded.
5	TEMP3	Read Only	A one indicates a high or low limit of VTIN3 has been exceeded from temperature sensor 3.
4	Chassis Intrusion	Read Only	A one indicates Chassis Intrusion has gone high.
3	FAN3	Read Only	A one indicates the fan count limit of FAN3 has been exceeded.
2	-5VIN	Read Only	A one indicates a high or low limit of -5VIN has been exceeded.
1	-12VIN	Read Only	A one indicates a high or low limit of -12VIN has been exceeded.
0	+12VIN	Read Only	A one indicates a high or low limit of +12VIN has been exceeded.

Note: Interrupt status register III is defined at index 9Bh

7.27 SMI# Mask Register 1 — Index 43h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN2	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt
6	FAN1	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
5	TEMP2	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
4	TEMP1	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
3	5VDD	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
2	+3.3VIN	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
1	VINR0	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
0	Vcore	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.

7.28 SMI# Mask Register 2 — Index 44h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved
6	VINR1	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
5	TEMP3	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
4	Chassis Intrusion	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
3	FAN3	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
2	-5VIN	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
1	-12VIN	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
0	+12VIN	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.

Note: SMI# Mask register III is defined at index 9Ch

7.29 IRQ Mask Register 1 — Index 45h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN2	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
6	FAN1	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
5	TEMP2	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
4	TEMP1	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
3	5VDD	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
2	+3.3VIN	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
1	VINR0	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
0	Vcore	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.

7.30 IRQ Mask Register 2 — Index 46h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Chassis clear	R/W	A one outputs a minimum 20 ms active low pulse on the Case Open pin. The register bit self clears after the pulse has been output.
6	VINR1	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
5	TEMP3	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
4	Chassis Intrusion	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
3	FAN3	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
2	-5VIN	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
1	-12VIN	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
0	+12VIN	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.

Note: IRQ mask register III is defined at index 9Dh

7.31 VID/Fan Divisor Register — Index 47h (Bank 0)

Power on default: 0101_xxxx

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	FAN2_DIV	R/W	FAN2 Speed Divisor. The third bit of FAN 2 divisor is defined in Index 5Dh. <7:6> = 00 - divide by 1; <7:6> = 01 - divide by 2 (Default); <7:6> = 10 - divide by 4; <7:6> = 11 - divide by 8.
5-4	FAN1_DIV	R/W	FAN1 Speed Control. The third bit of FAN 1 divisor is defined in Index 5Dh. <5:4> = 00 - divide by 1; <5:4> = 01 - divide by 2 (Default); <5:4> = 10 - divide by 4; <5:4> = 11 - divide by 8.
3-0	VID <3:0>	Read only	The VID <3:0> inputs, which is latched when VDD 5V power good.

Note: Please refer to Bank0 Index 5Dh, Fan divisor table.

7.32 Serial Bus Address Register — Index 48h (Bank 0)

Power on default: 0010_11xx.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6-0	SMBADDR1	R/W	Serial Bus Address <7:1> for general index registers. The address bit 0 and bit 1 are trapped by the pin 10 and pin 11, respectively.

7.33 Voltage ID (VID4) & Device ID — Index 49h (Bank 0)

Power on default: 0001_000x

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-1	DID<6:0>	Read only	Device ID<6:0>, W83791D/G version ID that differentiates chip serial product number. This default value is 0010000b, that means is 1.0.
0	VID4	Read only	The VID4 input, which is latched when VDD 5V power good.

7.34 Temperature 2 and Temperature 3 Serial Bus Address Register — Index4Ah (Bank 0)

Power on default: 01h; Reset by MR

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	DIS_T3	R/W	Set to 1, disable temperature 3 sensor and can not access any data from Temperature Sensor 3.
6-4	I2CADDR3	R/W	Temperature 3 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.
3	DIS_T2	R/W	Set to 1, disable temperature Sensor and cannot access any data from Temperature Sensor 2.
2-0	I2CADDR2	R/W	Temperature 2 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.

7.35 Pin Control Register — Index4Bh (Bank 0)

Power on default: 44h, Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	FAN3_DIV	R/W	FAN3 Speed Divisor. The third bit of FAN 3 speed divisor is defined in Index 5Dh. <7:6> = 00 - divide by 1; <7:6> = 01 - divide by 2; <7:6> = 10 - divide by 4; <7:6> = 11 - divide by 8;
5-4	ADCOVSEL	R/W	Select A/D Converter Clock Input. <5:4> = 00 - default. ADC clock select 22.5 Khz. <5:4> = 01- ADC clock select 5.6 Khz. (22.5K/4) <5:4> = 10 - ADC clock select 1.4Khz. (22.5K/16) <5:4> = 11 - ADC clock select 0.35 Khz. (22.5K/64)
3-0	Reserved		Reserved

7.36 SMI#/OVT# Property Select — Index 4Ch (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	TEMP_SMI_MD [1:0]	R/W	**Temperature SMI# Mode Select.** <00> - **Comparator Interrupt Mode:** Temperature 1/2/3 exceeds T_O (Over-temperature) limit causes and interrupt and this interrupt will be reset by reading all the Interrupt Staus. <01> - **Two Time Interrupt Mode:**(Default) This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis type. Temperature exceeding T_O, causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}. <10> **- One Time Interrupt Mode:** This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis type. Temperature exceeding T_O (Over-temperature, defined in Bank 1/2) causes an interrupt and then temperature going below T_{HYST} (Hysteresis temperature, defined in Bank 1/2) will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, and interrupt will not occur again until the temperature exceeding T_O.
5-4	OVT_MD[1:0]	R/W	**OVT# Mode Select.** There are three OVT# signal output type. <00> - **Comparator Mode:** (Default) Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. <01> - **Interrupt Mode:** Setting temperature exceeding T_O causes the OVT# output activated indefinitely until reset reading temperature sensor 1/2/3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor 1/2/3. Once the OVT# will not be activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again. <10> - **ACPI Mode:** If set to 1 then enable ACPI OVT# output. Which always send an OVT# signal when the temperature over the ACPI temperature increment value defined at Index 5Eh.
3	EN_OVT3	R/W	Enable temperature sensor 3 over-temperature (OVT) output if set to 1. Default is 0, disable OVT2 output through pin OVT#. The pin OVT# is wire OR with OVT1 and OVT2.

SMI#/OVT# Property Select — Index 4Ch (Bank 0), continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
2	EN_OVT2	R/W	Enable temperature sensor 2 over-temperature (OVT) output if set to 1. Default is 0, disable OVT2 output through pin OVT#. The pin OVT# is wire OR with OVT1 and OVT3.
1	EN_OVT1	R/W	Enable temperature sensor 1 over-temperature (OVT) output .if set to 1. Default is 0, disable OVT1 output through pin OVT#. The pin OVT# is wire OR with OVT2 and OVT3.
0	OVTPOL	R/W	**Over-Temperature Polarity.** Write 0, OVT# active high. Write 1, OVT# active low. Default is 1.

7.37 FAN 1- 3 IN/OUT and BEEP Control Register — Index 4Dh (Bank 0)

Power on default [7:0]: 0001_0101; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	DIS_ABN	R/W	Disable power-on abnormal the monitor voltage including Vcore, and +3.3V. If these voltages exceed the limit value, the pin of BEEP (Open Drain) will drives 300Hz and 600Hz frequency signal. Write 1, the frequency will be disable. Default 0. After power on, the system should set 1 to this bit to 1 in order to disable BEEP.
6	Reserved		Reserved.
5	FANOPV3	R/W	FAN 3 output value if FANINC3 sets to 0. Write 1, then pin 18 always generates logic high signal. Write 0, pin18 always generates logic low signal. This bit is 0.
4	FANINC3	R/W	FAN3 Input Control. Set to 1, pin 18 acts as FAN clock input, which is default value. Set to 0, this pin 18 acts as FAN control signal and the output value of FAN control is set by this register bit 5. This output pin can connect to power PMOS gate to control FAN ON/OFF.
3	FANOPV2	R/W	FAN 2 output value if FANINC2 sets to 0. Write 1, then pin 19 always generates logic high signal. Write 0, pin 19 always generates logic low signal. This bit is 0.
2	FANINC2	R/W	FAN2 Input Control. Set to 1, pin 19 acts as FAN clock input, which is default value. Set to 0, this pin 19 acts as FAN control signal and the output value of FAN control is set by this register bit 3. This output pin can connect to power NMOS gate to control FAN ON/OFF.
1	FANOPV1	R/W	FAN 1 output value if FANINC1 sets to 0. Write 1, then pin 20 always generates logic high signal. Write 0, pin20 always generates logic low signal. This bit is 0.
0	FANINC1	R/W	FAN1 Input Control. Set to 1, pin 20 acts as FAN clock input, which is default value. Set to 0, this pin 20 acts as FAN control signal and the output value of FAN control is set by this register bit 1. This output pin can connect to power PMOS gate to control FAN ON/OFF.

7.38 Bank Select — Index 4Eh (Bank 0)

Power on default [7:0] 1000_0000b; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	HBACS	R/W	High byte access. Set to 1, access Register 4Fh high byte register. Set to 0, access Register 4Fh low byte register. Default 1.
6:3	Reserved		Reserved
2:0	BANKSEL	R/W	Set the three bit to <001> means select to Bank1.

7.39 Winbond Vendor ID — Index 4Fh (Bank 0)

Power on default: A3h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7:0	Vendor ID	Read Only	Vendor ID low byte if CR4E.bit7=0. Default A3h. Vendor ID high byte if CR4E.bit7=1. Default 5Ch.

7.40 Winbond Test Register — Index 50h - 55h (Bank 0)

These Registers is reserved for Winbond test only. Users do not use these registers.

7.41 BEEP Control Register 1 — Index 56h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	EN_FAN2_BP	R/W	Enable BEEP output from FAN 2 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
6	EN_FAN1_BP	R/W	Enable BEEP output from FAN 1 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
5	EN_T2_BP	R/W	Enable BEEP output from Temperature Sensor 2 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
4	EN_T1_BP	R/W	Enable BEEP output from Temperature Sensor 1 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
3	EN_V5_BP	R/W	Enable BEEP output from VDD (5V) if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
2	EN_V33_BP	R/W	Enable BEEP output from 3.3V if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
1	EN_T3_BP	R/W	Enable BEEP output from Temperature Sensor 3 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
0	EN_V25A_BP	R/W	Enable BEEP output from Vcore if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.

7.42 BEEP Control Register 2 — Index 57h (Bank 0)

Power on default: 80h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	EN_GBP	R/W	Enable Global BEEP. Write 1, enable global BEEP output. Default 1. Write 0, disable all BEEP output.
6	EN_VR1_BP	R/W	Enable BEEP output from VINR1 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
5	EN_VR0_BP	R/W	Enable BEEP output from VINR0 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
4	EN_CASO_BP	R/W	Enable BEEP output from case open if the signal has gone high. Write 1, enable BEEP output. Default 0.
3	EN_FAN3_BP	R/W	Enable BEEP output from FAN 3 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
2	EN_NV5_BP	R/W	Enable BEEP output from -5V if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
1	EN_NV12_BP	R/W	Enable BEEP output from -12V if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.
0	EN_V12_BP	R/W	Enable BEEP output from +12V if the monitor value exceeds the limit value. Write 1, enable BEEP output. Default 0.

7.43 Chip ID — Index 58h (Bank 0)

Power on default: 71h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	CHIPID	Read Only	Winbond Chip ID. Read this register will return 71h.

7.44 Diode Selection Register — Index 59h (Bank 0)

Power on default: 70h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6	SELPIIV3	R/W	Temperature sensor diode 3. When set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode
5	SELPIIV2	R/W	Temperature sensor diode 2. When set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode

Diode Selection Register — Index 59h (Bank 0) , continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
4	SELPIIV1	R/W	Temperature sensor diode 1. When set to 1, select Pentium II compatible Diode. Set to 0 to select 2N3904 Bipolar mode
3-0	Reserved		Reserved

7.45 Reserved — Index 5Ah - (Bank 0)

7.46 FANIN 4/5 Control — Index 5Bh (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FANINC5	R/W	FAN5 Input Control. Set to 1, pin 47 acts as FAN clock input. Set to 0, this pin 47 acts as FAN control signal, which is **default** value. This output pin can connect to power PMOS gate to control FAN ON/OFF.
6	FANINC4	R/W	FAN4 Input Control. Set to 1, pin 46 acts as FAN clock input. Set to 0, this pin 46 acts as FAN control signal, which is **default** value. This output pin can connect to power PMOS gate to control FAN ON/OFF.
5:0	Reserved		Reserved

7.47 FAN 4/5 Divisor Control — Index 5Ch (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN5_OB	R/W	**Enable Fan 5 as Output Buffer.** Set to 1, FANPWM5 can drive logical high or logical low.
6:4	FAN_DIV5	R/W	**FAN5 Speed Divisor**. <6:4> = 000 - divide by 1(Default); <6:4> = 001 - divide by 2; <6:4> = 010 - divide by 4; <6:4> = 011 - divide by 8. <6:4> = 100 - divide by 16. <6:4> = 101 - divide by 32. <6:4> = 110 - divide by 64 <6:4> = 111 - divide by 128.
3	FAN4_OB	R/W	**Enable Fan 4 as Output Buffer.** Set to 1, FANPWM4 can drive logical high or logical low.

FAN 4/5 Divisor Control — Index 5Ch (Bank 0) , continued

BIT	NAME	ATTRIBUTE	DESCRIPTION
2:0	FAN_DIV4	R/W	**FAN4 Speed Divisor**. <2:0> = 000 - divide by 1(Default); <2:0> = 001 - divide by 2; <2:0> = 010 - divide by 4; <2:0> = 011 - divide by 8. <2:0> = 100 - divide by 16. <2:0> = 101 - divide by 32. <2:0> = 110 - divide by 64 <2:0> = 111 - divide by 128.

7.48 VBAT Monitor Control Register — Index 5Dh (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN DIV3_B2	R/W	FAN 3 divisor Bit 2. The bit 1-0 is defined in the Index 4Bh.
6	FANDIV2_B2	R/W	FAN 2 divisor Bit 2. The bit 1-0 is defined in the Index 47h.
5	FANDIV1_B2	R/W	FAN 1 divisor Bit 2. The bit 1-0 is defined in the Index 47h.
4	EN_ALARM_RSP	R/W	Enable Alarm Response if set to 1.
3	BJTS3	R/W	Temperature Sensor 3 type selection. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.
2	BJTS2	R/W	Temperature Sensor 2 type selection.Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.
1	BJTS1	R/W	Temperature sensor 1 type selection. Set to 1, select bipolar sensor. Set to 0, select thermistor sensor.
0	EN_VBAT_MNT	R/W	Write 1, enable battery voltage monitor. Write 0, disable battery voltage monitor. If enable this bit, the monitor value is value after one monitor cycle. Note that the monitor cycle time is at least 300 ms for W83791D/G.

7.49 ACPI Temperature Increment Register — Index 5Eh

Power on default: 05h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6-0	DIFFREG[6:0]	R/W	**ACPI Temperature Increment Register.** If set to this register to non-zero value, the OVT# signal will be activated at pointer of the temperature of times of DIFFREG (i.e. DIFFREG*n, where n is non-zero integer). The default value is 5 degree C.

7.50 Reserved — Index 5Fh (Bank 0)

7.51 FAN 1 Pre-Scale Register — Index 80h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM_CLK_SEL1	R/W	**PWM 1 Input Clock Select.** This bit select Fan 1 input clock to pre-scale divider. 0: 3MHz 1: 125 KHz
6-0	PRE_SCALE1[6:0]	R/W	**Fan 1 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM frequency = (Input clock / pre-scale) / 256

7.52 FAN 1 Duty Cycle Select Register — 81h (Bank 0)

Power on default: FFh

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	F1_DC[7:0]	R/W	**Fan 1 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan 1 control mode, read this register will return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX/256*100%) during one cycle.

7.53 FAN 2 Pre-Scale Register — Index 82h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM_CLK_SEL2	R/W	**PWM 2 Input Clock Select.** This bit select Fan 2 input clock to pre-scale divider. 0: 3 MHz 1: 125 KHz
6-0	PRE_SCALE2[6:0]	R/W	**Fan 2 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM frequency = (Input clock / pre-scale) / 256

7.54 FAN2 Duty Cycle Select Register — Index 83h (Bank 0)

Power on default: FFh

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	F2_DC[7:0]	R/W	**Fan 2 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan 2 control mode, read this register will return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is XX/256*100% during one cycle.

7.55 FAN 1/2 Configuration Register — Index 84h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	Reserved		Reserved
5-4	FAN2_TYPE	R/W	**FAN 2 PWM Control Type**. 00 - Manual PWM Control Mode. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.

FAN 1/2 Configuration Register — Index 84h (Bank 0), continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
3-2	FAN1_TYPE	R/W	**FAN 1 PWM Control Type**. 00 - Manual PWM Control, which is automatic PWM. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.
1	FAN2_OB	R/W	**Enable Fan 2 as Output Buffer.** Set to 1, FANPWM2 can drive logical high or logical low. Default Pin 11 (PWMOUT2) is open-drain.
0	FAN1_OB	R/W	**Enable Fan 1 as Output Buffer.** Set to 1, FANPWM1 can drive logical high or logical low. Default Pin 10 (PWMOUT1) is open-drain.

7.56 Fan 1 Target Temperature Register/Target Fan 1 Speed Control Register — Index 85h (Bank 0)

Power on default: 00h

VTIN1 target temperature register for Thermal Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6-0	FAN_TAR_T1[6:0]	R/W	**Fan 1 Target Temperature.** Only for Thermal Cruise mode. When the temperature 1 over the target temperature add tolerance temperature, the smart fan 1 duty cycle will up count until the duty cycle obtain to FFh.

Fan 1 target speed register for Fan Speed Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	FAN_TAR_CNT1 [7:0]	R/W	**Target Fan 1 Speed Control.** Only for Fan Speed Cruise Mode. When the fan 1 monitored Fan 1 Count over the target Fan Count add tolerance, the fan duty cycle will up/down count until the duty cycle have been corresponding the monitored speed count.

7.57 Fan 2 Target Temperature Register/Target Fan 2 Speed Control Register — Index 86h (Bank 0)

Power on default: 00h

VTIN2 target temperature register for Thermal Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved	R/W	Reserved.
6-0	FAN_TAR_T2 [6:0]	R/W	**Fan 2 Target Temperature.** Only for Thermal Cruise mode. When the temperature 2 over the target temperature add tolerance temperature, the smart fan 2 duty cycle will up count until the duty cycle obtain to FFh.

Fan 2 target speed register for Fan Speed Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	FAN_TAR_CNT2 [7:0]	R/W	**Target Fan 2 Speed Control.** Only for Fan Speed Cruise Mode. When the fan 2 monitored Fan 2 Count over the target Fan Count add tolerance, the fan duty cycle will up/down count until the duty cycle have been corresponding the monitored speed count.

7.58 Tolerance of Fan1/2 Target Temperature or Speed Register — Index 87h (Bank0)

Power on default: 00h

Tolerance of VTIN1/2 target temperature register.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-4	TOL_T2[3:0]	R/W	Tolerance of Fan 2 Target Temperature. Only for Thermal Cruise mode.
3-0	TOL_T1[3:0]	R/W	Tolerance of Fan 1 Target Temperature. Only for Thermal Cruise mode.

Tolerance of Fan 1/2 target speed register.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-4	TOL_FS2[3:0]	R/W	**Tolerance of Fan 2 Target Speed Count.** Only for Fan Speed Cruise mode.
3-0	TOL_FS1[3:0]	R/W	**Tolerance of Fan 1 Target Speed Count.** Only for Fan Speed Cruise mode.

7.59 Fan 1 PWM Stop Duty Cycle Register — Index 88h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_DC1[7:0]	R/W	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this value. This register should be written a non-zero minimum PWM stop duty cycle.

7.60 Fan 2 PWM Stop Duty Cycle Register — 89h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_DC2[7:0]	R/W	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this value. This register should be written a non-zero minimum PWM stop duty cycle.

7.61 Fan 1 Start-up Duty Cycle Register — Index 8Ah (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	START_DC1[7:0]	R/W	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

7.62 Fan 2 Start-up Duty Cycle Register — Index 8Bh (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	START_DC2[7:0]	R/W	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

7.63 Fan 1 Stop Time Register — Index 8Ch (Bank 0)

Power on default: 3Ch

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_TIME1[7:0]	R/W	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

7.64 Fan 2 Stop Time Register — Index 8Dh (Bank 0)

Power on default: 3Ch

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_TIME2 [7:0]	R/W	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

7.65 Fan 1/2/3 Step Down Time Register — Index 8Eh (Bank 0)

Power on default: 0Ah

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STEP_DOWN_T[7:0]	R/W	The time interval, which is 0.1 second unit, to decrease PWM duty in Thermal Cruise mode.

7.66 Fan 1/2/3 Step Up Time Register — Index 8Fh (Bank 0)

Power on default: 0Ah

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STEP_UP_T[7:0]	R/W	The time interval, which is 0.1 second unit, to increase PWM duty in Thermal Cruise mode.

7.67 Temperature Sensor 1 (VTIN1) Offset Register — Index 90h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	Reserved		Reserved.
5-0	OFFSET1[5:0]	R/W	Temperature 1 (VTIN1) base temperature. The temperature is added by both monitor value and offset value. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree

7.68 Temperature Sensor 2 (VTIN2) Offset Register — Index 91h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	Reserved	R/W	Reserved.
5-0	OFFSET2[5:0]	R/W	Temperature2 (VTIN2) base temperature. The temperature is added by both monitor value and offset value. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree

7.69 Temperature Sensor 3 (VTIN3) Offset Register — Index 92h (Bank 0)

Power-on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	Reserved	R/W	Reserved.
5-0	OFFSET3[5:0]	R/W	Temperature3 (VTIN3) base temperature. The temperature is added by both monitor value and offset value. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree

7.70 FAN 3 Pre-Scale Register — Index 93h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM_CLK_SEL3	R/W	**PWM 3 Input Clock Select.** This bit select Fan 3 input clock to pre-scale divider. 0: 3 MHz 1: 125 KHz
6-0	PRE_SCALE3[6:0]	R/W	**Fan 3 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM frequency = (Input clock / pre-scale) / 256

7.71 FAN 3 Duty Cycle Select Register — Index 94h (Bank 0)

Power on default: FFh

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	F3_DC[7:0]	R/W	**Fan 3 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan3 control mode, read this register would return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX/256*100%) during one cycle.

7.72 FAN 3 Configuration Register — Index 95h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM3INV	RO	PWMOUT3 input value if PWMOUT3 as GPIn. Return '1', the pin 23 status is logic high signal. Read '0', pin23 is logic low signal.
6	PWM2INV	RO	PWMOUT2 input value if PWMOUT2 as GPIn. Return '1', the pin 11 status is logic high signal. Read '0', pin11 is logic low signal.
5	PWM1INV	RO	PWMOUT1 input value if PWMOUT1 as GPIn. Return '1', the pin 10 status is logic high signal. Read '0', pin10 is logic low signal.
4	Reserved	Reserved	Reserved
3-2	FAN3_TYPE	R/W	FAN 3 PWM Control Type. 00 - Manual PWM Control. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.
1	Reserve	R/W	Reserved
0	FAN3_OB	R/W	**Enable Fan 3 as Output Buffer.** Set to 1, FANPWM3 can drive logical high or logical low. Default Pin 23 (PWMOUT3) is open-drain.

7.73 Fan 3 Target Temperature Register/Target Fan 3 Speed Control Register — Index 96h (Bank 0)

Power on default: 00h

VTIN3 target temperature register for Thermal Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved	R/W	Reserved.
6-0	FAN_TAR_T3[6:0]	R/W	**Fan 3 Target Temperature.** Only for Thermal Cruise mode. When the temperature 3 over the target temperature add tolerance temperature, the smart fan 3 duty cycle will up count until the duty cycle obtain to FFh.

Fan 3 target speed register for Fan Speed Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	FAN_TAR_CNT3 [7:0]	R/W	**Target Fan 3 Speed Control.** Only for Fan Speed Cruise Mode. When the fan 3 monitored Fan 3 Count over the target Fan Count add tolerance, the fan duty cycle will up/down count until the duty cycle have been corresponding the monitored speed count.

7.74 Tolerance of Fan 3 Target Temperature or Speed Register — Index 97h (Bank 0)

Power on default: 00h

Tolerance of VTIN3 target temperature register

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN3INV	RO	FAN 3 input value if FANINC3 sets to 1. Return '1', the pin 18 status is logic high signal. Read '0', pin18 is logic low signal.
6	FAN2INV	RO	FAN 2 input value if FANINC2 sets to 1. Return '1', the pin 19 status is logic high signal. Read '0', pin19 is logic low signal.
5	FAN1INV	RO	FAN 1 input value if FANINC1 sets to 1. Return '1', the pin 20 status is logic high signal. Read '0', pin20 is logic low signal.
4	Reserved	Reserved	Reserved
3-0	TOL_T3[3:0]	R/W	Tolerance of Fan 3 Target Temperature. Only for Thermal Cruise mode.

Tolerance of Fan 3 target speed register.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN3INV	RO	FAN 3 input value if FANINC3 sets to 1. Return '1', the pin 18 status is logic high signal. Read '0', pin18 is logic low signal.
6	FAN2INV	RO	FAN 2 input value if FANINC2 sets to 1. Return '1', the pin 19 status is logic high signal. Read '0', pin19 is logic low signal.
5	FAN1INV	RO	FAN 1 input value if FANINC1 sets to 1. Return '1', the pin 20 status is logic high signal. Read '0', pin20 is logic low signal.
4	Reserved	Reserved	Reserved
3-0	TOL_FS3[3:0]	R/W	Tolerance of Fan 3 Target Speed Count. Only for Fan Speed Cruise mode.

7.75 Fan 3 PWM Stop Duty Cycle Register — Index 98h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_DC3[7:0]	R/W	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this value. This register should be written a non-zero minimum PWM stop duty cycle.

7.76 Fan 3 Start-up Duty Cycle Register — Index 99h (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	START_DC3[7:0]	R/W	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

7.77 Fan 3 Stop Time Register — Index 9Ah (Bank 0)

Power on default: 3Ch

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_TIME3[7:0]	R/W	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

7.78 Interrupt Status Register III — Index 9Bh (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6	FAN5	Read Only	A one indicates the fan count limit of FAN5 has been exceeded.
5	FAN4	Read Only	A one indicates the fan count limit of FAN4 has been exceeded.
4	VBAT	Read Only	A one indicates a high or low limit of VBAT has been exceeded.
3	VSB	Read Only	A one indicates a high or low limit of VSB has been exceeded.
2	TART3	Read Only	**Target Temperature 3 Status.** A one indicates VTIN3 with Fan 3 full speed can not be in the specific range after 3 minutes.
1	TART2	Read Only	**Target Temperature 2 Statue.** A one indicates VTIN2 temperature with Fan 2 full speed can not be in the specific range after 3 minutes.
0	TART1	Read Only	**Target Temperature 1 Statue.** A one indicates VTIN1 temperature with Fan 1 full speed can not be in the specific range after 3 minutes.

7.79 SMI# Mask Register III — Index 9Ch (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6	FAN5	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
5	FAN4	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
4	VBAT	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
3	VSB	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt.
2	TART3	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt. (Target temperature 3)
1	TART2	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt. (Target temperature 2)
0	TART1	R/W	A one disables the corresponding interrupt status bit for SMI# interrupt. (Target temperature 1)

7.80 Interrupt Mask Register III — Index 9Dh (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6	FAN5	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
5	FAN4	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
4	VBAT	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
3	VSB	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt.
2	TART3	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt. (Target temperature 3)
1	TART2	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt. (Target temperature 2)
0	TART1	R/W	A one disables the corresponding interrupt status bit for IRQ interrupt. (Target temperature 1)

7.81 FAN4_PRE_SCALE register — Index 9Eh (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM_CLK_SEL4	R/W	**PWM 4 Input Clock Select.** This bit select Fan 4 input clock to pre-scale divider. 0: 3 MHz 1: 125 KHz
6:0	PRE_SCALE4 [6:0]	R/W	**Fan 4 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM frequency = (Input clock / pre-scale) / 256

7.82 FAN5_PRE_SCALE register — Index 9Fh (Bank 0)

Power on default: 01h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM_CLK_SEL5	Read /Write	**PWM 5 Input Clock Select.** This bit select Fan 5 input clock to pre-scale divider. 0: 3 MHz 1: 125 KHz
6:0	PRE_SCALE5[6:0]	Read /Write	**Fan 5 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM frequency = (Input clock / pre-scale) / 256

7.83 FAN 4 Duty Cycle Select Register—A0h (Bank 0)

Power on default: FFh

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	F4_DC[7:0]	R/W	**Fan 4 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan3 control mode, read this register would return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX/256*100%) during one cycle.

7.84 FAN 5 Duty Cycle Select Register—A1h (Bank 0)

Power on default: FFh

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	F5_DC[7:0]	R/W	**Fan 5 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan3 control mode, read this register would return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX/256*100%) during one cycle.

7.85 BEEP Control Register 3 — Index A3h (Bank 0)

Power on default: 00h ; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	EN_USER_BP	R/W	User defines BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)
6	FAN5_BP	R/W	Enable BEEP output from FAN5 Write 1; enable BEEP output. Set 0 (default value), it will be disable BEEP tone output.
5	FAN4_BP	R/W	Enable BEEP output from FAN4. Write 1; enable BEEP output. Set 0 (default value), it will be disable BEEP tone output.
4	EN_TART3_BP	R/W	Enable BEEP output from Target temperature 3. Write 1; enable BEEP output. Set 0 (default value), it will be disable BEEP tone output.
3	EN_TART2_BP	R/W	Enable BEEP output from Target temperature 2. Write 1; enable BEEP output. Set 0 (default value), it will be disable BEEP tone output.

BEEP Control Register 3 — Index A3h (Bank 0) , continued

BIT	NAME	ATTRIBUTE	DESCRIPTION
2	EN_TART1_BP	R/W	Enable BEEP output from Target temperature 1. Write 1; enable BEEP output. Set 0 (default value), it will be disable BEEP tone output.
1	EN_VBAT_BP	R/W	Enable BEEP output from V-Core B. Write 1; enable BEEP output, which is default value.
0	EN_VSB_BP	R/W	Enable BEEP Output from V-Core A if the monitor value exceeds the limits value. Write 1, enable BEEP output, which is default value.

7.86 Speech Flash Memory Read Data Registers — Index A4h-A5h (Bank 0)

Power on default: 00h

INDEX	NAME	ATTRIBUTE	DESCRIPTION
A4h	SPEECHRD2	RO	**Speech Flash Read Data 2.** Speech flash reading data bits [23:16].
A5h	SPEECHRD3	RO	**Speech Flash Read Data 3.** Speech flash reading data bits [31:24].

7.87 EVNTRAP1- 5 and GPIO 5-9 Select — Index A6h (Bank 0)

Power on default: 00h

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	GPIO_SEL	R/W	Write '1' to this bit then read it, if return '0' means speech function else means GPIO function.
6	SMI_LEDOUT	R/W	Select SMI# or LEDOUT function at pin 44. Default is SMI# function.
5	Reserved	Reserved	
4	EVNT5_GPIO9	R/W	Write '1' select to pin 1 as GPIO9 function when using speech. Default is '0'. Note: Index 15h bit6='0' if use GPIO function at this pin.
3	EVNT4_GPIO8	R/W	Write '1' select to pin 48 as GPIO8 function when using speech. Default is '0'. Note: Index 15h bit6='0' if use GPIO function at this pin.
2	EVNT3_GPIO7	R/W	Write '1' select to pin 47 as GPIO7 function when using speech. Default is '0'. Note: Index 15h bit6='0' if use GPIO function at this pin.
1	EVNT2_GPIO6	R/W	Write '1' select to pin 46 as GPIO6 function when using speech. Default is '0'. Note: Index 15h bit6='0' if use GPIO function at this pin.
0	EVNT1_GPIO5	R/W	Write '1' select to pin 45 as GPIO5 function when using speech. Default is '0'.

7.88 Flash Page count — Index A7h (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-5	Reserved		Reserved
4-0	Page count	RO	Flash (W55FXX) size of each page is 512K, so read these bits may know the flash size when finish page coding program.

7.89 Real Time Hardware Status Register I — Index A9h (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	FAN2	Read Only	Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.
6	FAN1	Read Only	Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.
5	TEMP2	Read Only	Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.
4	TEMP1	Read Only	Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.
3	5VDD	Read Only	Set 1, the voltage of +5V is over the limit value. Set 0, the voltage of +5V is in the limit range.
2	+3.3VIN	Read Only	Set 1, the voltage of +3.3V is over the limit value. Set 0, the voltage of +3.3V is in the limit range.
1	VINR0	Read Only	Set 1, the voltage of VINR0 is over the limit value. Set 0, the voltage of VINR0 is in the limit range.
0	Vcore	Read Only	Set 1, the voltage of VCORE is over the limit value. Set 0, the voltage of VCORE is in the limit range.

7.90 Real Time Hardware Status Register II — Index AAh (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Revered	Read Only	Reserved.
6	VINR1	Read Only	Set 1, the voltage of VINR1 is over the limit value. Set 0, the voltage of VINR1 is in the limit range.
5	TEMP3	Read Only	Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.
4	Chassis Intrusion	Read Only	Set 1, the case open sensor is sensed the high value. Set 0, the case open signal is low.

Real Time Hardware Status Register II — Index AAh (Bank 0), continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
3	FAN3	Read Only	Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is during the limit range.
2	-5VIN	Read Only	Set 1, the voltage of -5V is over the limit value. Set 0, the voltage of -5V is during the limit range.
1	-12VIN	Read Only	Set 1, the voltage of -12V is over the limit value. Set 0, the voltage of -12V is during the limit range.
0	+12VIN	Read Only	Set 1, the voltage of +12V is over the limit value. Set 0, the voltage of +12V is in the limit range.

7.91 Real Time Hardware Status Register III — Index ABh (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6	FAN5	Read Only	Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is during the limit range.
5	FAN4	Read Only	Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is during the limit range.
4	VBAT	Read Only	Set 1, the voltage of VBAT is over the limit value. Set 0, the voltage of VBAT is during the limit range.
3	VSB	Read Only	Set 1, the voltage of VSB is over the limit value. Set 0, the voltage of VSB is in the limit range.
2	TART3	Read Only	Set 1, when target temperature 3 with Fan 3 full speed can not be in the range after 3 minutes. Set 0, the temperature or speed is in the specific range.
1	TART2	Read Only	Set 1, when target temperature 2 with Fan 2 full speed can not be in the range after 3 minutes. Set 0, the temperature or speed is in the specific range.
0	TART1	Read Only	Set 1, when target temperature 1 with Fan 3 full speed can not be in the range after 3 minutes. Set 0, the temperature or speed is in the specific range.

7.92 Revered — Index AC - AFh (Bank 0)

7.93 Value RAM 2— Index B0h – B7h (BANK 0)

ADDRESS A6-A0 AUTO-INCREMENT	DESCRIPTION
B0h	5VSB reading
B1h	VBAT reading
B2h	VINR1 reading
B3h	Reserved
B4-B5h	5VSB High/Low Limit
B6-7h	VBAT High/ Low Limit
B8-B9h	VINR1 High/ Low Limit.
BAh	FAN4 count reading
BBh	FAN5 count reading
BC	FAN4 limit count
BD	FAN5 limit count
BE-BFh	Revered

7.94 Temperature Sensor 2 Temperature (High Byte) Register — Index C0h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	TEMP2<8:1>	Read Only	Temperature <8:1> of VTIN 2, which is high byte.

7.95 Temperature Sensor 2 Temperature (Low Byte) Register — Index C1h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TEMP2<0>	Read Only	Temperature <0> of VTIN2, which is low byte.
6-0	Reserved	Read Only	Read 0.

7.96 Temperature Sensor 2 Configuration Register — Index C2h (Bank 0)

Power on default: 00h; Reset by MR

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-5	Reserved		Reserved
4-3	FAULT	R/W	Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
2:1	Reserved		Reserved
0	STOP2	R/W	When set to 1 the sensor will stop monitor.

7.97 Temperature Sensor 2 Hysteresis (High Byte) Register — Index C3h (Bank 0)

Power on default: 4Bh; Reset by MR

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	THYST2<8:1>	R/W	Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

7.98 Temperature Sensor 2 Hysteresis (Low Byte) Register — Index C4h (Bank 0)

Power on default: 00h; Reset by MR

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	THYST2<0>	R/W	Temperature hysteresis bit 0, which is low Byte.
6-0	Reserved	Read Only	Read 0

7.99 Temperature Sensor 2 Over-temperature (High Byte) Register — Index C5h (Bank 0)

Power on default: 50h; Reset by MR

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	TOVF2<8:1>	R/W	Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

7.100 Temperature Sensor 2 Over-temperature (Low Byte) Register — Index C6h (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TOVF2<0>	R/W	Over-temperature bit 0, which is low Byte.
6-0	Reserved	Read Only	Read 0

7.101 Temperature Sensor 3 Temperature (High Byte) Register — Index C8h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	TEMP3<8:1>	Read Only	Temperature <8:1> of VTIN3, which is high byte.

7.102 Temperature Sensor 3 Temperature (Low Byte) Register — Index C9h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TEMP3<0>	Read Only	Temperature <0> of VTIN3, which is low byte.
6-0	Reserved	Read Only	Read 0.

7.103 Temperature Sensor 3 Configuration Register — Index CAh (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-5	Reserved		Reserved
4-3	FAULT	R/W	Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
2:1	Reserved	R/W	Reserved
0	STOP3	R/W	When set to 1 the sensor will stop monitor.

7.104 Temperature Sensor 3 Hysteresis (High Byte) Register — Index CBh (Bank 0)

Power on default: 4Bh; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	THYST3<8:1>	R/W	Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

7.105 Temperature Sensor 3 Hysteresis (Low Byte) Register — Index CCh (Bank 0)

Poweron default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
6-0	Reserved	Read Only	Read 0
7	THYST3<0>	R/W	Temperature hysteresis bit 0, which is low Byte.

7.106 Temperature Sensor 3 Over-temperature (High Byte) Register — Index CDh (Bank 0)

Power on default: 50h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	OVTF3<8:1>	R/W	Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

7.107 Temperature Sensor 3 Over-temperature (Low Byte) Register — Index CEh (Bank 0)

Power on default: 00h; Reset by MR.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	OVTF3<0>	R/W	Over-temperature bit 0, which is low Byte.
6-0	Reserved		Reserved

8. ARP (ADDRESS RESOLUTION PROTOCOL) USE REGISTER DEFINED

8.1 Unique Device Identifier (UDID) -- 20h-2Fh (Bank 1)

In order to provide a mechanism to isolate each device for the purpose of address assignment each device must implement a unique device identifier (UDID). This 128-bit number is comprised of the following fields:

1 Byte	1 Byte	2 Byte	2 Byte	2 Byte	2 Byte	2 Byte	4 Byte
Device Capabilities	Version/ Revision	Vendor ID	Device ID	Interface	Subsystem Vendor ID	Subsystem Device ID	Vendor Specific ID
Bank 1 Index 20h	Bank 1 Index 21h	Bank 1 22h-23h	Bank 1 24h-25h	Bank 1 26h-27h	Bank 1 28h-29h	Bank 1 2Ah-2Bh	Bank 1 2Ch-2Fh

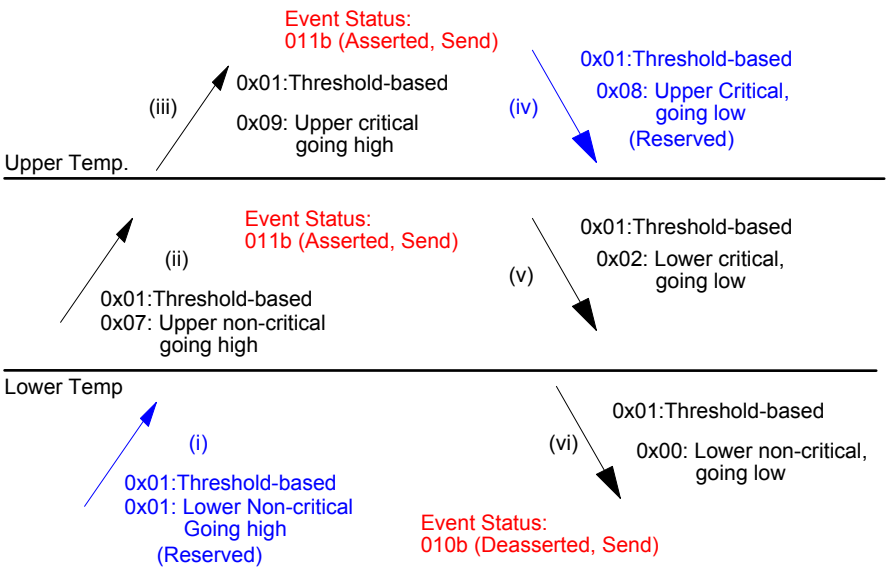
INDEX	ATTRIBUTE	DESCRIPTIONS
20h	R/W	**Device Capabilities (DEV_CAP [7:0]).** Describes the device's capabilities. See detail SMBus 2.0.
21h	R/W	**Version/Revision (VERSION [7:0]).** UDID version number and silicon revision identification. See detail SMBus2.0 Tues.
22-23h	R/W	**Vendor ID (VENDOR_ID [15:0]).** The device manufacturer's ID as assigned by the SBS Implementers' Forum or the PCI SIG.
24-25h	R/W	**Device ID (DEV_ID [15:0]).** The device ID as assigned by the device manufacturer (identified by the Vendor ID field).
26-27h	R/W	**Interface (INTERFACE [15:0]).** Identifies the protocol layer interfaces supported over the SMBus connection by the device. For example, ASF and IPMI.
28-29h	R/W	**Subsystem Vendor ID (SVENDOR_ID [15:0]).** This field may hold a value derived from any of several sources: 1. The device manufacturer's ID as assigned by the SBS Implementers' Forum or the PCI SIG. 2. The device OEM's ID as assigned by the SBS Implementers' Forum or the PCI SIG. 3. A value that, in combination with the Subsystem Device ID, can be used to identify an organization or industry group that has defined a particular common device interface specification.
2A-2Bh	R/W	**Subsystem Device ID (SDEV_ID [15:0]).** The subsystem ID identifies a specific interface, implementation, or device. The Subsystem ID is defined by the party identified by the Subsystem Vendor ID field.
2C-2Fh	R/W	**Vendor Specific ID (SPEC_ID [31:0]).** A unique number per device. See detail SMBus 2.0.

8.2 ASF Sensor Environmental Event

The document in ASF specification version 0.73 has indicated the listed table is presented as a ***guide*** only (Section 3.3.5.1 Page 8). It is ***not*** intended to represent a complete list of the possible environmental events from a system. The definition of the Event is shown as follow.

8.2.1 Temperature: Get Event Data message

In the W83791D/G, it has three temperatures for monitoring System Board, CPU1, and CPU2. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

ASF PACKET DATA	TEMPERATURE 1
Event sensor type	0x01 (Temperature sensor)
Event type Event offset	Threshold-based: 0x01h. The W83971D/G does not implement "generic severity".  Event sensor type: 0x01 (Temperature) Event Type: 0x01 (Threshold-based)
Event source type	The W83791D/G is complying ASF 1.0 specification and the value is 0x68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83791D/G is APR assigned address.
Sensor number	Temperature 1: 0Eh (Don't use 00h and FFh. Therefore 01h → VIN0). Temperature 2: 0Fh Temperature 3: 10h

Temperature: Get Event Data message, continued.

<table>
<tr><th>ASF PACKET DATA</th><th>TEMPERATURE 1</th></tr>
<tr><td>Entity ID</td><td>Temperature 1: 07h (System board)
Temperature 2/3: 03h (Processor)
These are defined in Table 28-11 of IPMI v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.</td></tr>
<tr><td>Entity instance</td><td>Temperature 1: 01h (main system board).
Temperature 2: 01h (Processor 1)
Temperature 3: 02h (Processor 2)
These are programmable.</td></tr>
<tr><td>Event status index</td><td>Temperature 1: 0Dh (zero-based)
Temperature 2: 0Eh
Temperature 3: 0Fh</td></tr>
<tr><td>Event status</td><td>
<table>
<tr><th>Status Value</th><th>Status type</th><th>Description</th><th>Byte Count</th></tr>
<tr><td>0000_0010b</td><td>Deasserted (send)</td><td>Refer as above figure.</td><td>0Bh</td></tr>
<tr><td>0000_0011b</td><td>Asserted (send)</td><td>W83791D/G will respond all relative information.</td><td>0Bh</td></tr>
<tr><td>0000_0111b</td><td>Event Status End</td><td>When event status index is more than 10h, the machine will be ended the transmission.</td><td>02h</td></tr>
</table>
The reference table of ASF 0.64 is shown as following.
</td></tr>
<tr><td>Event Severity</td><td>Monitor (0x01): That is represented the monitored temperature is under the lower temperature.
Non Critical (0x08): that is represented the temperature is located between the lower and upper temperature.
Critical Condition (0x10): that is represented the monitored temperature is over the upper temperature.

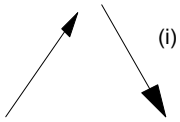
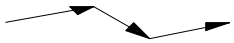
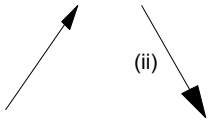
Critical Condition (0x10)
Upper Temp. ——————————
Non Critical (0x08)
Lower Temp. ——————————
Monitor (0x01)</td></tr>
</table>

Entity ID and Instance (Default):

ENTITY ID (PROGRAMMABLE)	ENTITY INSTANCE (PROGRAMMABLE)	SENSOR IN W83791D/G	EVENT STATUS INDEX	EVENT NUMBER	EVENT SENSOR TYPE
07h (System Board)	01h	+3.3VIN	02h	03h	02h (Voltage)
	01h	+5VIN	03h	04h	02h
	01h	+12VIN	04h	05h	02h
	01h	-12VIN	05h	06h	02h
	01h	-5VIN	06h	07h	02h
	01h	VSB	07h	08h	02h
	01h	VBAT	08h	09h	02h
	01h	VINR0	09h	0Ah	02h
	01h	FAN1	0Ah	0Bh	04h (Fan)
	01h	Temperature1	0Dh	0Eh	01h (Temperature)
03h (Processor)	01h	VCORE	00h	01h	02h
	01h	FAN2	0Bh	0Ch	04h
	01h	Temperature 2	0Eh	0Fh	01h
	02h	VINR1	01h	02h	02h
	02h	FAN3	0Ch	0Dh	04h
	02h	Temperature 3	0Fh	10h	01h
23h (System Chassis)	01h	Case Intrusion	10h	11h	05h (Chassis Intrusion)

8.2.2 Voltage: Get Event Data message

In the W83791D/G, it has three temperatures for monitoring System Board, CPU1, and CPU2. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

<table>
<tr><th>ASF PACKET DATA</th><th>VOLTAGE INPUT</th></tr>
<tr><td>Event sensor type</td><td>02h (Voltage sensor)</td></tr>
<tr><td>Event type
Event offset</td><td>Discrete (Generic Severity): 07h
 
(i)
07h: Discrete (Generic Severity)
02h: Transition to Critical from less severe
Event Status: 011b (Asserted, send)
High voltage
 
07h: Discrete (Generic Severity)
07h: Monitor
Event Status: 010b (Deasserted, send)
Low voltage
 
(ii)
07h: Discrete (Generic Severity)
02h: Transition to Critical from less severe
Event Status: 011b (Asserted, send)
Event sensor type: 02h (Voltage)
Event Type: 07h (Discrete, Generic Severity)</td></tr>
<tr><td>Event source type</td><td>The W83791D/G is complying ASF 1.0 specification and the value is 0 x 68.</td></tr>
<tr><td>Sensor device</td><td>The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83791D/G is APR assigned address.</td></tr>
<tr><td>Sensor number</td><td>The number is shown as following:
<table>
<tr><th>Voltage Sensor</th><th>Sensor Number</th></tr>
<tr><td>VCORE</td><td>01h</td></tr>
<tr><td>VINR0</td><td>02h</td></tr>
<tr><td>+3.3VIN</td><td>03h</td></tr>
<tr><td>+5VIN</td><td>04h</td></tr>
<tr><td>+12VIN</td><td>05h</td></tr>
<tr><td>-12VIN</td><td>06h</td></tr>
<tr><td>-5VIN</td><td>07h</td></tr>
<tr><td>VSB</td><td>08h</td></tr>
<tr><td>VBAT</td><td>09h</td></tr>
<tr><td>VINR1</td><td>0Ah</td></tr>
</table></td></tr>
</table>

Voltage: Get Event Data message, continued.

<table>
<tr><th>ASF PACKET DATA</th><th>VOLTAGE INPUT</th></tr>
<tr><td>Entity ID</td><td>The Entity ID is shown as following.
<table>
<tr><th>Voltage Sensor</th><th>Entity ID</th></tr>
<tr><td>VCORE</td><td>03h (Processor)</td></tr>
<tr><td>VINR0</td><td rowspan="9">07h (System board)</td></tr>
<tr><td>+3.3VIN</td></tr>
<tr><td>+5VIN</td></tr>
<tr><td>+12VIN</td></tr>
<tr><td>-12VIN</td></tr>
<tr><td>-5VIN</td></tr>
<tr><td>VSB</td></tr>
<tr><td>VBAT</td></tr>
<tr><td>VINR1</td><td>03h (Processor)</td></tr>
</table>
These ID are defined in Table 28-11 of IPMI v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.</td></tr>
<tr><td>Entity instance</td><td>The Entity Instance is shown as following.
<table>
<tr><th>Sensor</th><th>Entity Instance</th></tr>
<tr><td>VCORE</td><td>01h (Processor 1)</td></tr>
<tr><td>VINR0</td><td rowspan="9">01h (Main system board)</td></tr>
<tr><td>+3.3VIN</td></tr>
<tr><td>+5VIN</td></tr>
<tr><td>+12VIN</td></tr>
<tr><td>-12VIN</td></tr>
<tr><td>-5VIN</td></tr>
<tr><td>VSB</td></tr>
<tr><td>VBAT</td></tr>
<tr><td>VINR1</td><td>02h (Processor 2)</td></tr>
</table></td></tr>
<tr><td>Event status index</td><td>VCORE: 00h
VINR0: 01h
+3.3VIN: 02h
+5VIN : 03h
+12VIN: 04h
-12VIN: 05h
-5VIN: 06h
VSB: 07h
VBAT: 08h
VINR1: 09h</td></tr>
</table>

Voltage: Get Event Data message, continued.

<table>
<tr><th>ASF PACKET DATA</th><th>VOLTAGE INPUT</th></tr>
<tr><td>Event status</td><td>
<table>
<tr><th>Status Value</th><th>Status type</th><th>Description</th><th>Byte Count</th></tr>
<tr><td>0000_0010b</td><td>Desserted (send)</td><td></td><td>0Bh</td></tr>
<tr><td>0000_0011b</td><td>Asserted (send)</td><td>W83791D/G will respond all relative information.</td><td>0Bh</td></tr>
<tr><td>0000_0111b</td><td>Event Status End</td><td>When event status index is more than 0Fh, the machine will be ended the transmission.</td><td>02h</td></tr>
</table>
The reference table of ASF 0.64 is shown as following.
</td></tr>
<tr><td>Event Severity</td><td>Monitor (0x01): That is represented the monitored voltage is during the limit value.
Critical Condition (0x10): that is represented the monitored voltage is over the limit value.

Critical Condition (0x10)
Upper Volt. ——————————
Monitor (0x01)
Lower Volt. ——————————
Critical Condition (0x10)</td></tr>
</table>

8.2.3 Fan: Get Event Data message

In the W83791D/G, it has three temperatures for monitoring System Board, CPU1, and CPU2. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

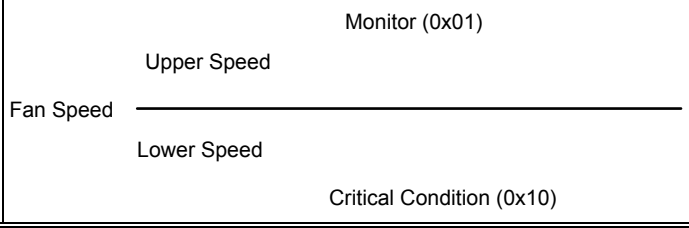
<table>
<tr><th>ASF PACKET DATA</th><th>FAN CLOCK INPUT</th></tr>
<tr><td>Event sensor type</td><td>04h (Fan speed sensor)</td></tr>
<tr><td>Event type
Event offset</td><td>Discrete (Generic Severity): 07h
(i) 05h: 'digital' Discrete (Generic Severity)
00h: Limit Not Exceeded
Event Status: 010b (Deasserted, send)
High Speed (Low Count)
Fan Limit ——————————
Lower Speed (High Count) Event Status: 011b (Asserted, send)
05h: 'digital' Discrete (Generic Severity)
01h: Limit Exceeded

Event sensor type: 04h (Fan)
Event Type: 05h ('digital ' Discrete, Generic Severity)</td></tr>
</table>

Fan: Get Event Data message, continued.

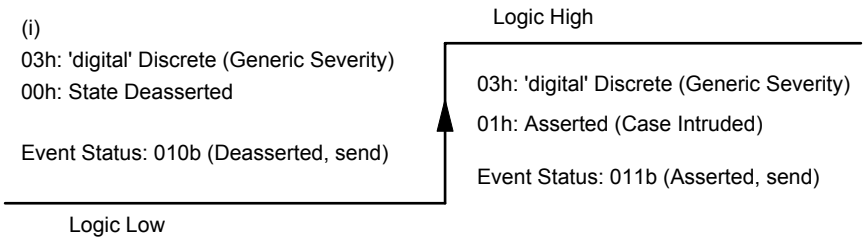
<table>
<tr><th>ASF PACKET DATA</th><th>FAN CLOCK INPUT</th></tr>
<tr><td>Event source type</td><td>The W83791D/G is complying ASF 1.0 specification and the value is 0 x 68.</td></tr>
<tr><td>Sensor device</td><td>The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83791D/G is APR assigned address.</td></tr>
<tr><td>Sensor number</td><td>The number is shown as following:
<table>
<tr><th>Fan Sensor</th><th>Sensor Number</th></tr>
<tr><td>FAN 1</td><td>0Bh</td></tr>
<tr><td>FAN 2</td><td>0Ch</td></tr>
<tr><td>FAN 3</td><td>0Dh</td></tr>
</table></td></tr>
<tr><td>Entity ID</td><td>The Entity ID is shown as following.
<table>
<tr><th>Voltage Sensor</th><th>Entity ID (default)</th></tr>
<tr><td>FAN 1</td><td>07h (System board)</td></tr>
<tr><td>FAN 2</td><td rowspan="2">03h (Processor)</td></tr>
<tr><td>FAN 3</td></tr>
</table>
These ID are defined in Table 28-11 of IPMI v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.</td></tr>
<tr><td>Entity instance</td><td>The Entity Instance is shown as following.
<table>
<tr><th>Fan Sensor</th><th>Entity Instance (default)</th></tr>
<tr><td>FAN 1</td><td>01h (Main system board)</td></tr>
<tr><td>FAN 2</td><td>01h (Processor 1)</td></tr>
<tr><td>FAN 3</td><td>02h (Processor 2)</td></tr>
</table></td></tr>
<tr><td>Event status index</td><td>FAN1 : 0Ah
FAN2 : 0Bh
FAN3 : 0Ch</td></tr>
<tr><td>Event status</td><td>
<table>
<tr><th>Status Value</th><th>Status type</th><th>Description</th><th>Byte Count</th></tr>
<tr><td>0000_0010b</td><td>Deasserted (send)</td><td></td><td>0Bh</td></tr>
<tr><td>0000_0011b</td><td>Asserted (send)</td><td>W83791D/G will respond all relative information.</td><td>0Bh</td></tr>
<tr><td>0000_0111b</td><td>Event Status End</td><td>When event status index is more than 0Fh, the machine will be ended the transmission.</td><td>02h</td></tr>
</table>
The reference table of ASF 0.64 is shown as following.</td></tr>
</table>

Fan: Get Event Data message, continued.

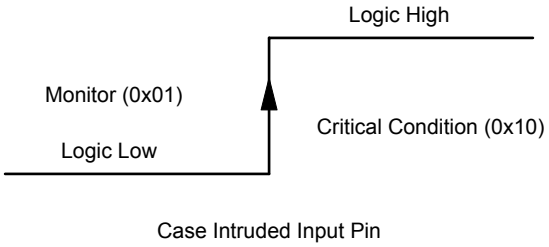
ASF PACKET DATA	FAN CLOCK INPUT
Event Severity	Monitor (0x01): That is represented the monitored fan count is under the limit count. Critical Condition (0x10): that is represented the monitored fan count is over the limit count. 

8.2.4 Case Intrusion: Get Event Data message

In the W83791D/G, it has three temperatures for monitoring System Board. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

ASF PACKET DATA	CASE INTRUSION INPUT
Event sensor type	05h (Chassis Intrusion)
Event type Event offset	'digital' Discrete (Generic Severity): 03h  Event sensor type: 05h (Case Intruded) Event Type: 03h ('digital ' Discrete, Generic Severity)
Event source type	The W83791D/G is complying ASF 1.0 specification and the value is 0 x 68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83791D/G is APR assigned address.
Sensor number	The sensor number for case intruded is 11h
Entity ID	The Entity ID is 23h for case intruded These ID are defined in Table 28-11 of IPMI v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.

Case Intrusion: Get Event Data message, continued.

<table>
<tr><th>ASF PACKET DATA</th><th>CASE INTRUSION INPUT</th></tr>
<tr><td>Entity instance</td><td>The Entity Instance is 01h for (Main system board)</td></tr>
<tr><td>Event status index</td><td>0x0D (W83791D/G sensor index)</td></tr>
<tr><td>Event status</td><td>
<table>
<tr><th>Status Value</th><th>Status type</th><th>Description</th><th>Byte Count</th></tr>
<tr><td>0000_0010b</td><td>Deasserted (send)</td><td></td><td>0Bh</td></tr>
<tr><td>0000_0011b</td><td>Asserted (send)</td><td>W83791D/G will respond all relative information.</td><td>0Bh</td></tr>
<tr><td>0000_0111b</td><td>Event Status End</td><td>When event status index is more than 0Fh, the machine will be ended the transmission.</td><td>02h</td></tr>
</table>
The reference table of ASF 0.64 is shown as following.
</td></tr>
<tr><td>Event Severity</td><td>Monitor (0x01): That is represented the monitored CASEOPEN is logic Low
Critical Condition (0x10): that is represented the monitored CASEOPEN is logic High.
 
</td></tr>
</table>

8.3 ASF Response Registers — Index 40h-7Fh (Bank 1)

8.3.1 ASF Upper/Lower Temperature Registers:

Generic/Upper/Under temperature

INDEX	DESCRIPTION	DEFAULT TEMPERATURE
40h	Non-critical temperature of temperature sensor 1 setting.	4Bh (75 Centigrade)
41h	Critical Temperature of temperature sensor 1 setting	50h (80 Centigrade)
42h	Non-critical temperature of temperature sensor 2 setting.	4Bh
43h	Critical Temperature of temperature sensor 2 setting	50h
44h	Non-critical temperature of temperature sensor 3 setting.	4Bh
45h	Critical Temperature of temperature sensor 3 setting	50h
46h-4Eh	Reserved	Reserved.

Note: When read index 45h (Bank 1) have to use index 46h (Bank 1).

8.3.2 Sensor device: (SMBus Address, Read/Write)

INDEX	DESCRIPTION	DEFAULT VALUE
4Fh	Sensor Device SMBus Address assigned by ARP	00h

8.3.3 Relative Entity ID Table:

INDEX	MONITOR ITEM	DEFAULT ENTITY ID
50h	VIN0 (VCORE)	3 (CPU)
51h	VIN1 (VINR0)	7 (System Board)
52h	VIN2 (+3.3VIN)	7 (System Board)
53h	VIN3 (+5 VIN)	7 (System Board)
54h	VIN4 (+12VIN)	7 (System Board)
55h	VIN5 (-12VIN)	7 (System Board)
56h	VIN6 (-5VIN)	7 (System Board)
57h	VSB	7 (System Board)
58h	VBAT	7 (System Board)
59h	VINR1	3 (CPU)
5Ah	FAN1	7 (System Board)
5Bh	FAN2	3 (CPU)
5Ch	FAN3	3 (CPU)
5Dh	Temperature 1	7 (System Board)
5Eh	Temperature 2	3 (CPU)
5Fh	Temperature 3	3 (CPU)
60h	Chassis Intrusion	23 (System Chassis)
61h-6Fh	Reserved	Reserved

Table of Entity ID defined in PET 1.0 or IPMI 1.0

ENTITY DEFINITION	ENTITY ID
CPU	3
System	7
Memory module	8
System Chassis	23
Fan/Cooling device	29
Memory device	32

8.3.4 Entity Instance Register

Maximum number of instance is 15

INDEX	BIT	ENTITY	ENTITY INSTANCE (DEFAULT VALUE)
70h	<7:4>	VIN0(Vcore)	1 (Processor 1_CPU1).
	<3:0>	VIN1(VINR0)	1 (System board 1).
71h	<7:4>	VIN2 (+3.3VIN)	1 (System board 1).
	<3:0>	VIN3 (+5VIN)	1 (System board 1).
72h	<7:4>	VIN4 (+12VIN)	1 (System board 1).
	<3:0>	VIN5 (-12VIN)	1 (System board 1).
73h	<7:4>	VIN6 (-5VIN)	1 (System board 1).
	<3:0>	VIN7(VSB)	1 (System board 1).
74 h	<7:4>	VIN8(VBAT)	1 (System board 1).
	<3:0>	VIN9(VINR1)	2 (Processor 2_CPU2).
75h	<7:4>	FAN1	1 (System board 1).
	<3:0>	FAN2	1 (Processor 1_CPU1).
76h	<7:4>	FAN3	2 (Processor 2_CPU2)
	<3:0>	TEMP1	1 (System board 1)
77h	<7:4>	TEMP2	1 (Processor 1)
	<3:0>	TEMP3	2 (Processor 2)
78h	<7:4>	Reserved	0
	<3:0>	Chassis	1 (System Chassis)

The Entity for a given event varies according to what entity the environmental sensor is monitoring. For example, a typical managed system board can have temperature monitoring associated with the system board and with the main processor. Thus, the Entity IDs and Entity Instance values for these would be Entity ID=7, Entity Instance=1 for 'main system board' and Entity ID=3, Entity Instance=1 for 'processor 1', respectively.

8.4 BJT RT-Table - 50h-57h (Bank 7) — TEST mode only

Bank 7 registers 50h-57h are BJT table for Winbond test. User doesn't use these registers.

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 DC Characteristics

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

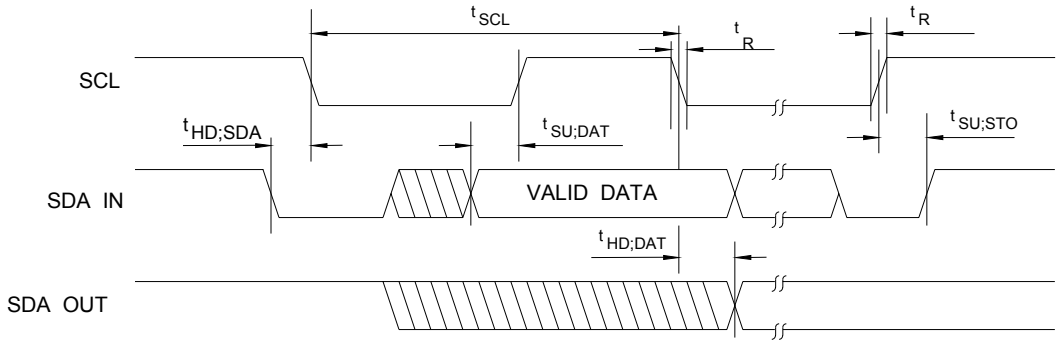
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

DC Characteristics, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

9.3 AC Characteristics

9.3.1 Serial Bus Timing Diagram



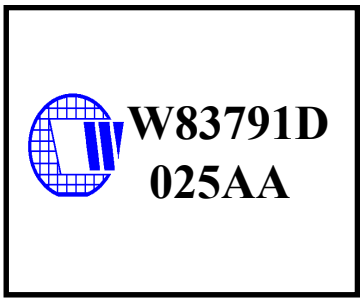
Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

10. HOW TO READ THE TOP MARKING

The top marking of W83791D



Left: Winbond logo
1st line: Type number W83791D, D means LQFP (Thickness = 1.4 mm).
2nd line: Tracking code 025 A A

025: packages made in 2000, week 25
A: assembly house ID; A means ASE, O means OSE
A: IC revision; A means version A, B means version B

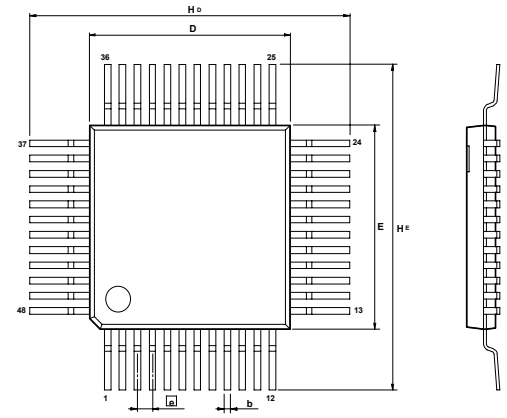
The top marking of W83791G

Left: Winbond logo
1st line: Type number W83791G, G means lead-free package.
2nd line: Tracking code 025 A A

025: packages made in 2000, week 25
A: assembly house ID; A means ASE, O means OSE
A: IC revision; A means version A, B means version B

11. PACKAGE SPECIFICATION

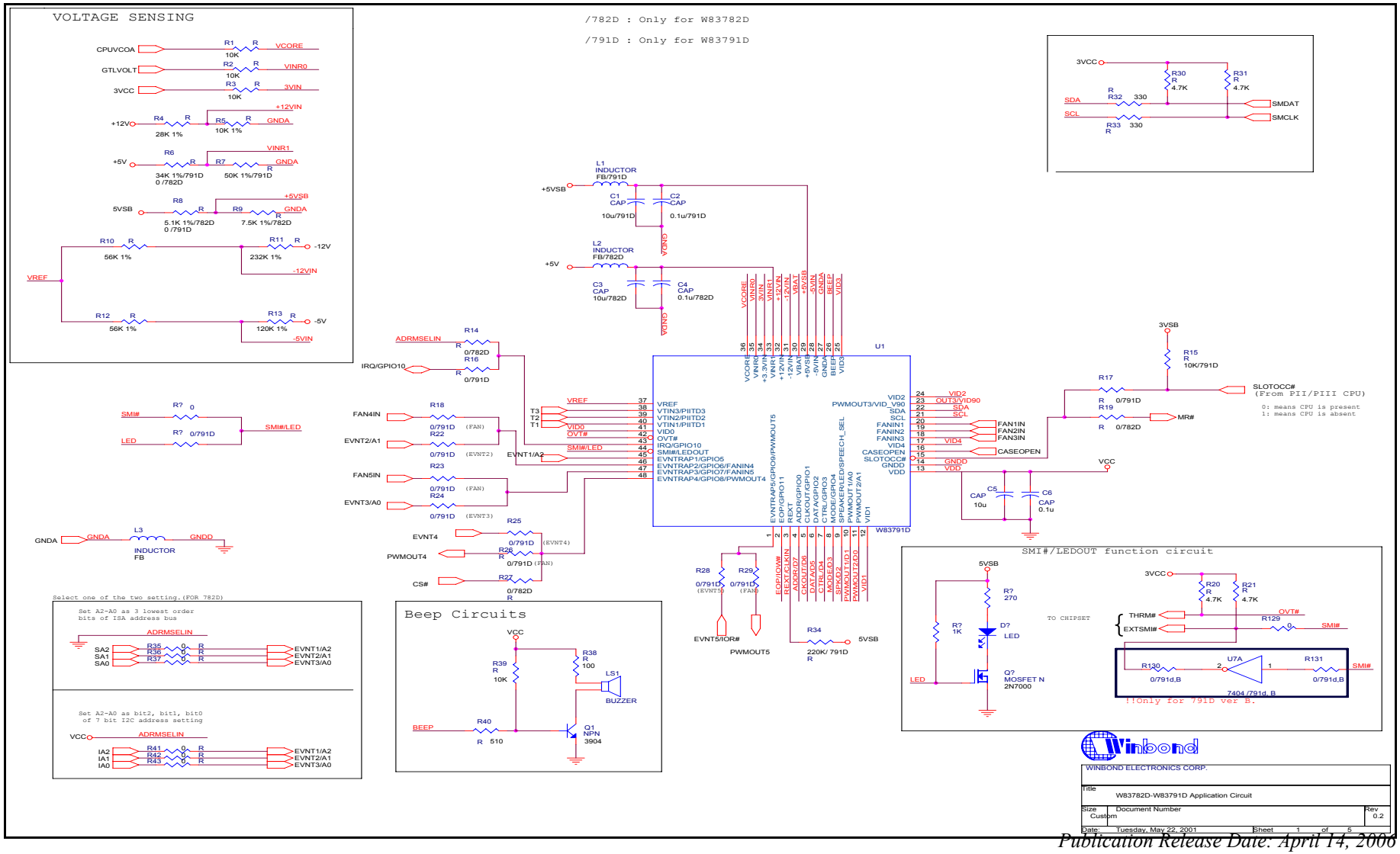
(48-pin LQFP)

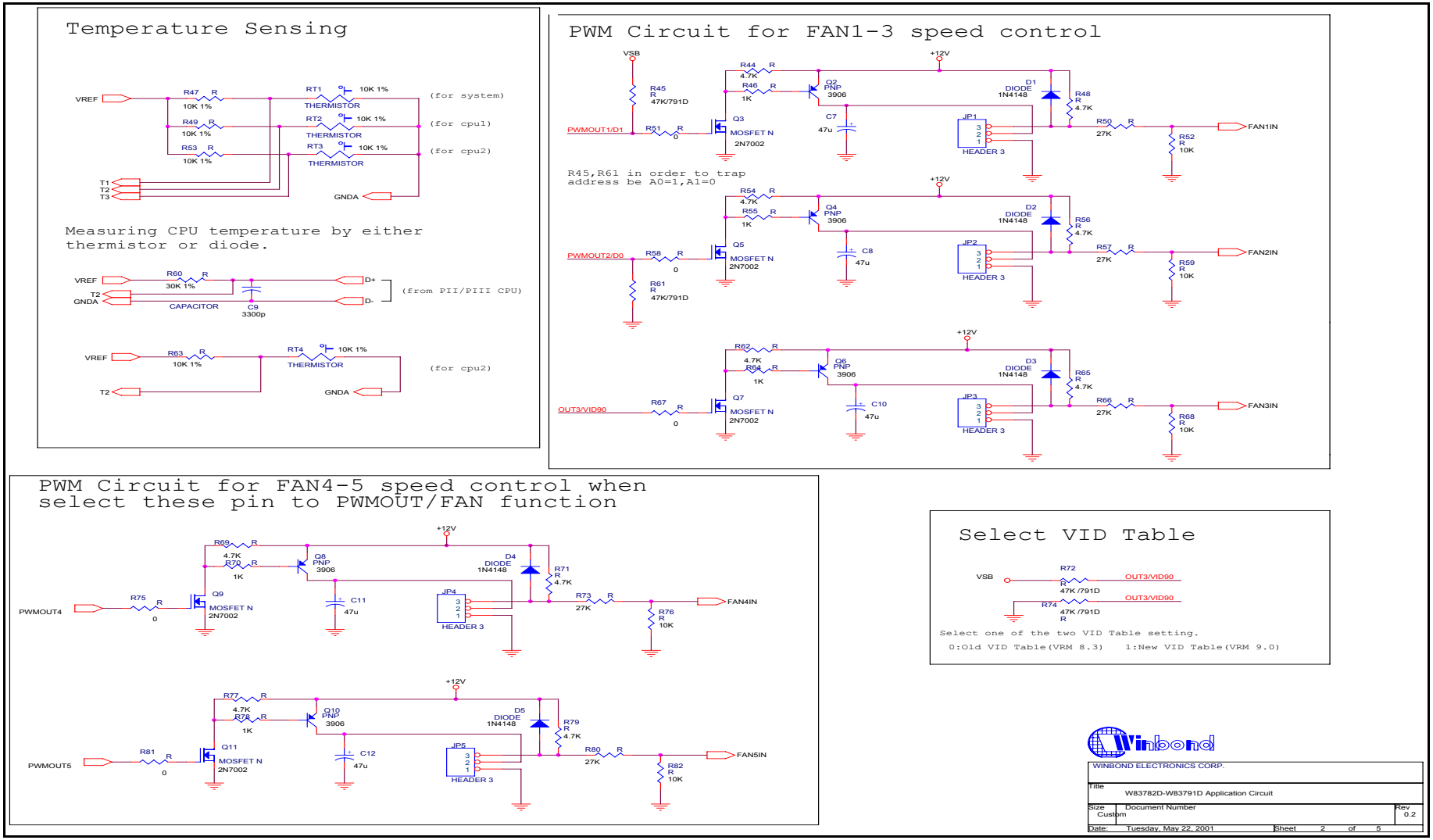


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.


VOLTAGE SENSING
/782D : Only for W83782D
/791D : Only for W83791D
U1
W83791D
Beep Circuits
SMI#/LEDOUT function circuit
Select one of the two setting.(FOR 782D)
WINBOND ELECTRONICS CORP.
W83782D-W83791D Application Circuit
Tuesday, May 22, 2001


Temperature Sensing
VREF
R47 R 10K 1%
RT1 THERMISTOR 10K 1%
(for system)
R49 R 10K 1%
RT2 THERMISTOR 10K 1%
(for cpu1)
R53 R 10K 1%
RT3 THERMISTOR 10K 1%
(for cpu2)
T1
T2
T3
GNDA
Measuring CPU temperature by either thermistor or diode.
VREF
R60 R 30K 1%
T2
GNDA
CAPACITOR
C9 3300p
D+
D-
(from PII/PIII CPU)
VREF
R63 R 10K 1%
RT4 THERMISTOR 10K 1%
(for cpu2)
T2
GNDA
PWM Circuit for FAN1-3 speed control
VSB
+12V
R45 R 47K/791D
R44 R 4.7K
R46 R 1K
Q2 PNP 3906
D1 DIODE 1N4148
R48 R 4.7K
PWMOUT1/D1
R51 R 0
Q3 MOSFET N 2N7002
C7 47u
JP1 HEADER 3
R50 R 27K
R52 R 10K
FAN1IN
R45,R61 in order to trap address be A0=1,A1=0
R54 R 4.7K
R55 R 1K
Q4 PNP 3906
D2 DIODE 1N4148
R56 R 4.7K
PWMOUT2/D0
R58 R 0
Q5 MOSFET N 2N7002
C8 47u
JP2 HEADER 3
R57 R 27K
R59 R 10K
FAN2IN
R61 R 47K/791D
R62 R 4.7K
R64 R 1K
Q6 PNP 3906
D3 DIODE 1N4148
R65 R 4.7K
OUT3/VID90
R67 R 0
Q7 MOSFET N 2N7002
C10 47u
JP3 HEADER 3
R66 R 27K
R68 R 10K
FAN3IN
PWM Circuit for FAN4-5 speed control when select these pin to PWMOUT/FAN function
+12V
R69 R 4.7K
R70 R 1K
Q8 PNP 3906
D4 DIODE 1N4148
R71 R 4.7K
PWMOUT4
R75 R 0
Q9 MOSFET N 2N7002
C11 47u
JP4 HEADER 3
R73 R 27K
R76 R 10K
FAN4IN
R77 R 4.7K
R78 R 1K
Q10 PNP 3906
D5 DIODE 1N4148
R79 R 4.7K
PWMOUT5
R81 R 0
Q11 MOSFET N 2N7002
C12 47u
JP5 HEADER 3
R80 R 27K
R82 R 10K
FAN5IN
Select VID Table
VSB
R72 R 47K /791D
R74 R 47K /791D
OUT3/VID90
OUT3/VID90
Select one of the two VID Table setting.
0:Old VID Table(VRM 8.3) 1:New VID Table(VRM 9.0)
WINBOND ELECTRONICS CORP.
Title
W83782D-W83791D Application Circuit
Size Custom
Document Number
Rev 0.2
Date: Tuesday, May 22, 2001
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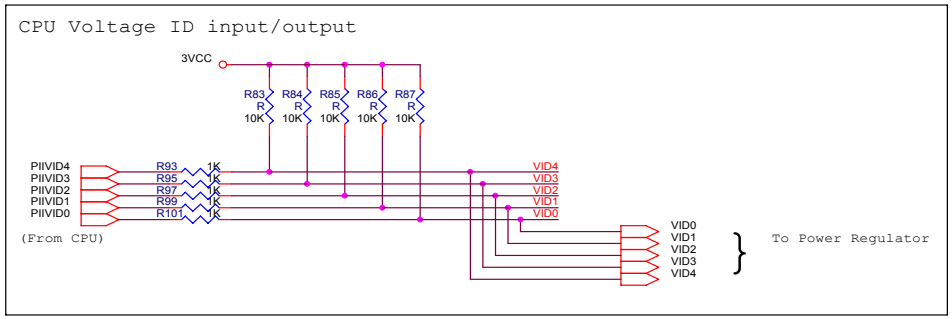

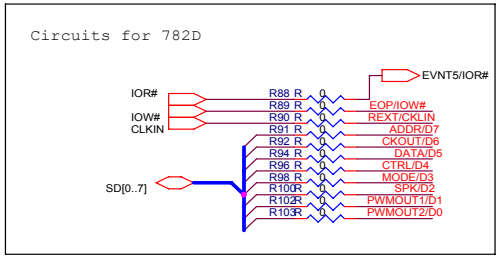

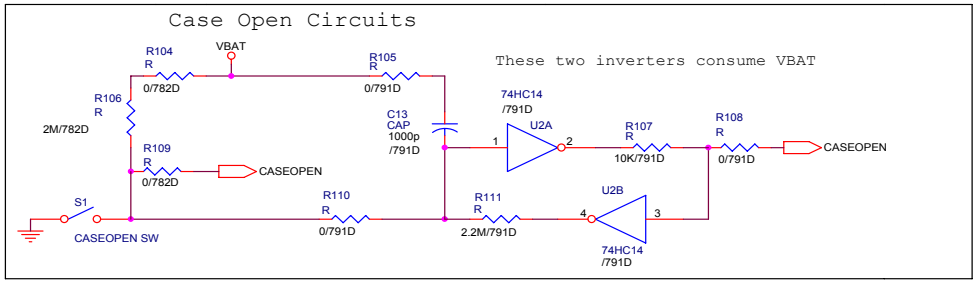

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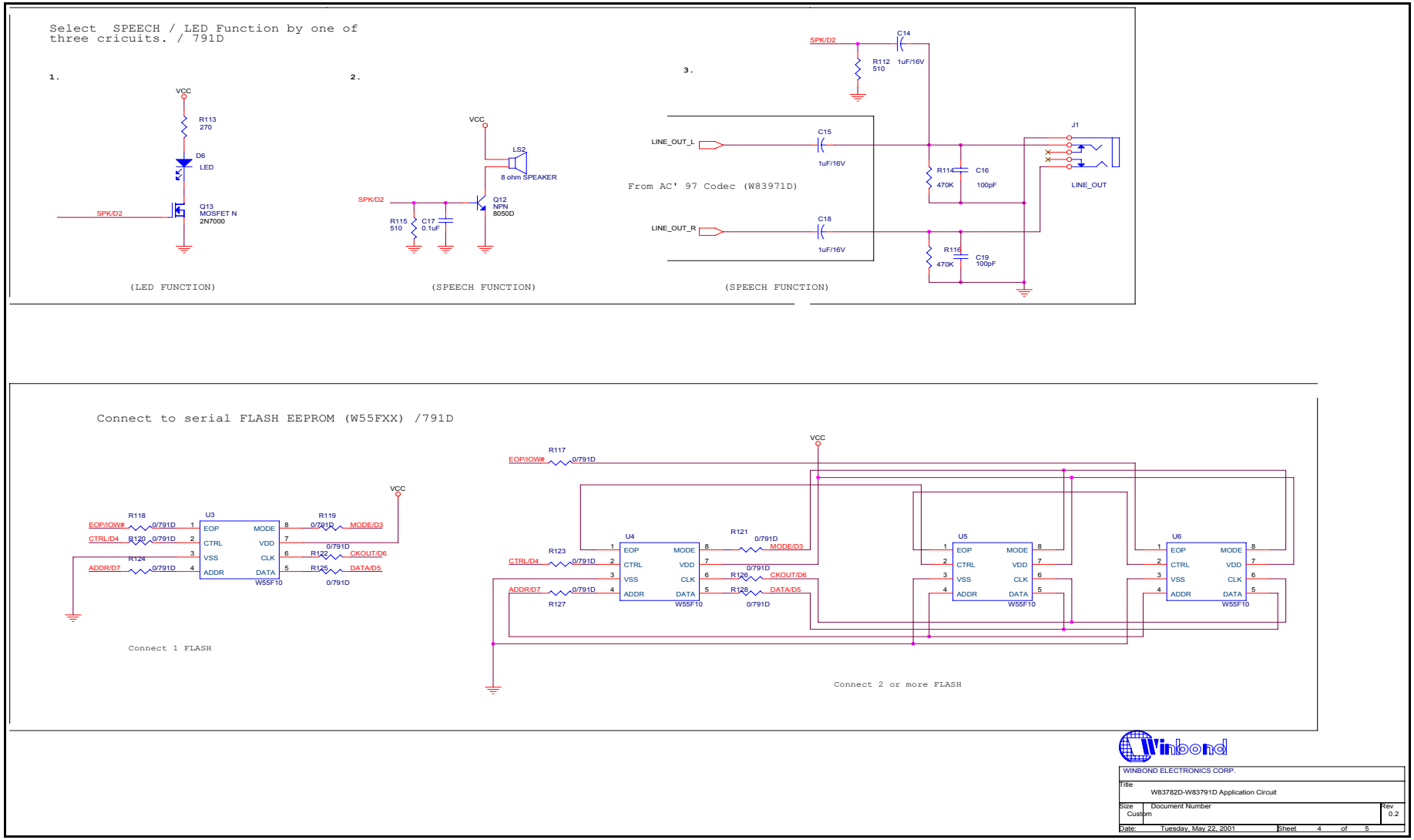
Date: Tuesday, May 22, 2001	Sheet 3 of 5	


Select SPEECH / LED Function by one of three cricuits. / 791D
1.
2.
3.
VCC
R113
270
D6
LED
Q13
MOSFET N
2N7000
SPK/D2
(LED FUNCTION)
LS2
8 ohm SPEAKER
Q12
NPN
8050D
R115
510
C17
0.1uF
(SPEECH FUNCTION)
C14
R112
510
1uF/16V
LINE_OUT_L
LINE_OUT_R
C15
C18
1uF/16V
From AC' 97 Codec (W83971D)
R114
470K
C16
100pF
R116
470K
C19
100pF
J1
LINE_OUT
(SPEECH FUNCTION)
Connect to serial FLASH EEPROM (W55FXX) /791D
U3
R118
R119
R120
R122
R124
R125
EOP/IOW#
CTRL/D4
ADDR/D7
MODE/D3
CKOUT/D6
DATA/D5
0/791D
EOP
CTRL
VSS
ADDR
MODE
VDD
CLK
DATA
W55F10
Connect 1 FLASH
R117
R121
R123
R126
R127
R128
U4
U5
U6
Connect 2 or more FLASH
WINBOND ELECTRONICS CORP.
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Custom
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of
5

REV	Decription
0.1	First Publication
0.15	Add FAN/PWMOUT4-5 circuit
0.16	Change R34 connect to 5VSB
0.17	1. Change R32/R33 value to 330 ohm 2. Modify R34 value as 220K ohm 3. Change SMI# (pin 44) circuit. This update is for B version.
0.2	Update Pin44 (SMI#/LEDOUT) circuit. This update is for C version.

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