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# W83L786R / W83L786G
# Nuvoton
# H/W Monitoring IC

## W83L786R

## Data Sheet Revision History

| | PAGES | DATES | VERSION | VERSION ON WEB | MAIN CONTENTS |
|---|---|---|---|---|---|
| 1 | P.8 | 09/29/03 | 0.6 | N/A | Pin 23, 24: from GPIO to VIN1,2 |
| 2 | P.14, P.18, P.55, P.59 | 10/22/04 | 0.7 | N/A | Add pin function description, functional description, electrical characteristics and top marking explanation |
| 3 | N/A | 03/31/06 | 0.8 | N/A | Add Pb-free package type; correct current mode temp. sensor inputs from one set to two sets |
| 4 | | | | | |
| 5 | | | | | |



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## *Table of Contents-*

## 1. GENERAL DESCRIPTION

W83L786R/G is an evolving product of W83L785R -- Nuvoton's most popular hardware monitoring IC, and intelligent fan controlling IC. Specifically designed for the graphic cards and barebone / mini systems, W83L786R/G can be used to monitor several critical hardware parameters of the system, including voltages, fan speeds, and temperatures, which are very important for the system to work stably and properly.

W83L786R/G provides one set of 5-bit, VRM 9.0 compatible VID that could be used for GPU/CPU overclocking. By hardware trapping could set up the starting VID value. The W83L786R/G can monitor up to 5 analog voltage inputs, 2 fan tachometer inputs, and 3 remote temperature sensors. Two of the temperature inputs could be connected to CPU/GPU thermal diode sensors, and the other remote temperature sensor could be performed by thermistors. Power-on fan_set configuration offers the function to choose one of the four duty cycles, 100%, 81%, 62%, 43%, as initial fan speed. 2 sets of PWM (Pulse Width Modulation) / DC (Direct Current) fan output for SMART FAN™ control – "Thermal Cruise™" mode and "SMART FAN™ II "mode. Under "Thermal Cruise™ "mode, temperatures of GPU and the system can be maintained within specific programmable ranges under the hardware control. Under "SMART FAN™ II" mode, the fan could be operated at the lowest possible speed for minimum acoustic noise, and the dynamic intelligent fan management could create the most quiet system environment and stable working performance. An 8-bit analog-to-digital converter (ADC) is built inside W83L786R/G. As for warning mechanism, W83L786R/G provides four pure hardware event pins for independent warning signals: VOLTAGE_FAULT#, FAN_FAULT#, TEMP_FAULT#, and INT#. All threshold values could be set for system protection without any timing delay. One bit power-on address selection is used to decide the address of the W83L786R/G over $I^2C$ serial bus interface. W83L786R/G also provides up to 14 optional multifunctional GPIO. Also, Watch Dog Timer ™ could set up reset time flexibly; facilitate hardware management and monitoring. W83L786R/G is powered by 3.3V.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper / preset range. The application software could be Nuvoton's Hardware Doctor™, Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable interrupts. For the spacing saving consideration of the Graphic cards and Notebook system, W83L786R/G is 28-pin SSOP package.

# 2. FEATURES

## 2.1 Monitoring Items

### 2.1.1 Temperature

- Measure the temperature with high accuracy.
- Two thermal diode sensor inputs (current mode) and one thermistor sensor input.
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items.

### 2.1.2 Voltage

- 5 voltage sensor inputs.
  --- Typically for Vcore, +3.3V (Power), RAM, AGP…etc.
- Five VID bits Intel VRM 9.0 compliant to set Vcore voltage for GPU overclocking.
- Watch Dog Timer with INT# output for overclocking failure recovery. (VID pins output control is also cleared by this INT#).
- Power on configuration for Vcore input.

### 2.1.3 Fan

- 2 sets of fan speed monitoring and controlling.
- 3D/2D application being used and transferring fan set to the most appropriate fan speed control.
- Fan set: power on configuration for fan speed at four rotation rate levels at 43%, 62%, 81%, and 100% duty cycle.
- Two DC/PWM fan output control.
- SMART FAN™ function compliant.

## 2.2 Actions Enabling

- Issue FAN_FAULT#, VOLTAGE_FAULT#, TEMP_FAULT#, and INT# signals to activate system protection.
- Warning signal pop-up in application software.

## 2.3 General

- Interface: I²C / SMBus control.
- 1 bit $I^2C$ address selection.
- Up to 14 GPIOs.
- Nuvoton hardware monitoring application software (Hardware Doctor™) support Windows 95 / 98 / 2000 / XP and Windows NT 4.0 / 5.0.
- 3.3V $V_{CC}$ operation.

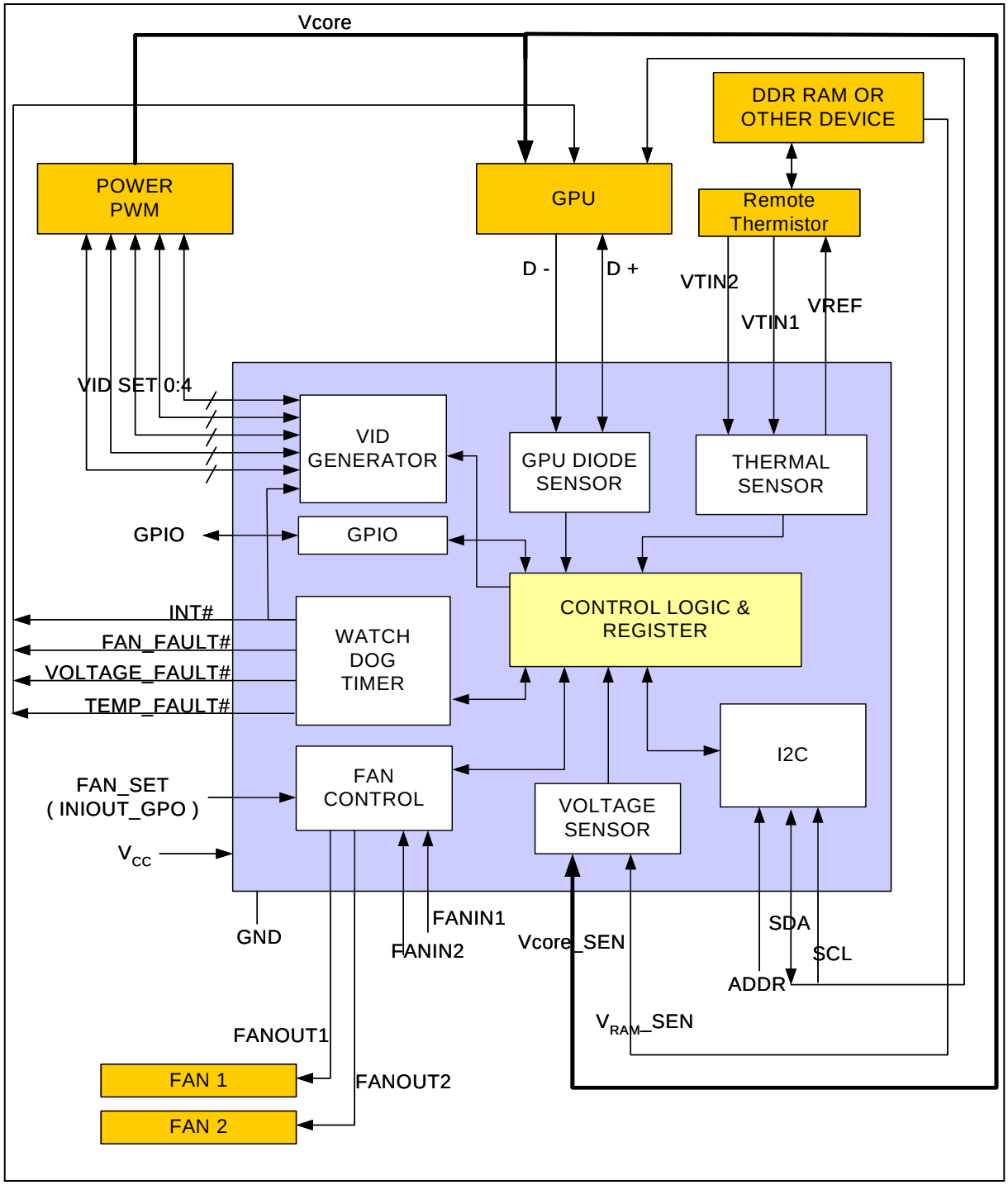
## 2.4 Package

- 28-pin SSOP (209mil).

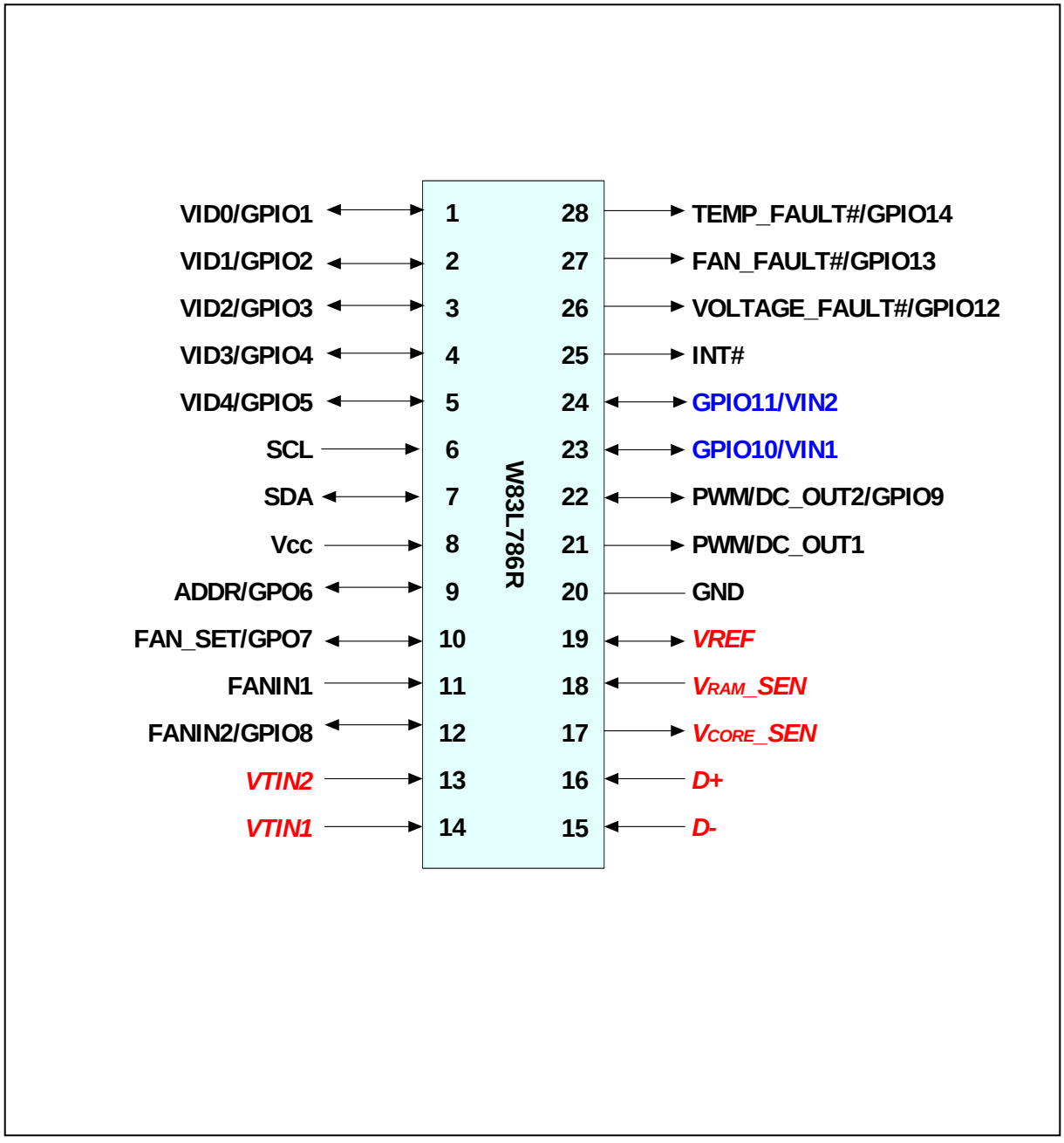
## 3. KEY SPECIFICATIONS

| | |
|---|---|
| ■ Voltage monitoring accuracy | ±3% (typ.) |
| ■ Monitoring temperature range | 0°C to +160°C |
| ■ Monitoring temperature accuracy | ± 3°C (max.) (@70°C) |
| ■ Supply voltage | 3.3V±10% |
| ■ Operating supply current | 2 mA typ. |
| ■ Power down supply current | 10 uA typ. |
| ■ ADC resolution | 8 Bits |

## 4. BLOCK DIAGRAM



## 5. PIN CONFIGURATION



## 6. PIN DESCRIPTION

| PIN TYPE | PIN ATTRIBUTE |
|---|---|
| $I/O_{12t}$ | TTL level bi-directional pin with 12 mA source-sink capability |
| $I/O_{12ts}$ | TTL level and schmitt trigger with 12 mA source-sink capability |
| $I/O_{8ts}$ | TTL level and schmitt trigger with 8 mA source-sink capability |
| $I/O_{6ts}$ | TTL level and schmitt trigger with 6 mA source-sink capability |
| $I/OD_{12ts}$ | TTL level and schmitt trigger open drain output with 12 mA sink capability |
| $OUT_{12}$ | Output pin with 12 mA source-sink capability |
| $OD_{12}$ | Open-drain output pin with 12 mA sink capability |
| AOUT | Output pin (Analog) |
| $IN_t$ | TTL level input pin |
| $IN_{ts}$ | TTL level input pin and schmitt trigger |
| AIN | Input pin(Analog) |

| PIN NAME | NO | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| VID0 / GPIO1 | 1 | $I/OD_{12ts}$ | Digital Input (Open drain). Voltage supply readouts from GPU. This value is read into the VID register.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| VID1 / GPIO2 | 2 | $I/OD_{12ts}$ | Digital Input (Open drain). Voltage supply readouts from GPU. This value is read into the VID register.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| VID2 / GPIO3 | 3 | $I/OD_{12ts}$ | Digital Input (Open drain). Voltage supply readouts from GPU. This value is read into the VID register.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| VID3 / GPIO4 | 4 | $I/OD_{12ts}$ | Digital Input (Open drain). Voltage supply readouts from GPU. This value is read into the VID register.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |

PIN description, continued.

| PIN NAME | NO | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| VID4 / GPIO5 | 5 | $I/OD_{12ts}$ | Digital Input (Open drain). Voltage supply readouts from GPU. This value is read into the VID register.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| SCL | 6 | $IN_{ts}$ | Digital Input (Open drain). SMBus serial clock input. Requires SMBus pull-up. |
| SDA | 7 | $I/OD_{12}$ | Digital I/O (Open drain). SMBus bidirectional serial data. Requires SMBus pull-up. |
| Vcc | 8 | POWER | Analog Input. Monitors +3.3V power supply. |
| ADDR / GPO6 | 9 | $IN_{TS}/OUT_{12}$ | Determines the SMBus device address.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| FAN_SET / GPO7 | 10 | $AIN/OUT_{12}$ | Determines the FAN initial speed.<br>General purpose Output function.<br>This multi-functional pin is programmable. |
| FANIN1 | 11 | $IN_{TS}$ | 0V to +3.3V amplitude fan tachometer input.(Default) |
| FANIN2 / GPIO8 | 12 | $IN_{TS}/OUT_{12TS}$ | 0V to +3.3V amplitude fan tachometer input.(Default) /<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| **VTIN2** | **13** | **AIN** | **Analog Input.** |
| **VTIN1** | **14** | **AIN** | **Analog Input. This pin could connect to thermister or thermal diode. Regard as anode connection if connected to thermal diode; share cathode with D-.** |
| **D-** | **15** | **AIN** | **Cathode Connection to GPU Thermal Diode.** |
| **D+** | **16** | **AIN** | **Anode Connection to GPU Thermal Diode.** |
| **$V_{CORE}$_SEN** | **17** | **AIN** | **Analog Input. Monitors GPU core voltage (0V-3V).** |

PIN description, continued.

| PIN NAME | NO | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| **$V_{RAM}$_SEN** | **18** | **AIN** | **Analog Input. Monitors RAM's voltage.** |
| **VREF** | **19** | **AOUT** | **Reference voltage.** |
| GND | 20 | GROUND | Ground pin for the W83L786R |
| PWM/DC OUT1 | 21 | $OD_{12}$/$OUT_{12}$/AOUT | Fan speed control output. This pin is default DC output level. It can be programmed as PWM output. |
| PWM/DC OUT2 / GPIO9 | 22 | $OD_{12}$ /AOUT/$IOD_{12TS}$ | Fan speed control output. This pin is default DC output level. It can be programmed as PWM output.<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| **VIN1/GPIO 10** | **23** | **AIN/$IOD_{12TS}$** | **Analog Input. Monitors voltage.**<br>**General purpose I/O function.** |
| **VIN2/GPIO11** | **24** | **AIN/$IOD_{12TS}$** | **Analog Input. Monitors voltage.**<br>**General purpose I/O function.** |
| INT# | 25 | $OD_{12}$ | System Interrupt. |
| VOLTAGE_FAULT# / GPIO12 | 26 | $OD_{12}$/$IOD_{12TS}$ | Active-Low output. This pin will be a logic LOW when the voltage exceeds its high/low limit. (Default)<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| FAN_FAULT# / GPIO13 | 27 | $OD_{12}$/$IOD_{12TS}$ | Active-Low output. This pin will be a logic LOW when the Fan1 or fan2 is abnormally stopped. (Default)<br>General purpose I/O function.<br>This multi-functional pin is programmable. |
| TEMP_FAULT# / GPIO14 | 28 | $OD_{12}$/$IOD_{12TS}$ | Active-Low output. This pin will be a logic LOW when the temperature of the system or GPU exceeds its limit. (Default)<br>General purpose I/O function.<br>This multi-functional pin is programmable. |

# 7. FUNCTIONAL DESCRIPTION

## 7.1 General Description

W83L786R/G provides 5 analog voltage inputs, 2 fan speed input monitoring and output controls which support both PWM (Pulse Width Modulation) fan control and DC (Direct Current) fan control, all of them being implemented with SMART FAN™ I and SMART FAN™ II, and 3 sets of thermal inputs for remote thermistors and GPU thermal diode sensor. W83L786R/G is I²C / SMBus interface compatible. 1 set of 5-bit VID input/output for processor VID table could be selected by hardware trapping for VRM9.0 specifications. Furthermore, the Watch Dog Timer will monitor every function and store the values to registers for comparison with preset ranges. If the monitored value exceeds the limit value, the interrupt status will be set to 1 and W83L786R/G will issue interrupt signals such as INT# and IRQ if not masked. W83L786R/G also provides software and hardware Watch Dog Timer to avoid system hang on.

## 7.2 Access Interface

W83L786R/G provides I²C Serial Bus for microprocessor to read/write internal registers, and the I²C address default value is 01011110b (Pin 9 pull high). If Pin 9 pulls low, the I²C address value is 01011100b.

## 7.3 The First Serial Bus Access Timing

(a) Serial bus writes to internal address register followed by the data byte

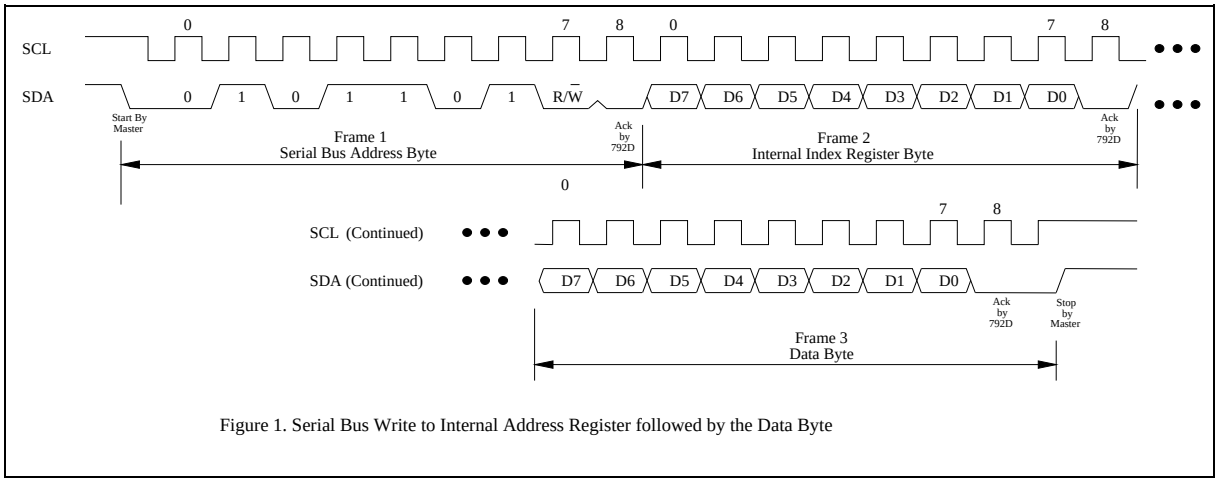



Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

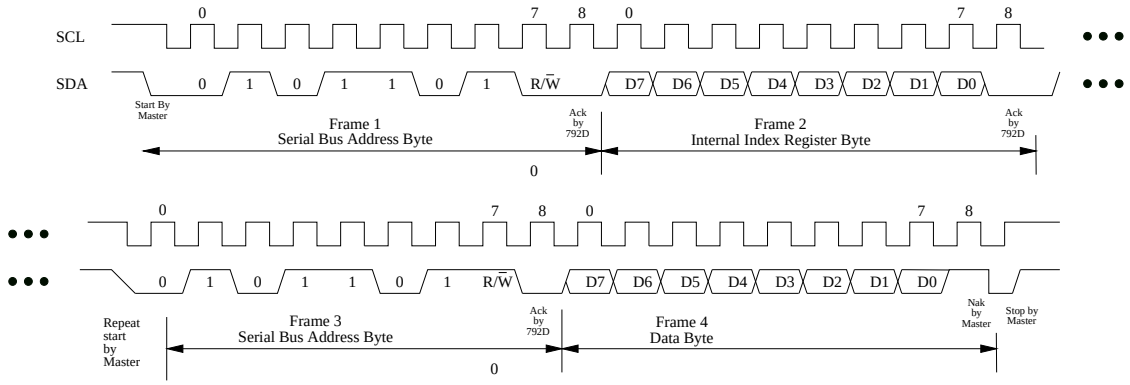



Figure 2. Serial Bus Read from Internal Address Register

## 7.4 Analog Inputs

The maximum input voltage of the analog pin is 2.048V because the 8-bit ADC has the 2mv LSB. Actually, the application of the voltage monitoring would most often be connected to power suppliers. The input voltage lower than 2.048V could directly connect to the analog inputs. The inputs voltage higher than 2.048V should be reduced by external resistors so as to meet the input range. This is shown in Figure 3.

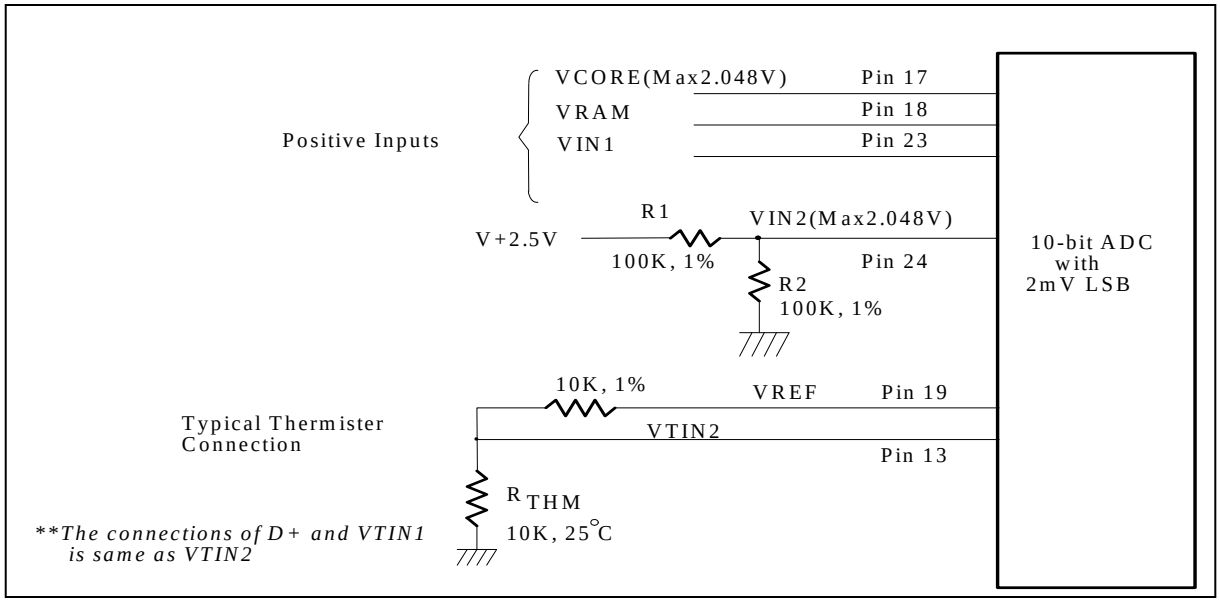



Figure 3

### 7.4.1 Voltage Input can not be over 2.048V

The input voltage Vcore , Vram, VIN1 and VIN2 can be expressed as following equation:

$$VIN2 = V_{+2.5V} \times \frac{R_2}{R_1 + R_2}$$ . $V_{+2.5V}$ is +2.5V inputs.

The value of R1 and R2 can be selected to 100K Ohms and 100K Ohms, respectively, when the input voltage is 2.5V. The node voltage of VIN2 can be subject to less than 2.048V for the maximum input range of the 8-bit ADC. The pin 8 is connected to the power supply VCC with +3.3V. There are two functions in this pin with 3.3V: the first function is to supply internal analog power of W83L786R/G and the second function is to connect this pin to internal serial resistors to monitor the +3.3V voltage. The values of two serial resistors are 20K ohms and 40K ohms so that input voltage to ADC is 1.1V which is less than 2.048V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{20K\Omega}{20K\Omega + 40K\Omega} \cong 1.1V$$

where VCC is set to 3.3V.

### 7.4.2 Voltage Fault (VOLTAGE_FAULT #)

W83L786R/G provides a good protection for voltage. Set Pin 26 (VOLTAGE_FAULT#) to monitor voltage. When Vcore (Pin17), Vram (Pin18), VIN1 (Pin23), VIN2 (Pin24), or VCC (Pin8) voltage exceeds high or low voltage limit in VR2B ~ VR34, Pin 26 VOLTAGE_FAULT# will be asserted (Figure 4).

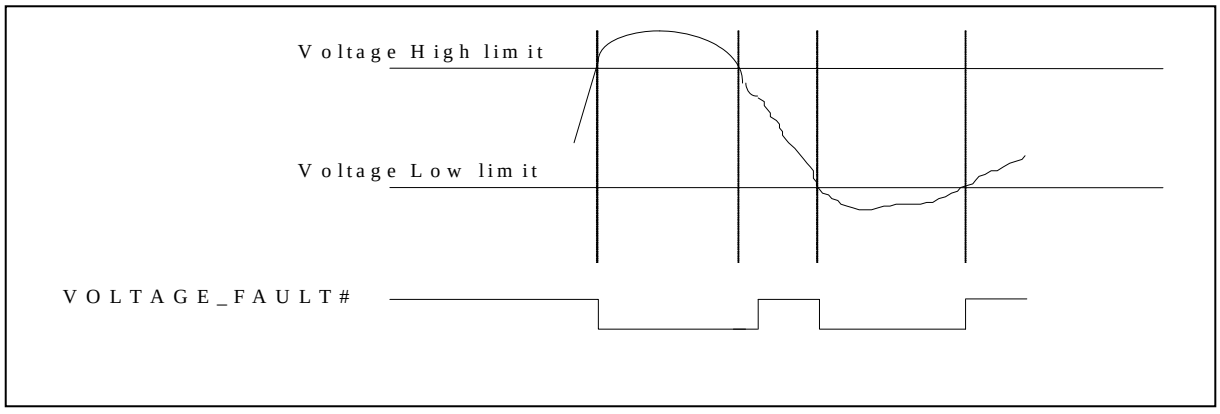



Figure 4. Voltage Fault

## 7.5 Temperature Measurement Machine

The temperature data format is 8-bit unsigned for thermal sensor. The 8-bit temperature data can be obtained by reading the VR [25h], VR [26h] or VR [27h]. The format of the temperature data is shown in Table 1.

| TEMPERATURE | 8-BIT DIGITAL OUTPUT | |
|---|---|---|
| | 8-BIT BINARY | 8-BIT HEX |
| +160°C | 1010,0000 | A0h |
| +25°C | 0001,1001 | 19h |
| +2°C | 0000,0010 | 02h |
| +1°C | 0000,0001 | 01h |
| +0°C | 0000,0000 | 00h |

**Table 1**

### 7.5.1 Monitor Temperature from Thermistor

W83L786R/G can connect two thermistors and one thermal diode sensor to measure three different environment temperatures. The specification of thermistor should be considered to (1) β value is 3435 K, and (2) resistor value is 10K ohms at 25°C. In the Figure 3, the themistor is connected by a serial resistor with 10K Ohms, and then connect to $V_{REF}$ (pin 19).

### 7.5.2 Monitor Temperature from Thermal Diode

W83L786R/G can alternate the thermistor to thermal diode interface and the circuit connection is shown as Figure 5. The pin of D- is connected to power supply ground (GND) and the pin D+ is connected to pin D+ or VTIN1 in the W83L786R/G. The bypass capacitor C=2200pF should be added to filter the high frequency noise.

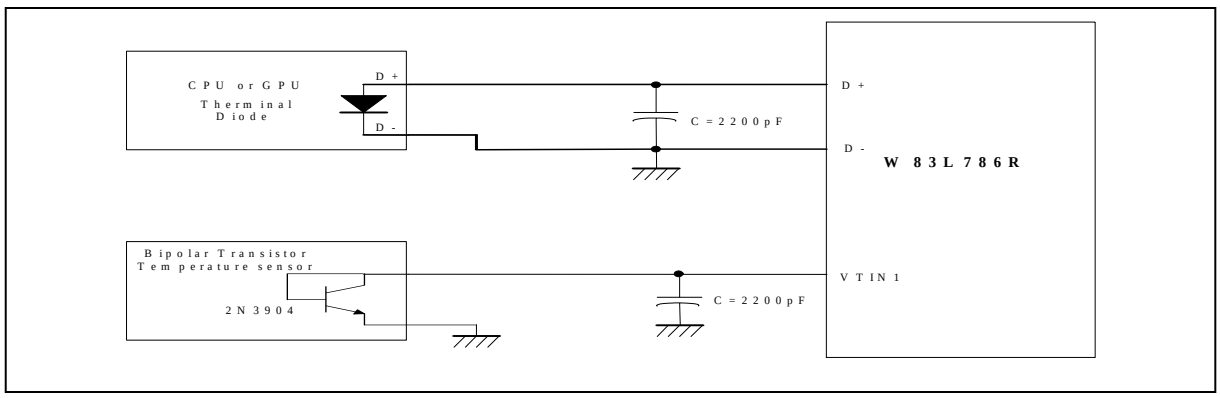



Figure 5

### 7.5.3 Temperature Fault (TEMP_FAULT #)

W83L786R/G provides a good protection for temperature fault. Set Pin 28 (TEMP_FAULT#) to monitor temperature. When D+-D- (Pin16, 15), VTIN1 (Pin14), or VTIN2 (Pin13) temperature exceeds temperature fault limit in VR35, VR37, or VR39, Pin 28 TEMP_FAULT# will be asserted (Figure 6).

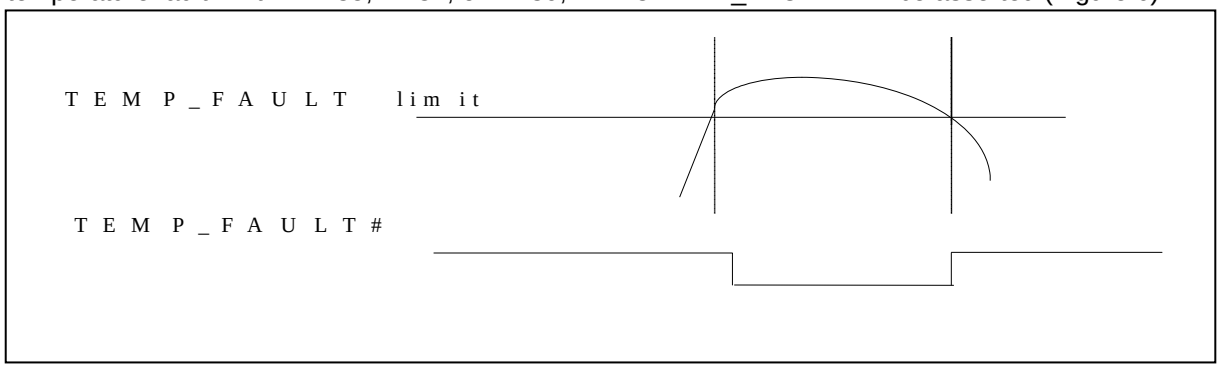



Figure 6. TEMP_FAULT

## 7.6 FAN Speed Count and FAN Speed Control

### 7.6.1 Fan Speed Count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over VCC. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown in Figure 7.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register VR28 or VR29, and the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR54.bit0~2, bit4~6 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. Table 2 is an example for the relation of divisor, RPM, and count.

| DIVISOR | NOMINAL RPM | TIME PER REVOLUTION | COUNTS | 70% RPM | TIME FOR 70% |
|---|---|---|---|---|---|
| 1 | 8800 | 6.82 ms | *153* | 6160 | 9.74 ms |
| **2 (default)** | 4400 | 13.64 ms | *153* | 3080 | 19.48 ms |
| 4 | 2200 | 27.27 ms | *153* | 1540 | 38.96 ms |
| 8 | 1100 | 54.54 ms | *153* | 770 | 77.92 ms |
| 16 | 550 | 109.08 ms | *153* | 385 | 155.84 ms |
| 32 | 275 | 218.16 ms | *153* | 192 | 311.68 ms |
| 64 | 137 | 436.32 ms | *153* | 96 | 623.36 ms |
| 128 | 68 | 872.64 ms | *153* | 48 | 1246.72 ms |

**Table 2**

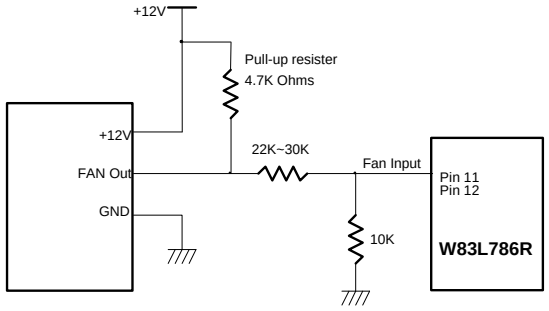



Figure 7-1. Fan with Tach Pull-Up to +12V, or Totern-Pole Output and Register Attenuator

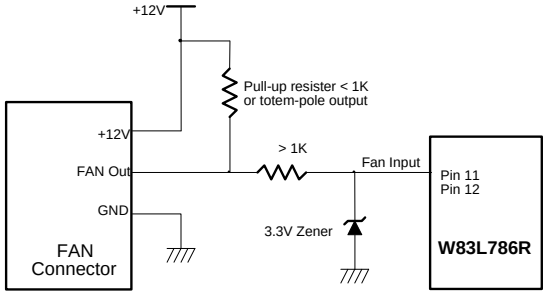



Figure 7-2. Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

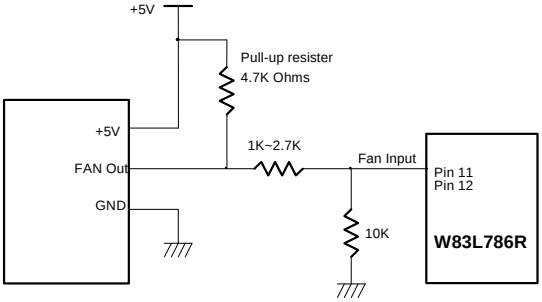



Figure 7-3. Fan with Tach Pull-Up to +5V, or Totern-Pole Output and Register Attenuator

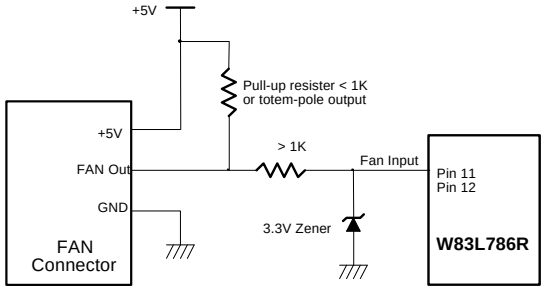


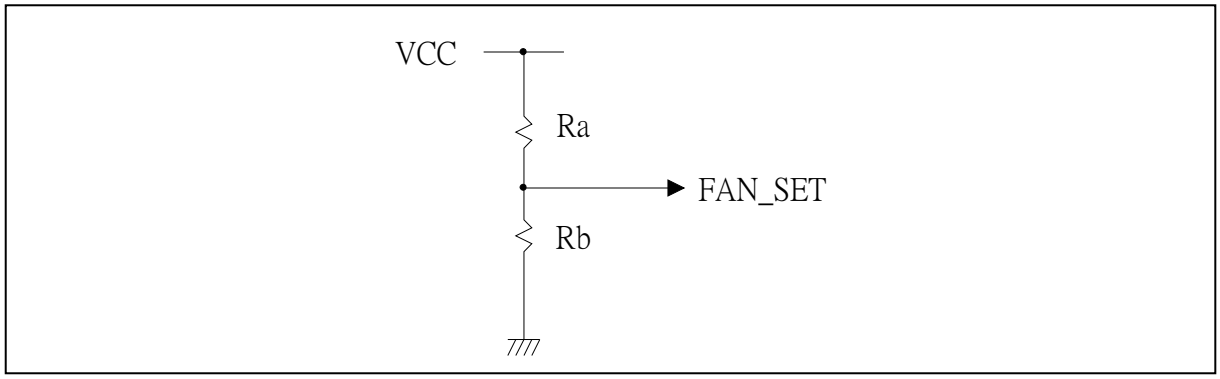

Figure 7-4. Fan with Tach Pull-Up to +5V, or Totem-Pole Putput and Zener Clamp

### 7.6.2 Fan Speed Control

W83L786R/G provides two sets for PWM/DC fan speed control. The duty cycle of PWM or the output voltage of DC can be programmed by a 4-bit register. There are four mode to control fan speed which are set by programming CR80 [3:2] and CR [5:4], and default are FAN_SET mode.

#### 7.6.2.1. Default Fan Speed Setting

There is a pin to set the default value for fan speed control by adjusting external serial resistors. After power up, the default value will be stored in CR90 (FAN_SET mode). The figure and table are shown below.




| SECTION | FAN SPEED RATE | RA | RB |
|---|---|---|---|
| **3** | 100% | 9.1K | × |
| **2** | 81% | 4.7K | 9.1K |
| **1** | 62% | 9.1K | 4.7K |
| **0** | 43% | × | 9.1K |

Figure 8 OFFSET Setting

#### 7.6.2.2. PWM Mode

$$\text{Duty}-\text{cycle}(\%)=\frac{\text{Programmed 4-bit Register Value}}{16}\times 100\%$$

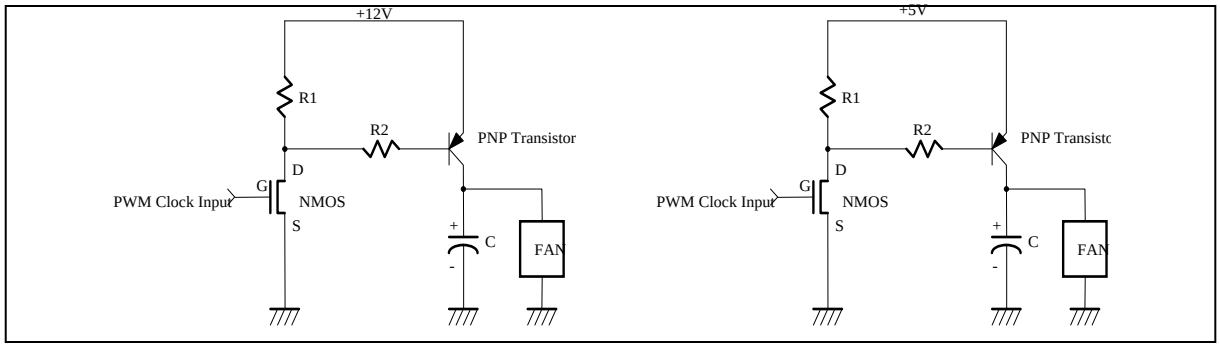



Figure 9

### 7.6.2.3. DC Mode

W83L796R/G has a 4-bit DAC, which produces 0 to 3.3 voltages DC output that provides maximum 2 sets for fan speed control. The analog output can be programmed in the CR 81, and CR 87 (manual mode). The expression of output voltage can be represented as follows,

$$\text{OUTPUT Voltage} = \text{VCC} \times \frac{\text{Programmed 4 - bit Register Value}}{16}$$

The application circuit is shown as follow,

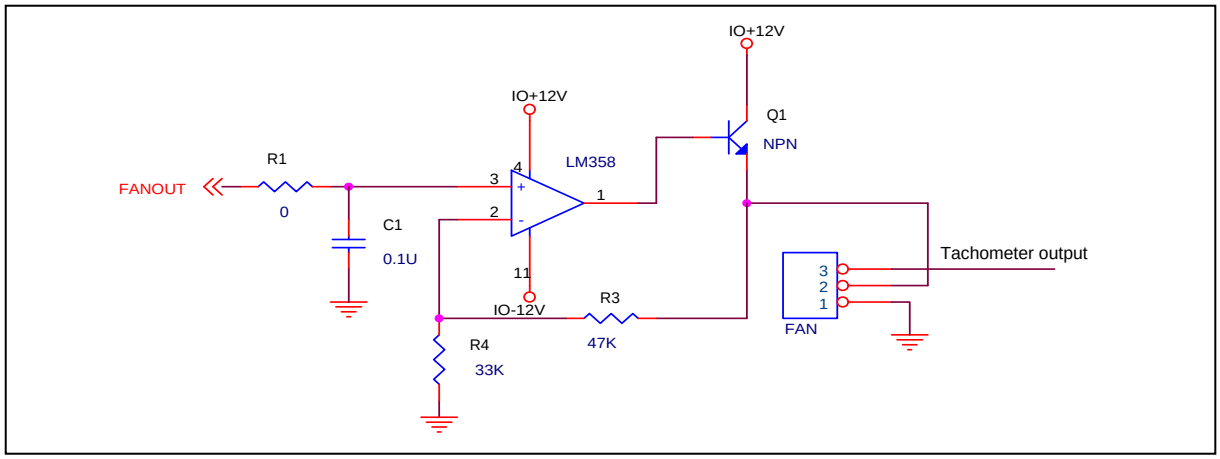



Figure 10

Must be take care when choosing the OP-AMP and the transistor. The OP-AMP is used for amplify the 5V range of the DC output up to 12V. The transistor should has a suitable $\beta$ value to avoid its base current pulling down the OP-AMP 's output and gain the common current to operate the fan at fully speed. (For more cost and effort efficient solution please refer to W83391TS/QS – the DC fan pre-driver that could provide up to 24V gate voltage for external N-channel MOSFET driving)

### 7.6.3 SMART FANTM I Control

W83L786R/G supports two sets SMART FAN™ I function and mapping to D+,D- (PWM/DC_OUT1), VTIN1 (PWM/DC_OUT2) . If CR80 [3:2] or CR80 [5:4] set to 2'b10, Fan1 or Fan2 will enable SMART FAN™ I function.

At this mode, W83L786R/G provides the SMART FAN™ system to automatically control fan speed to keep the temperatures of CPU and the system within specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS and the fan speed will be lowered as long as the current temperature remains below the setting value. Once the temperature exceeds the high limit (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its full speed but the temperature still exceeds the high limit (ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but still above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target range (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset stop value until the temperature exceeds the low limit.

Figure 11-1, 11-2 gives an illustration of Thermal Cruise Mode.

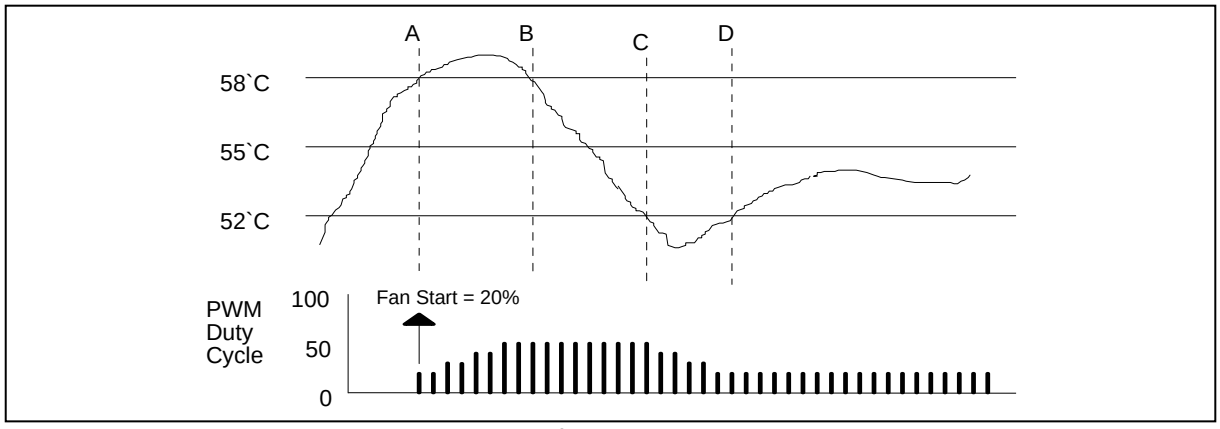



Figure 11-1

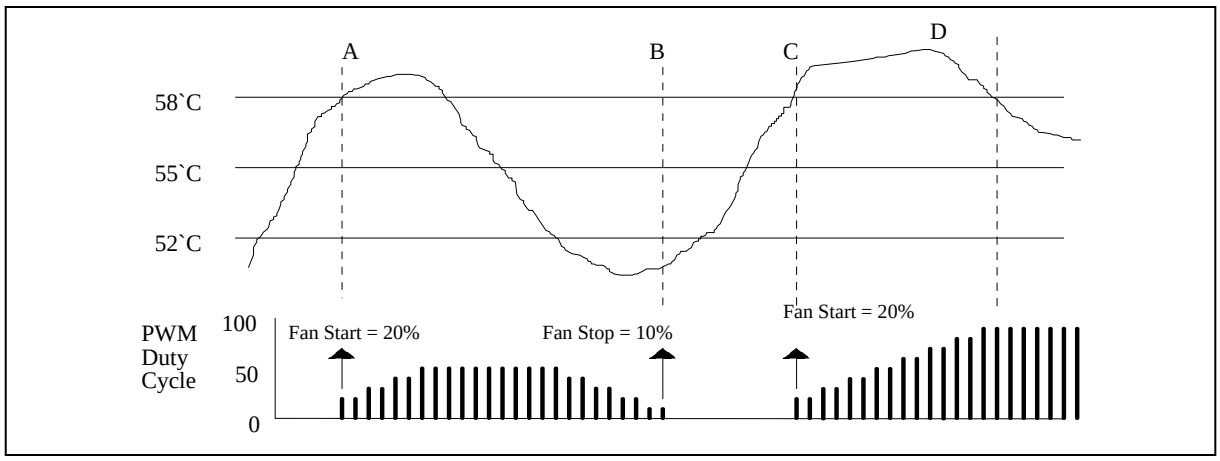



Figure 11-2

Of course, SMART FAN™ control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

### 7.6.4 SMART FANTM II Control

W83786R/G provide 4 temperature points each can automatically control PWM or DC fan mode. Each temperature maps different fan out level, the relationship is shown as follows:

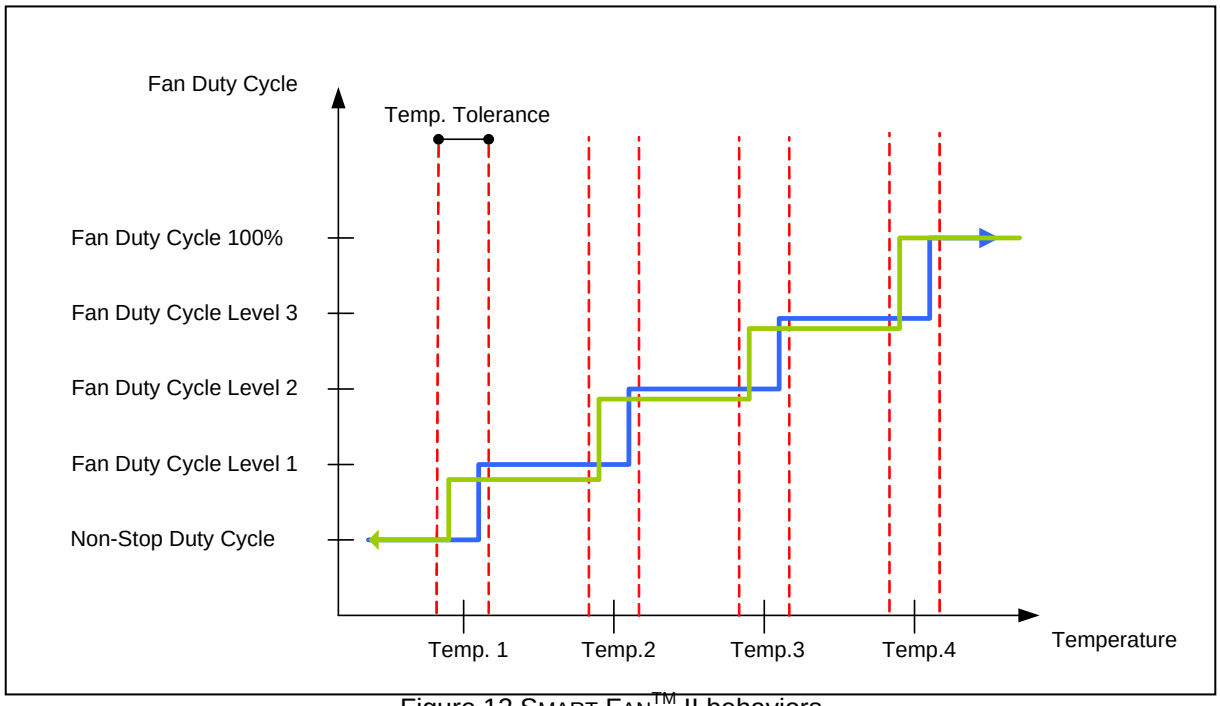



Figure 12 SMART FAN™ II behaviors

The SMART FAN™ II, a new innovation of Nuvoton, is specifically designed to operate fans at the lowest possible speed so as to minimize acoustic noise. As the figure shown above, it is clear that SMART FAN™ II describes a relationship between Fan PWM Duty Cycle/DC Level and temperature. Users can program CR [84h] to enable SMART FAN™ II mode. SMART FAN™ II registers allow users to define suitable fan output levels to improve acoustic noise, power consumption and reliability issues regarding to specific fan.

Each fan has 4 duty cycle registers and 4 temperature point registers to setup the relation between fan output and temperature. Tolerance registers CR [87h], CR [97h] are used to postpone the response of fan output and avoid fan output throttles at each temperature point because fan throttling might produce some undesired noise.

The mechanism of SMART FAN™ II is described as follows:

(1) At first, the fan speed operates at Non-Stop Duty Cycle, and keeps constant while temperature rises. When rising temperature hits critical Temp.1, fan speed remains unchanged. If the temperature keeps on rising and finally hits the upper edge of Temp. Tolerance of Temp.1, it triggers the fan speed change mechanism and fan speed jumps from Non-Stop Duty Cycle to Fan Duty Cycle Level 1.

(2) Fan speed remains constant at Fan Duty Cycle Level 1 even though the monitored temperature hits Temp.2.

(3) Fan speed will directly jump from Fan Duty Cycle Level 1 to Fan Duty Cycle Level 2 while the monitored temperature hits the upper edge of Temp. Tolerance of Temp.2.

(4) Same mechanism happens between Temp.3 and Temp.4.

(5) If the monitored temperature between Temp.3 and Temp.4, for example, begins to fall, the fan will keep its speed at Fan Duty Cycle Level 3, which is a constant.

(6) If the monitored temperature keeps on falling, the fan speed still remains the same unless the temperature hits the lower edge of Temp. Tolerance of Temp.3.

(7) Once the monitored temperature hits the lower edge of Temp. Tolerance of Temp.3, the fan speed reduces directly from Fan Duty Cycle Level 3 to Fan Duty Cycle Level 2, and keeps the same speed until the temperature hits the next lower edge of Temp. Tolerance.

| REGISTER | TEMP 1 – FAN1 | TEMP 2 – FAN2 | TEMP 3 – FAN3 |
|---|---|---|---|
| Non-Stop Duty Cycle | CR[88h] b3:b0 | CR[89h] b3:b0 | CR[98h] b3:b0 |
| Duty Level 1 | CR[88h] b7:b4 | CR[89h] b7:b4 | CR[98h] b7:b4 |
| Duty Level 2 | CR[E0h] b7:b4 | CR[E1h] b7:b4 | CR[E2h] b7:b4 |
| Duty Level 3 | CR[E0h] b3:b0 | CR[E1h] b3:b0 | CR[E2h] b3:b0 |
| Temp Point 1 | CR[85h] b7:b0 | CR[86h] b7:b0 | CR[96h] b7:b0 |
| Temp Point 2 | CR[E3h] b7:b0 | CR[E6h] b7:b0 | CR[E9h] b7:b0 |
| Temp Point 3 | CR[E4h] b7:b0 | CR[E7h] b7:b0 | CR[EAh] b7:b0 |
| Temp Point 4 | CR[E5h] b7:b0 | CR[E8h] b7:b0 | CR[EBh] b7:b0 |
| Tolerance | CR[87h] b3:b0 | CR[87h] b7:b4 | CR[97h] b3:b0 |

### 7.6.5 Fan Fault (FAN_FAULT #)

W83L786R/G provides a good protection for fan speed. Set Pin 27 (FAN_FAULT#) to monitor fan speed. When FANIN1 (Pin11) or FANIN2 (Pin12) exceeds fan count high limit in VR3B or VR3C. Pin27 FAN_FAULT# will be asserted (Figure 13).

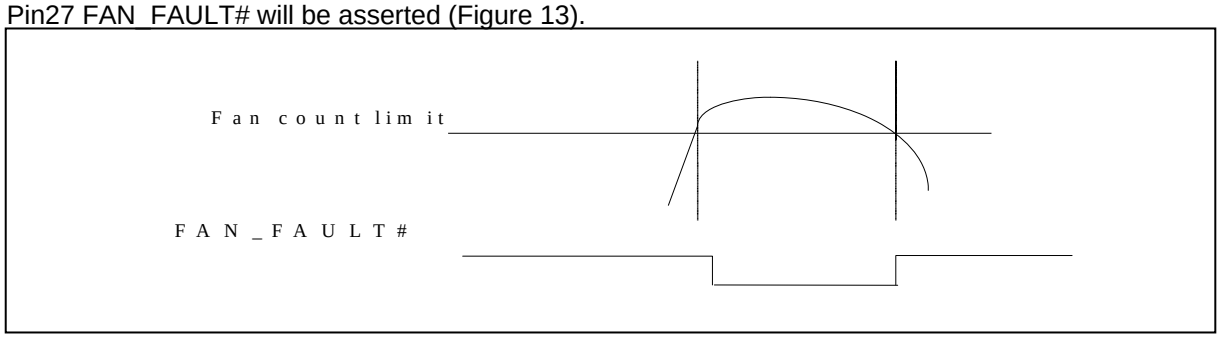



Figure 13. FAN_FAULT

## 7.7 Fault Signal—INT#

### 7.7.1 Temperature

**Pin INT# for temperature has 3 modes.**

#### 7.7.1.1. Comparator Interrupt Mode

Temperature exceeding $T_O$ causes an interrupt and this interrupt will be reset when reading all of the Interrupt Status Registers. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_{HYST}$, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding $T_O$ and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below $T_{HYST}$. (Figure 14-1)

#### 7.7.1.2. Two-Times Interrupt Mode

Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_{HYST}$, the interrupt will not occur. (Figure 14-2)

#### 7.7.1.3. One-Time Interrupt Mode

Temperature exceeding $T_O$ causes an interrupt and then temperature going below $T_{HYST}$ will not cause an interrupt. Once an interrupt event has occurred by exceeding $T_O$, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding $T_O$. (Figure 14-3)

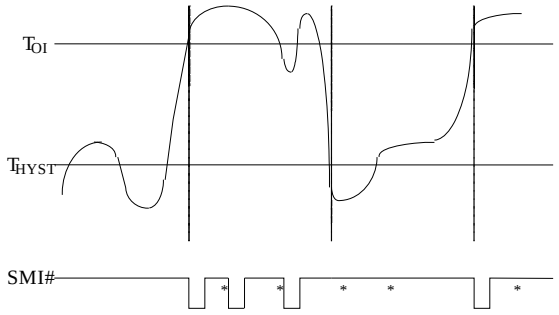
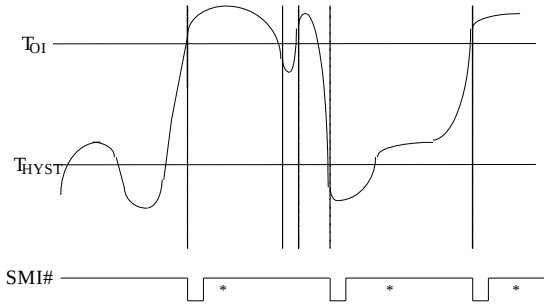
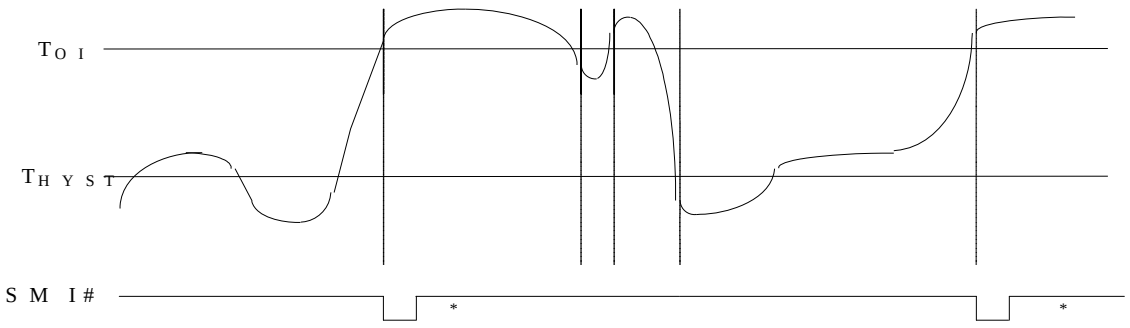



Figure 14-1. Comparator Interrupt Mode




*Interrupt Reset when Interrupt Status Registers are read

Figure 14-2. Two-Times Interrupt Mode




*Interrupt Reset when Interrupt Status Registers are read

Figure 14-3. One-Time Interrupt Mode

### 7.7.2 Voltage

INT# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 15-1)

### 7.7.3 Fan

INT# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit (set at value ram index 3Bh and 3Ch), will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 15-2)

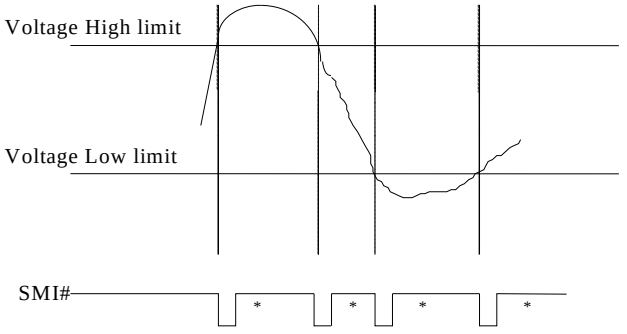



Figure 15-1. Voltage SMI# Mode

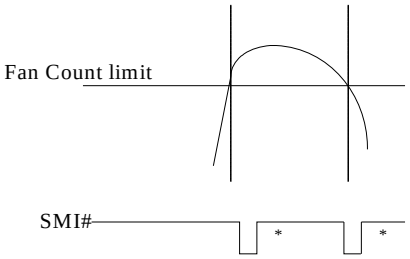



Figure 15-2. Fan SMI# Mode

*Interrupt Reset when Interrupt Status Registers are read

# 8. CONTROL AND STATUS REGISTER

## 8.1 Configuration Register - Index 40h

Power on default [7:0] = 0000, 0001b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | Software Reset | Read/Write | A one restores power on default value to all registers except the Serial Bus Address register. This bit is itself clear when it is set. |
| 6-5 | Reserved | Read/Write | Reserved |
| 4 | SOFT_PWDN | Read/Write | **Software Power Down.** Set to 1 to power down this chip, but $I^2C$ interface is still working. |
| 3 | Reserved | Read/Write | Reserved |
| 2 | EN_VRM9_VCORE | Read/Write | A one enable VRM9.0 function for VCORE channel |
| 1 | INT# Main Mask | Read/Write | A one disables the INT# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit. |
| 0 | START | Read/Write | A one enables startup of monitoring operations; a zero puts the part in standby mode.<br>***Note:*** *The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.* |

## 8.2 INT# Status Register 1 - Index 41h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | TEMP2_STS | Read Only | A one indicates a High or Low limit has been exceeded from temperature sensor 2 (VTIN2). This bit is cleared when this register is read. |
| 6 | TEMP1_STS | Read Only | A one indicates a High or Low limit has been exceeded from temperature sensor 1 (VTIN1). This bit is cleared when this register is read. |
| 5 | TEMP0_STS | Read Only | A one indicates a High or Low limit has been exceeded from temperature sensor 0 (D+_D-). This bit is cleared when this register is read. |
| 4 | VIN2_STS | Read Only | A one indicates a High or Low limit has been exceeded. (VIN2) This bit is cleared when this register is read. |

INT# Status Register 1 - Index 41h , continued.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 3 | VIN1_STS | Read Only | A one indicates a High or Low limit has been exceeded. (VIN1) This bit is cleared when this register is read. |
| 2 | VCC_STS | Read Only | A one indicates a High or Low limit has been exceeded. (VCC, +3.3V) This bit is cleared when this register is read. |
| 1 | VRAM_STS | Read Only | A one indicates a High or Low limit has been exceeded. (VRAM) This bit is cleared when this register is read. |
| 0 | VCORE_STS | Read Only | A one indicates a High or Low limit has been exceeded. (VCORE) This bit is cleared when this register is read. |

## 8.3 INT# Status Register 2 - Index 42h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-2 | Reserved | Read Only | Reserved. |
| **1** | **FAN2_STS** | **Read Only** | **A one indicates the fan count limit has been exceeded. This bit is cleared when this register is read.** |
| **0** | **FAN1_STS** | **Read Only** | **A one indicates the fan count limit has been exceeded. This bit is cleared when this register is read.** |

## 8.4 INT# Mask Register 1 - Index 43h

Power on default <7:0> = **1101**, **111**0 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | MAK_T2_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (Temperature 2) |
| 6 | MSK_T1_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (Temperature 1) |
| 5 | MSK_T0_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (Temperature 0) |
| **4** | **MSK_VIN2_INT** | **Read/Write** | **A one disables the corresponding interrupt status bit for SMI# interrupt. (VIN2)** |
| **3** | **MSK_VIN1_INT** | **Read/Write** | **A one disables the corresponding interrupt status bit for SMI# interrupt. (VIN1)** |
| 2 | MSK_VCC_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (VCC, +3.3V) |
| 1 | MSK_VRAM_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (VRAM) |
| 0 | MSK_VCORE_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (VCORE) |

## 8.5 INT# Mask Register 2 - Index 44h

Power on default <7:0> = 1111, 1110 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-2 | Reserved | Read/Write | Reserved. |
| 1 | MSK_FAN2_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (Fan 2 speed counter) |
| 0 | MSK_FAN1_INT | Read/Write | A one disables the corresponding interrupt status bit for SMI# interrupt. (Fan 1 speed counter) |

## 8.6 Watch Dog Timer Register I - Index 45h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | Reserved | Read/write | Reserved. |
| 3 | VID_WDT_TIMEOUT | Read/write | A one indicates Watch Dog Timer has been time-out.<br>It can be write from "1" to "0" only. |
| 2 | EN_VID_WDT | Read/write | <1> - Enable WDT |
| 1-0 | VID_WDT_CLK | Read/write | ***<00h> - 1Hz (1000ms)***<br>***<01h> - 10Hz (100ms)***<br>***<10h> - 100Hz (10ms)***<br>***<11h> - 1KHz (1ms)*** |

## 8.7 Watch Dog Timer Register II - Index 46h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | VID_WDT | Read/write | Watch Dog Timer Register<br><7:0> Read this register means how much time left that Watch Dog Timer will be time-out.<br>Write this register to set a time into Watch Dog Timer.<br>Write 00h means disable this function.<br>The Watch Dog Timer unit are set by CR45 bit 1~0.<br>Pin INT# generates a low pulse when Watch Dog Timer time-out event occurs. |

## 8.8 GPIO/GPO Function Enable Control Register - Index 47h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | EN_GPIO14 | Read/Write | **Pin 28 Function Select.**<br><0> - Function of Pin 28 is TEMP_FAULT#.<br><1> - Function of Pin 28 is GPIO14. |
| 6 | EN_GPIO13 | Read/Write | **Pin 27 Function Select.**<br><0> - Function of Pin 27 is FAN_FAULT#.<br><1> - Function of Pin 27 is GPIO13. |
| 5 | EN_GPIO12 | Read/Write | **Pin 26 Function Select.**<br><0> - Function of Pin 26 is VOLTAGE_FAULT#.<br><1> - Function of Pin 26 is GPIO12. |
| **4** | **EN_GPIO11** | **Read/Write** | **Pin 24 Function Select.**<br>**<0> - Function of Pin 24 is VIN2.**<br>**<1> - Function of Pin 24 is GPIO11.** |
| **3** | **EN_GPIO10** | **Read/Write** | **Pin 23 Function Select.**<br>**<0> - Function of Pin 23 is VIN1.**<br>**<1> - Function of Pin 23 is GPIO10.** |
| 2 | EN_GPIO9 | Read/Write | **Pin 22 Function Select.**<br><0> - Function of Pin 22 is PWM/DC_OUT2.<br><1> - Function of Pin 22 is GPIO9. |
| 1 | EN_GPIO8 | Read/Write | **Pin 12 Function Select.**<br><0> - Function of Pin 12 is FANIN2.<br><1> - Function of Pin 12 is GPIO8. |
| **0** | **EN_GPO6&7** | **Read/Write** | **Enable GPO6 & GPO7 Function of Pin 9 & Pin10.**<br>**<0> - Functions of GPO6 & GPO7 are disabled.**<br>**<1> - Functions of GPO6 & GPO7 are enabling.** |

## 8.9 VID0-4/GPIO1-5 I/O Mode Control Register - Index 48h

Power on default [7:0] = 0000, 0000 b

The VxGPIOy_MOD set the I/O mode of VxGPIOy. Their default states are input mode. When set them to output mode, we can program PWM device to adjust the GPU's Vcore. If Watch Dog Timer even occur after we programmed the VxGPIOy to adjust GPU's Vcore, the VxGPIOy_MOD are set to their default state –input mode. At that time, GPU's Vcore is set to default value.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-5 | Reserved | Read/write | Reserved. |
| 4 | V4GPIO5_MOD | Read/Write | **VID4/GPIO5 I/O Mode Select.**<br><0> - V4GPIO5 are input ports.<br><1> - V4GPIO5 are output ports. |
| 3 | V3GPIO4_MOD | Read/Write | **VID3/GPIO4 I/O Mode Select.**<br><0> - V3GPIO4 are input ports.<br><1> - V3GPIO4 are output ports. |
| 2 | V2GPIO3_MOD | Read/Write | **VID2/GPIO3 I/O Mode Select.**<br><0> - V2GPIO3 are input ports.<br><1> - V2GPIO3 are output ports. |
| 1 | V1GPIO2_MOD | Read/Write | **VID1/GPIO2 I/O Mode Select.**<br><0> - V1GPIO2 are input ports.<br><1> - V1GPIO2 are output ports. |
| 0 | V0GPIO1_MOD | Read/Write | **VID0/GPIO1 I/O Mode Select.**<br><0> - V0GPIO1 are input ports.<br><1> - V0GPIO1 are output ports. |

## 8.10 GPIO8-14 I/O Mode Control Register - Index 49h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | Reserved | Read/write | Reserved. |
| 6 | GPIO14_MODE | Read/Write | **GPIO14 I/O Mode Select.** (Only for GPIO function of Pin 28 is enabled.)<br><0> - GPIO14 is an input port.<br><1> - GPIO14 is an output port. |
| 5 | GPIO13_MODE | Read/Write | **GPIO13 I/O Mode Select.** (Only for GPIO function of Pin 27 is enabled.)<br><0> - GPIO13 is an input port.<br><1> - GPIO13 is an output port. |

GPIO8-14 I/O Mode Control Register - Index 49h, continued.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 4 | GPIO12_MODE | Read/Write | **GPIO12 I/O Mode Select.** (Only for GPIO function of Pin 26 is enabled.)<br><0> - GPIO12 is an input port.<br><1> - GPIO12 is an output port. |
| 3 | GPIO11_MODE | Read/Write | **GPIO11 I/O Mode Select.**<br><0> - GPIO11 is an input port.<br><1> - GPIO11 is an output port. |
| 2 | GPIO10_MODE | Read/Write | **GPIO10 I/O Mode Select.**<br><0> - GPIO10 is an input port.<br><1> - GPIO10 is an output port. |
| 1 | GPIO9_MODE | Read/Write | **GPIO9 I/O Mode Select.** (Only for GPIO function of Pin 22 is enabled.)<br><0> - GPIO9 is an input port.<br><1> - GPIO9 is an output port. |
| 0 | GPIO8_MODE | Read/Write | **GPIO8 I/O Mode Select.** (Only for GPIO function of Pin 12 is enabled.)<br><0> - GPIO8 is an input port.<br><1> - GPIO8 is an output port. |

## 8.11 GPO6-7 & VID0-4/GPIO1-5 Output Data Register - Index 4Ah

Power on default [7:0] = 000P, PPPP b (P: power on trapping)

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | Reserved | Read/write | Reserved. |
| 6 | GPO7_VAL | Read/Write | ***GPO7 Value. Set the output value of GPIO7 pin.*** |
| 5 | GPO6_VAL | Read/Write | ***GPO6 Value. Set the output value of GPIO6 pin.*** |
| 4 | V4GPIO5_VAL | Read/Write | **V4GPIO5 Value.** Set the output value of VID4/GPIO5 pin. Reading this bit will return ***the output value of GPIO5.*** |
| 3 | V3GPIO4_VAL | Read/Write | **V3GPIO4 Value.** Set the output value of VID3/GPIO4 pin. Reading this bit will return ***the output value of GPIO4.*** |
| 2 | V2GPIO3_VAL | Read/Write | **V2GPIO3 Value.** Set the output value of VID2/GPIO3 pin. Reading this bit will return ***the output value of GPIO3.*** |
| 1 | V1GPIO2_VAL | Read/Write | **V1GPIO2 Value.** Set the output value of VID1/GPIO2 pin. Reading this bit will return ***the output value of GPIO2.*** |
| 0 | V0GPIO1_VAL | Read/Write | **V0GPIO1 Value.** Set the output value of VID0/GPIO1 pin. Reading this bit will return ***the output value of GPIO1.*** |

## 8.12 GPIO8-14 Data Register - Index 4Bh

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | Reserved | Read/write | Reserved. |
| 6 | GPIO14_VAL | Read/Write | **GPIO14 Value.** Set the output value of GPIO14 pin. Reading this bit will return the value of pin 28. |
| 5 | GPIO13_VAL | Read/Write | **GPIO13 Value.** Set the output value of GPIO13 pin. Reading this bit will return the value of pin 27. |
| 4 | GPIO12_VAL | Read/Write | **GPIO12 Value.** Set the output value of GPIO12 pin. Reading this bit will return the value of pin 26. |
| 3 | GPIO11_VAL | Read/Write | **GPIO11 Value.** Set the output value of GPIO11 pin. Reading this bit will return the value of pin 24. |
| 2 | GPIO10_VAL | Read/Write | **GPIO10 Value.** Set the output value of GPIO10 pin. Reading this bit will return the value of pin 23. |
| 1 | GPIO9_VAL | Read/Write | **GPIO9 Value.** Set the output value of GPIO9 pin. Reading this bit will return the value of pin 22. |
| 0 | GPIO8_VAL | Read/Write | **GPIO8 Value.** Set the output value of GPIO8 pin. Reading this bit will return the value of pin 12. |

## 8.13 Nuvoton Vendor ID (Low Byte) - Index 4Ch

Power-on default [7:0] = 1010, 0011 b (0xA3h)

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7:0 | VIDL[7:0] | Read Only | Vendor ID Low Byte. Default A3h. |

## 8.14 Nuvoton Vendor ID (High Byte) - Index 4Dh

Power-on default [7:0] = 0101, 1100 b (0x5Ch)

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7:0 | VIDH[7:0] | Read Only | **Vendor ID High Byte.** Default 5Ch |

## 8.15 Chip ID - Index 4Eh

Power on default [7:0] = **1000, 0000** b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | CHIPID[7:0] | Read Only | **Nuvoton Chip ID number.** Read this register will return ***0x80h*** for W83L786R/G. |

## 8.16 VID0-4 Input Data Register - Index 4Fh

Power on default [7:0] = 000P, PPPP b (P: power on trapping)

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-5 | Reserved | Read Only | Reserved. |
| 4 | VID4P_VAL | Read Only | **VID4 Value.** Reading this bit will return ***the value of pin 5.*** |
| 3 | VID3P_VAL | Read Only | **VID3 Value.** Reading this bit will return ***the value of pin 4.*** |
| 2 | VID2P_VAL | Read Only | **VID2 Value.** Reading this bit will return ***the value of pin 3.*** |
| 1 | VID1P_VAL | Read Only | **VID1 Value.** Reading this bit will return ***the value of pin 2.*** |
| 0 | VID0P_VAL | Read Only | **VID0 Value.** Reading this bit will return ***the value of pin 1.*** |

## 8.17 VID0-4/GPIO1-5 Output Mode Control Register - Index 50h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-5 | Reserved | Read/write | Reserved. |
| 4 | VID4_OB | Read/write | Enable VID4/GPIO5 as Output Buffer. Set to<br><1> VID4/GPIO5 can drive logical high or logical low.<br><0> VID4/GPIO5 is open-drain. |
| 3 | VID3_OB | Read/write | Enable VID3/GPIO4 as Output Buffer. Set to<br><1> VID3/GPIO4 can drive logical high or logical low.<br><0> VID3/GPIO4 is open-drain. |
| 2 | VID2_OB | Read/write | Enable VID2/GPIO3 as Output Buffer. Set to<br><1> VID2/GPIO3 can drive logical high or logical low.<br><0> VID2/GPIO3 is open-drain. |
| 1 | VID1_OB | Read/write | Enable VID1/GPIO2 as Output Buffer. Set to<br><1> VID1/GPIO2 can drive logical high or logical low.<br><0> VID1/GPIO2 is open-drain. |
| 0 | VID0_OB | Read/write | Enable VID0/GPIO1 as Output Buffer. Set to<br><1> VID0/GPIO1 can drive logical high or logical low.<br><0> VID0/GPIO1 is open-drain. |

### 8.18 GPIO8-14 Output Mode Control Register - Index 51h

Power on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | Reserved | Read/write | Reserved. |
| 6 | GPIO14_OB | Read/write | Enable GPIO14 as Output Buffer. Set to<br><1> GPIO14 can drive logical high or logical low.<br><0> GPIO14 is open-drain. |
| 5 | GPIO13_OB | Read/write | Enable GPIO13 as Output Buffer. Set to<br><1> GPIO13 can drive logical high or logical low.<br><0> GPIO13 is open-drain. |
| 4 | GPIO12_OB | Read/write | Enable GPIO12 as Output Buffer. Set to<br><1> GPIO12 can drive logical high or logical low.<br><0> GPIO12 is open-drain. |
| 3 | GPIO11_OB | Read/write | Enable GPIO11 as Output Buffer. Set to<br><1> GPIO11 can drive logical high or logical low.<br><0> GPIO11 is open-drain. |
| 2 | GPIO10_OB | Read/write | EnableGPIO10 as Output Buffer. Set to<br><1> GPIO10 can drive logical high or logical low.<br><0> GPIO10 is open-drain. |
| 1 | GPIO9_OB | Read/write | Enable GPI9 as Output Buffer. Set to<br><1> GPIO9 can drive logical high or logical low.<br><0> GPIO9 is open-drain. |
| 0 | GPIO8_OB | Read/write | Enable GPIO8 as Output Buffer. Set to<br><1> GPIO8 can drive logical high or logical low.<br><0>GPIO8 is open-drain. |

### 8.19 INT# Property Select - Index 52h

Power on - <7:0> --0000, 0100 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| **7-4** | **Reserved** | **Read/Write** | **Reserved.** |
| 3-2 | TEMP_INT_MD [1:0] | Read/Write | **Temperature INT Mode Select.**<br><00> - **Comparator Interrupt Mode:**<br>Temperature 1/2/3 exceeds $T_O$ (Over-temperature) limit causes an interrupt. Reading the Interrupt Status will reset this interrupt.<br><01> - **Two Time Interrupt Mode:**(Default)<br>This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis and $T_O$ type. Temperature exceeding $T_O$, causes an interrupt and then temperature going below $T_{HYST}$ will also cause another interrupt if the previous interrupt has been reset by reading the interrupt Status Register. Once an interrupt event has occurred by exceeding $T_O$, then reset, if the temperature remains above the $T_{HYST}$.<br><10> **- One Time Interrupt Mode:**<br>This bit use in temperature sensor 1/2 interrupt mode with hysteresis type. Temperature exceeding $T_O$ (Over-temperature) causes an interrupt and then temperature going below $T_{HYST}$ (Hysteresis temperature) will not cause an interrupt. Once an interrupt event has occurred by exceeding $T_O$, then going below $T_{HYST}$, and interrupt will not occur again until the temperature exceeding $T_O$. |
| 1 | EN_INT# | Read/Write | **Enable INT# Output.** A one enables the INT# Interrupt output. |
| **0** | **Reserved** | **Read/Write** | **Reserved.** |

## 8.20 Thermal Sensor 1/2/3 Type Register - Index 53h

Power on default [7:0] = 0100, 0001 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-3 | Reserved | Read/Write | Reserved. |
| 2 | T2_TYPE | Read/Write | Temperature sensor 2 type.<br><0> - Thermistor (10K @ 25 degree C, B=3435).<br><1> - thermal diode. |
| 1 | T1_TYPE | Read/Write | Temperature sensor 1 type.<br><0> - Thermistor (10K @ 25 degree C, B=3435).<br><1> - thermal diode. |
| 0 | T0_TYPE | Read/Write | Temperature sensor 0 (GPU) type.<br><0> - Thermistor (10K @ 25 degree C, B=3435)<br><1> - thermal diode. |

## 8.21 Fan Divisor Register - Index 54h

Power on default [7:0] = 0001, 0001 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | Reserved | Read/write | Reserved. |
| 6-4 | FAN2_DIV_SEL[2:0] | Read/Write | **FAN2 Divisor Select.**<br><000> - divide by 1;<br><001> - divide by 2;<br><010> - divide by 4;<br><011> - divide by 8.<br><100> - divide by 16.<br><101> - divide by 32.<br><110> - divide by 64.<br><111> - divide by 128. |
| 3 | Reserved | Read/write | Reserved. |
| 2-0 | FAN1_DIV_SEL[2:0] | Read/Write | **FAN1 Divisor Select.**<br><000> - divide by 1;<br><001> - divide by 2;<br><010> - divide by 4;<br><011> - divide by 8.<br><100> - divide by 16.<br><101> - divide by 32.<br><110> - divide by 64.<br><111> - divide by 128. |

## 8.22 Reserved - Index 55h ~ 5Fh

Reserved

## 8.23 FAN Configuration Register - Index 80h

Power on default [7:0] = 00**11**, **11**00 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7 | EN_PWM2 | Read/Write | FAN2 Control Mode<br><1> - PWM FAN Control Mode<br><0> - DC FAN Control Mode |
| 6 | EN_PWM1 | Read/Write | FAN1 Control Mode<br><1> - PWM FAN Control Mode<br><0> - DC FAN Control Mode |
| 5-4 | FAN2_MODE | Read/Write | FAN2 Control Mode.<br><00> - Manual Control Mode. (Default)<br><01> - Thermal Cruise mode.<br><10> - SMART FAN™ II Mode.<br><11> - FAN_SET. |
| 3-2 | FAN1_MODE | Read/Write | FAN 1 Control Mode.<br><00> - Manual Control Mode. (Default)<br><01> - Thermal Cruise mode.<br><10> - SMART FAN™ II Mode.<br><11> - FAN_SET. |
| **1-0** | **Reserved** | **Read/Write** | **Reserved.** |

## 8.24 DC FAN1 Output Voltage Level Control Register (Manual Mode) /FAN1 Output Voltage Table (SMART FAN™ II Mode) – Index 81h

Power on default [7:0] **1111**, 1111 b

For **Manual Mode**

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | Reserved | Read/Write | Reserved. |
| 3-0 | FAN1_DC [3:0] | Read/Write | DC FAN1 Output Level. Only for Thermal Manual Mode while CR80h bit3-2 is 00. This 3-bit register determines the DC FAN driving voltage.<br><0x0h> - DC output is 0V.<br><0xFh> - DC output is 3.3V.<br><0xXh> - DC output levels are from 0V to 3.3v and they are separated into 16 levels equally. |

For **SMART FAN™ II Mode**

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | FAN1_TAB2[3:0] | Read/Write | FAN1 Output Level 2 for SMART FAN™ II Mode. |
| 3-0 | FAN1_TAB1[3:0] | Read/Write | FAN1 Output Level 1 for SMART FAN™ II Mode. |

## 8.25 FAN1 Output Voltage Table (SMART FANTM II Mode) - Index 82h

Power on default [7:0] **1111**, 1111 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | FAN1_TAB4[3:0] | Read/Write | FAN1 Output Level 4 for SMART FAN™ II Mode. |
| 3-0 | FAN1_TAB3[3:0] | Read/Write | FAN1 Output Level 3 for SMART FAN™ II Mode. |

## 8.26 TEMP0 (D+_D-) Target Temperature Register (Thermal Cruise Mode) / TEMP_POINT 1 for FAN1 (SMART FAN™ II Mode) - Index 83h

Power on default [7:0] = 0000, 0000 b

TEMP1 target temperature register for **Thermal Cruise mode**.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| **7**-0 | TEMP_TAR_T0[**7**:0] | Read/Write | **TEMP0 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit3-2 is 01. |

TEMP_**POINT1** register for **Smart FAN II Mode**.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | TEMP_**P**1F1[**7**:0] | Read/Write | **TEMP_POINT1 for FAN1 use Smart FAN II Mode.** |

## 8.27 TEMP_POINT2 for FAN1 (SMART FANTM II Mode) - Index 84h

***Power on default [7:0] = 0000, 0000 b***

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| ***7-0*** | ***TEMP_P2F1[7:0]*** | ***Read/Write*** | ***TEMP_POINT2 for FAN1 use SMART FAN™ II Mode.*** |

## 8.28 FAN 1 Speed Low Limit Rate Control Register (Thermal Cruise Mode) / TEMP_*POINT3* for FAN1 (SMART FAN™ II Mode) - Index 85h

Power on default [7:0] = ***0000, 0000*** b

| Bit | Name | Read/Write | Description |
|---|---|---|---|
| 7-4 | Reserved | Read/Write | Reserved. |
| 3-0 | FAN1_LL [3:0] | Read/Write | Low Limit Speed of FAN1. Only for **Thermal Cruise mode**. |

TEMP_***POINT***3 register for **Smart FAN II Mode**.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | TEMP_***P***3F1[***7***:0] | Read/Write | **TEMP_*POINT*3 for FAN1 use SMART FAN™ II Mode.** |

## 8.29 TEMP_POINT4 for FAN1 (SMART FANTM II Mode) - Index 86h

***Power on default [7:0] = 0000, 0000 b***

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | ***TEMP_P4F1[7:0]*** | Read/Write | ***TEMP_POINT4 for FAN1 use SMART FAN™ II Mode.*** |

## 8.30 DC FAN2 Output Voltage Level Control Register (Manual Mode)/ FAN2 Output Voltage Table (SMART FAN™ II Mode) - 87h

Power on default [7:0] **1111**, 1111 b

For **Manual Mode**

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | Reserved | Read/Write | Reserved. |
| 3-0 | FAN2_DC [3:0] | Read/Write | DC FAN2 Output Level. Only for Thermal Manual Mode while CR80h bit5-4 is 00. This 3-bit register determines the DC FAN driving voltage.<br><0x0h> - DC output is 0V.<br><0xFh> - DC output is 3.3V.<br><0xXh> - DC output levels are from 0V to 3.3v and they are separated into 16 levels equally. |

For **SMART FAN™ II Mode**

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | FAN2_TAB2[3:0] | Read/Write | FAN2 Output Level 2 for SMART FAN™ II Mode. |
| 3-0 | FAN2_TAB1[3:0] | Read/Write | FAN2 Output Level 1 for SMART FAN™ II Mode. |

## 8.31 FAN2 Output Voltage Table (SMART FANTM II Mode) - Index 88h

Power on default [7:0] **1111,** 1111 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | FAN2_TAB4[3:0] | Read/Write | FAN2 Output Level 4 for SMART FAN™ II Mode. |
| 3-0 | FAN2_TAB3[3:0] | Read/Write | FAN2 Output Level 3 for SMART FAN™ II Mode. |

## 8.32 TEMP1 (VTIN1) Target Temperature Register (Thermal Cruise Mode) / TEMP_POINT 1 for FAN2 (SMART FAN™ II Mode) - Index 89h

Power on - [7:0] = 0000, 0000 b

TEMP2 target temperature register for **Thermal Cruise mode**.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| **7**-0 | TEMP_TAR_T1[**7**:0] | Read/Write | **TEMP1 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit5-4 is 01. |

TEMP_POINT1 register for **SMART FAN™ II Mode**.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | TEMP_**P**1F2[**7**:0] | Read/Write | **TEMP_POINT1 for FAN2 use SMART FAN™ II Mode.** |

## 8.33 TEMP_POINT2 for FAN2 (SMART FANTM II Mode) - Index 8Ah

***Power on - [7:0] = 0000, 0000 b***

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| ***7-0*** | ***TEMP_P2F2[7:0]*** | ***Read/Write*** | ***TEMP_POINT2 for FAN2 use SMART FAN™ II Mode.*** |

## 8.34 FAN 2 Speed Low Limit Rate Control Register/ TEMP_*POINT3* for FAN2 SMART FAN™ II Mode) - Index 8*B*h

Power on default [7:0] =***0000, 0000*** b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-5 | Reserved | Read/Write | Reserved. |
| 4-1 | FAN2_LL [3:0] | Read/Write | Low Limit Speed of FAN2. Only for **Thermal Cruise mode**. |

TEMP_***POINT3*** register for **SMART FAN™ II Mode**.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | TEMP_***P***3F2[***7***:0] | Read/Write | **TEMP_*POINT*3 for FAN2 use SMART FAN™ II Mode.** |

## 8.35 TEMP_POINT4 for FAN2 (SMART FANTM II Mode) - Index 8Ch

***Power on default [7:0] = 0000, 0000 b.***

| Bit | Name | Read/Write | Description |
|---|---|---|---|
| 7-0 | ***TEMP_P4F2[7:0]*** | Read/Write | ***TEMP_POINT4 for FAN2 use SMART FAN™ II Mode.*** |

## 8.36 Tolerance of Temperature Register - Index 8Dh

Power on default [7:0] = **0011, 0011** b

For Thermal Cruise mode

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | TOL_T1[3:0] | Read/Write | **Tolerance of Fan 2 Target Temperatures (Temp1).** Only for Thermal Cruise mode. |
| 3-0 | TOL_T0[3:0] | Read/Write | **Tolerance of Fan 1 Target Temperature (Temp0).** Only for Thermal Cruise mode. |

For Smart FAN II Mode

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-4 | TOL_T1[3:0] | Read/Write | **Tolerance of Fan 2 Temperatures (Temp1).** Only for SMART FAN™ II Mode. |
| 3-0 | TOL_T0[3:0] | Read/Write | **Tolerance of Fan 1 Temperature (Temp0).** Only for SMART FAN™ II Mode. |

## 8.37 FAN 2D/3D state Control Register - Index 8Eh

At SMART FAN™ II Mode, FAN will be controlled by 2D/3D mode after writing **2Dh/3Dh** to CR8A

## 8.38 FAN Pre-Scale Register - Index 8Fh

**Power on default [7:0] = 0010, 0010 b**

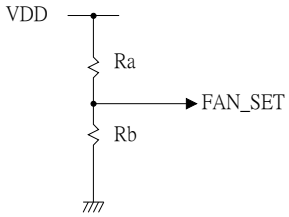
| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| ***7*** | ***PWM2_CLK_SEL*** | ***Read/Write*** | ***PWM Input Clock Select of Fan 2. This bit select FAN input clock to pre-scale divider.***<br>***<0> - 1.44MHz***<br>***<1> - 180KHz*** |
| ***6-4*** | ***PWM2_CLK_DIV [2:0]*** | ***Read/Write*** | ***FAN 2 PWM Input Clock divider.***<br>***<000> - divider is 1***<br>***<001> - divider is 2***<br>***<010> - divider is 4***<br>***<011> - divider is 8***<br>***<100> - divider is 16***<br>***<101> - divider is 32***<br>***<110> - divider is 64***<br>***<111> - divider is 128*** |
| ***3*** | ***PWM1_CLK_SEL*** | ***Read/Write*** | ***PWM Input Clock Select of Fan 1. This bit select FAN input clock to pre-scale divider.***<br>***<0h> - 1.44MHz***<br>***<1h> - 180KHz*** |

FAN Pre-Scale Register - Index 8Fh, continued.

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| ***2-0*** | ***PWM1_CLK_DIV [2:0]*** | ***Read/Write*** | ***FAN 1 PWM Input Clock divider.***<br>***<000> - divider is 1***<br>***<001> - divider is 2***<br>***<010> - divider is 4***<br>***<011> - divider is 8***<br>***<100> - divider is 16***<br>***<101> - divider is 32***<br>***<110> - divider is 64***<br>***<111> - divider is 128*** |

## 8.39 FAN Initial Output Value – Index90h

Power on trapping

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| ***7*** | ***FAN_3DST*** | ***Read*** | ***A one indicates FAN is working at 3D mode (for SMART FAN™ II Mode).***<br>***If GPIO11 is disabled, it can be programmed by Pin24.***<br>***Else, it can be programmed directly by I²C.*** |
| 6-4 | Reserved | Read/Write | Reserved. |
| 3-0 | FANINI [3:0] | Read/Write | **FAN Initial Speed.**<br>  <br>Use two resistors to divide a four section to represent different initial FAN Speed. The table is shown as following. |

| Section | FAN Speed rate | Ra | Rb |
|---|---|---|---|
| 3 | 100% | 9.1K | × |
| 2 | 81% | 4.7K | 9.1K |
| 1 | 62% | 9.1K | 4.7K |
| 0 | 43% | × | 9.1K |

## 8.40 Fan Step down Time Register - Index 91h

Power on default [7:0] = **0001, 0100** b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | STEP_DOWN_T[7:0] | Read/Write | The time interval, which is 1-second unit, to decrease DC output level in SMART FAN™ II Control mode. |

## 8.41 Fan Step up Time Register - Index 92h

Power on default [7:0] = 0000, 1010 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | STEP_UP_T[7:0] | Read/Write | The time interval, which is 1-second unit, to increase DC output level in SMART FAN™ II Control mode. |

## 8.42 Temperature Sensor 0 (D+_D-) Offset Register - Index 93h

Power-on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | OFFSET0[7:0] | Read/Write | Temperature 0 base temperature. The real temperature is sum of both monitor value and offset value.<br>0111,1111 => +127 degree C<br>0111,1110 => +126 degree C<br>:<br>0000,0001 => +1 degree C<br>0000,0000 => +0 degree C<br>1111,1111 => -1 degree C<br>1111,1110 => -2 degree C<br>:<br>1000,0000 => -128 degree |

## 8.43 Temperature Sensor 1 (VTIN1) Offset Register – Index94h

Power-on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | OFFSET1[7:0] | Read/Write | Temperature 1 base temperatures. The real temperature is sum of both monitor value and offset value.<br>0111,1111 => +127 degree C<br>0111,1110 => +126 degree C<br>:<br>0000,0001 => +1 degree C<br>0000,0000 => +0 degree C<br>1111,1111 => -1 degree C<br>1111,1110 => -2 degree C<br>:<br>1000,0000 => -128 degree |

## 8.44 Temperature Sensor 2 (VTIN2) Offset Register - Index 95h

Power-on default [7:0] = 0000, 0000 b

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | OFFSET2 [7:0] | Read/Write | Temperature 2 base temperatures. The real temperature is sum of both monitor value and offset value.<br>0111,1111 => +127 degree C<br>0111,1110 => +126 degree C<br>:<br>0000,0001 => +1 degree C<br>0000,0000 => +0 degree C<br>1111,1111 => -1 degree C<br>1111,1110 => -2 degree C<br>:<br>1000,0000 => -128 degree |

## 8.45 VRM9.0 High Tolerance Register - Index 96h

**Power-on default [7:0] = 0001, 1001 b**

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| **7-0** | **VRM9TOL_H [7:0]** | **Read/Write** | |

## 8.46 VRM9.0 Low Tolerance Register - Index 97h

**Power-on default [7:0] = 0001, 1001 b**

| BIT | NAME | READ/WRITE | DESCRIPTION |
|---|---|---|---|
| 7-0 | VRM9TOL_L [7:0] | Read/Write | |

Value RAM and Limit Value

## 8.47 Value RAM - Index 20h- 3Fh or 60h - 7Fh

| INDEX A7-A0 | DESCRIPTION | UNIT |
|---|---|---|
| 20h | VCORE reading | |
| 21h | VRAM reading | |
| 22h | **VCC reading** | |
| 23h | **VIN1 reading** | |
| 24h | **VIN2 reading** | |
| 25h | Temperature 0 reading (D+_D-, 0 ~ 255) | °C |
| 26h | Temperature 1 reading (VTIN1, 0 ~ 255) | °C |
| 27h | Temperature 2 reading (VTIN2, 0 ~ 255) | °C |
| 28h | FANIN1 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. | Count |
| 29h | FANIN2 reading<br>**Note:** This location stores the number of counts of the internal clock per revolution. | Count |
| 2Ah | Reserved | |
| 2Bh | VCORE High Limit. (0xff) | |
| 2Ch | VCORE Low Limit. (0x00) | |
| 2Dh | VRAM High Limit. (0xff) | |
| 2Eh | VRAM Low Limit. (0x00) | |
| 2Fh | **VCC High Limit. (0xff)** | |
| 30h | **VCC Low Limit. (0x00)** | |
| 31h | **VIN1 High Limit. (0xff)** | |
| 32h | **VIN1 Low Limit. (0x00)** | |
| 33h | **VIN2 High Limit. (0xff)** | |
| 34h | **VIN2 Low Limit. (0x00)** | |

Value RAM - Index 20h- 3Fh or 60h - 7Fh, continued.

| INDEX A7-A0 | DESCRIPTION | UNIT |
|---|---|---|
| 35h | Over Temperature 0 Limit (High). (0x50) | °C |
| 36h | Temperature 0 Hysteresis Limit (Low). (0x4b) | °C |
| 37h | Over Temperature 1 Limit (High). (0x50) | °C |
| 38h | Temperature 1 Hysteresis Limit (Low). (0x4b) | °C |
| 39h | Over Temperature 2 Limit (High). (0x50) | °C |
| 3Ah | Temperature 2 Hysteresis Limit (Low). (0x4b) | °C |
| 3Bh | FAN1 Fan Count Limit. (0xff)<br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. | Count |
| 3Ch | FAN2 Fan Count Limit. (0xff)<br>**Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed. | Count |
| ***3Dh*** | ***FAN1 Speed Control Output Level*** | |
| ***3Eh*** | ***FAN2 Speed Control Output Level*** | |
| 3Fh | Reserved | |

# 9. ELECTRICAL CHARACTERISTICS

## 9.1 Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage | -0.5 to 7.0 | V |
| Input Voltage | -0.5 to $V_{DD}$+0.5 | V |
| Operating Temperature | 0 to +70 | ° C |
| Storage Temperature | -55 to +150 | ° C |

**Note:** Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

## 9.2 DC Characteristics

(Ta = 0° C to 70° C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V)

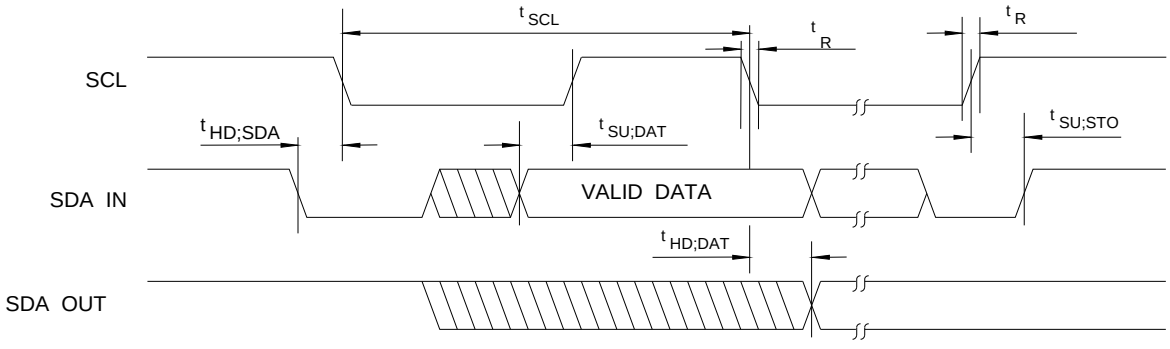
| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$I/O_{12t}$ - TTL level bi-directional pin with source-sink capability of 12 mA** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = - 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |
| **$I/O_{12ts}$ - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD}$ = 5 V |
| Hysteresis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$ = 5 V |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = - 12 mA |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0V |

DC Characteristics, continued

| PARAMETER | SYM. | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| **$OUT_{12t}$ - TTL level output pin with source-sink capability of 12 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| Output High Voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = -12 mA |
| **$OD_8$ - Open-drain output pin with sink capability of 8 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 8 mA |
| **$OD_{12}$ - Open-drain output pin with sink capability of 12 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 12 mA |
| **$OD_{48}$ - Open-drain output pin with sink capability of 48 mA** | | | | | | |
| Output Low Voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 48 mA |
| **$IN_t$ - TTL level input pin** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.0 | | | V | |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |
| **$IN_{ts}$ - TTL level Schmitt-triggered input pin** | | | | | | |
| Input Low Threshold Voltage | $V_{t-}$ | 0.5 | 0.8 | 1.1 | V | $V_{DD}$ = 5 V |
| Input High Threshold Voltage | $V_{t+}$ | 1.6 | 2.0 | 2.4 | V | $V_{DD}$ = 5 V |
| Hysteresis | $V_{TH}$ | 0.5 | 1.2 | | V | $V_{DD}$ = 5 V |
| Input High Leakage | $I_{LIH}$ | | | +10 | μA | $V_{IN}$ = $V_{DD}$ |
| Input Low Leakage | $I_{LIL}$ | | | -10 | μA | $V_{IN}$ = 0 V |

## 9.3 AC Characteristics

### 9.3.1 Serial Bus Timing Diagram

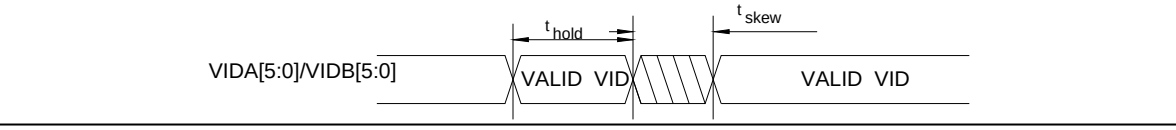



Serial Bus Timing Diagram

Serial Bus Timing

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| SCL clock period | $t_{SCL}$ | 10 | | uS |
| Start condition hold time | $t_{HD;SDA}$ | 4.7 | | uS |
| Stop condition setup-up time | $t_{SU;STO}$ | 4.7 | | uS |
| DATA to SCL setup time | $t_{SU;DAT}$ | 120 | | nS |
| DATA to SCL hold time | $t_{HD;DAT}$ | 5 | | nS |
| SCL and SDA rise time | $t_R$ | | 1.0 | uS |
| SCL and SDA fall time | $t_F$ | | 300 | nS |

### 9.3.2 VID Input Skew




VID Input Timing

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| VID Input Unstable Time | $t_{Skew}$ | | 0.8 | uS |
| VID Valid Input Hold Time | $t_{hold}$ | 4 | | uS |

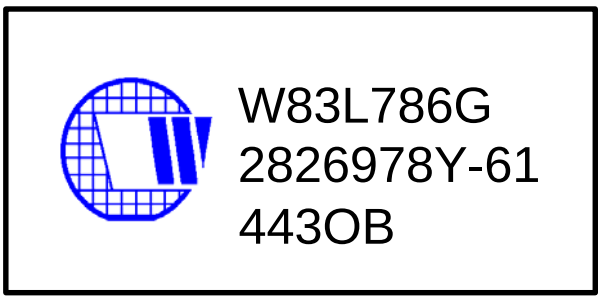
## 10. THE TOP MARKING

The top marking of W83L786R


Left: Nuvoton logo
1st line: Nuvoton logo and part number: W83L786R
2nd line: Tracking code 2 826978Y-61
3rd line: Tracking code 443 O B

**443**: packages made in '04, week 43
**O**: assembly house ID; A means ASE, S means SPIL, O means OSE
**B**: IC revision

The top marking of W83L786G

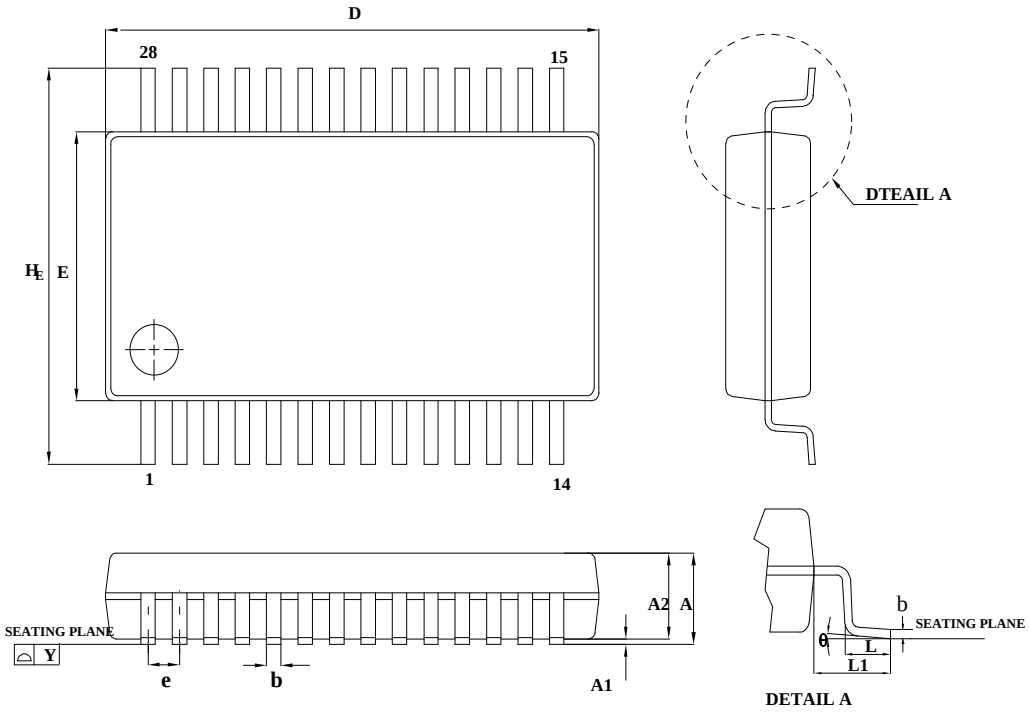



Left: Nuvoton logo
1st line: Nuvoton logo and part number: W83L786G; G means Pb-free package
2nd line: Tracking code 2 826978Y-61
3rd line: Tracking code 443 O B

**443**: packages made in '04, week 43
**O**: assembly house ID; A means ASE, S means SPIL, O means OSE
**B**: IC revision

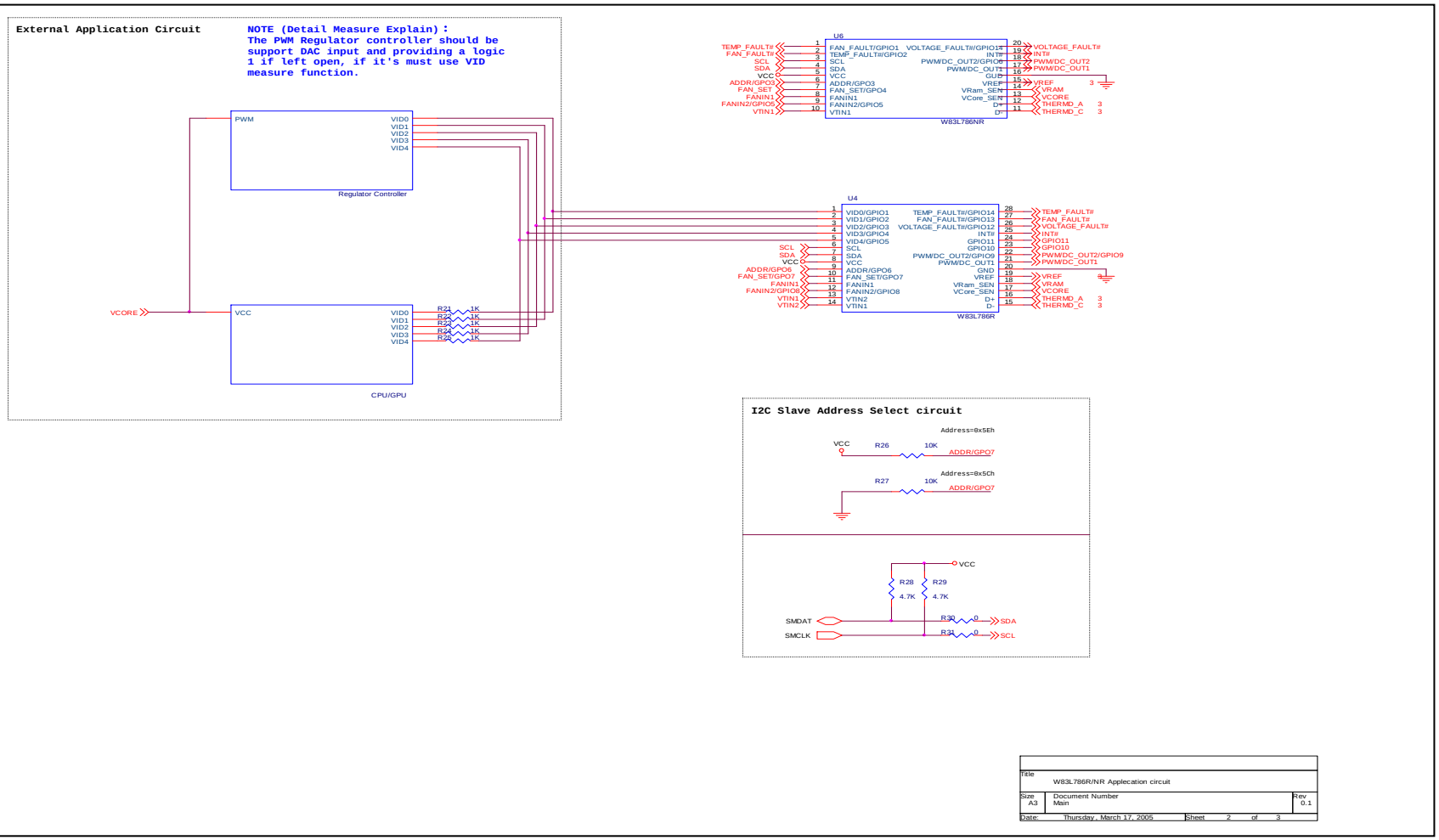
## 11. PACKAGE SPECIFICATION

- 28L SSOP-209 mil

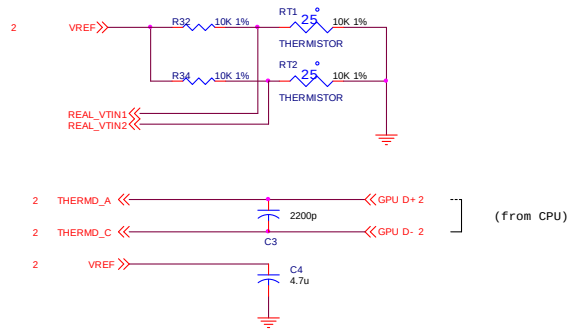



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | — | — | 2.00 | — | — | 0.079 |
| A1 | 0.05 | — | — | 0.002 | — | — |
| A2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| b | 0.22 | — | 0.38 | 0.009 | — | 0.015 |
| c | 0.09 | — | 0.25 | 0.004 | — | 0.010 |
| D | 10.05 | 10.20 | 10.35 | 0.395 | 0.401 | 0.407 |
| E | 5.00 | 5.30 | 5.60 | 0.197 | 0.209 | 0.220 |
| $H_E$ | 7.40 | 7.80 | 8.20 | 0.291 | 0.307 | 0.323 |
| e | — | 0.65 | — | — | 0.0256 | — |
| L | 0.55 | 0.75 | 0.95 | 0.021 | 0.030 | 0.037 |
| L1 | — | 1.25 | — | — | 0.050 | — |
| Y | — | — | 0.10 | — | — | 0.004 |
| θ | 0 | — | 8 | 0 | — | 8 |

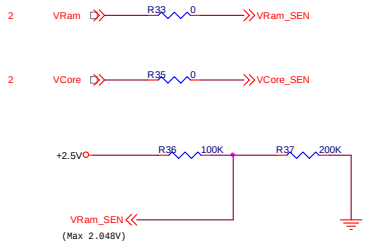
## 12. APPLICATION CIRCUITS



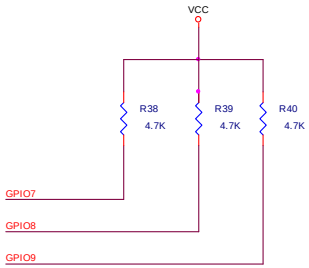
**Temperature sensing circuit**



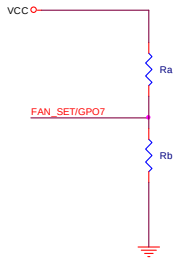

**Voltage sensing circuit**




**ALL GPIO pins must add pull-pu resistor**



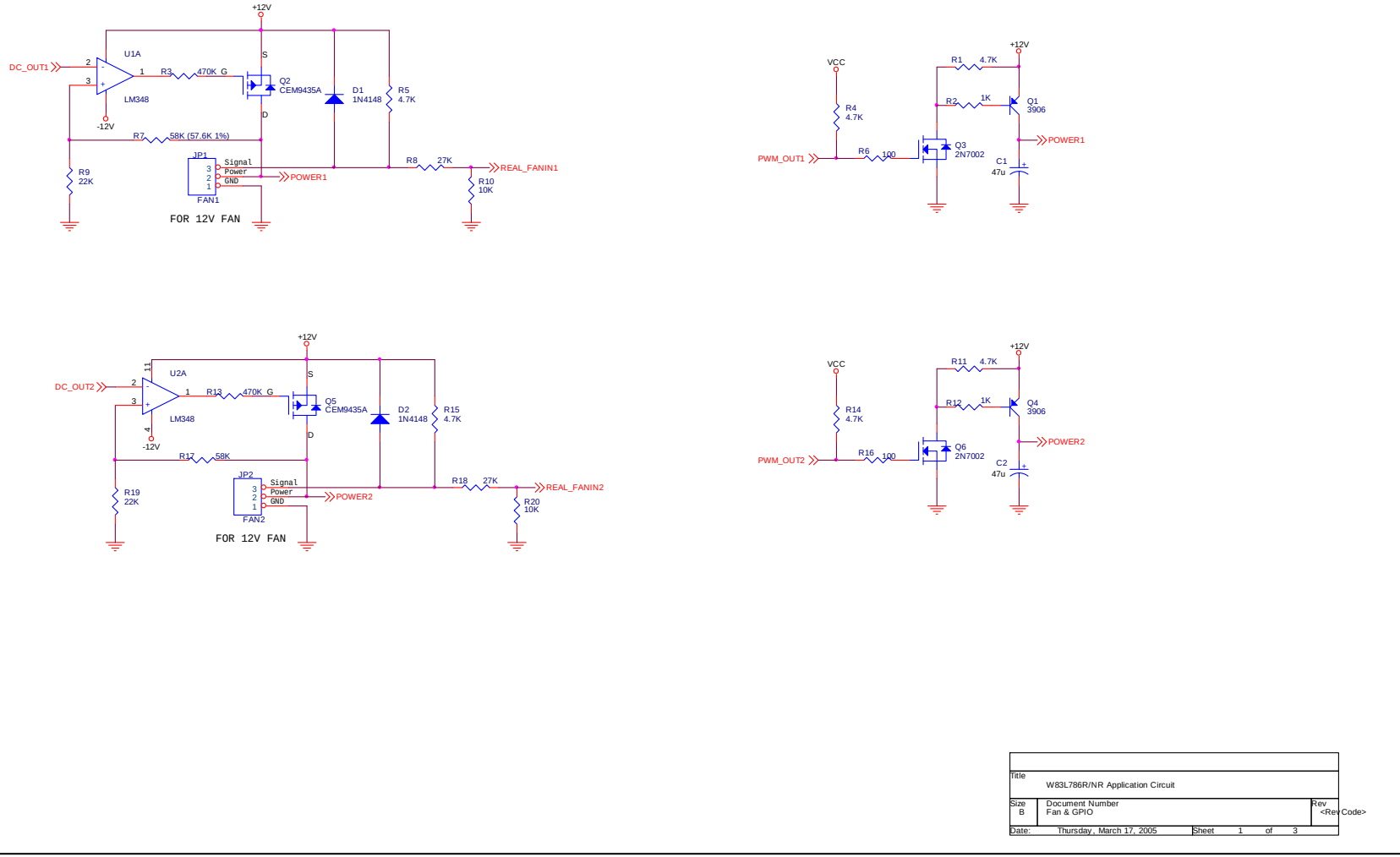

**Fan initial speed setting**




| Section | Fan Speed rate | Ra | Rb |
|---|---|---|---|
| 3 | 100% | 9.1K | X |
| 2 | 81% | 4.7K | 9.1K |
| 1 | 62% | 9.1K | 4.7K |
| 0 | 43% | X | 9.1K |

| | | |
|---|---|---|
| Title | W83L786R/NR Application Circuit | |
| Size B | Document Number Temperature & Voltage | Rev |
| Date: Thursday, March 17, 2005 | Sheet 3 of 3 | |

**PWM FAN Speed control circuit**



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