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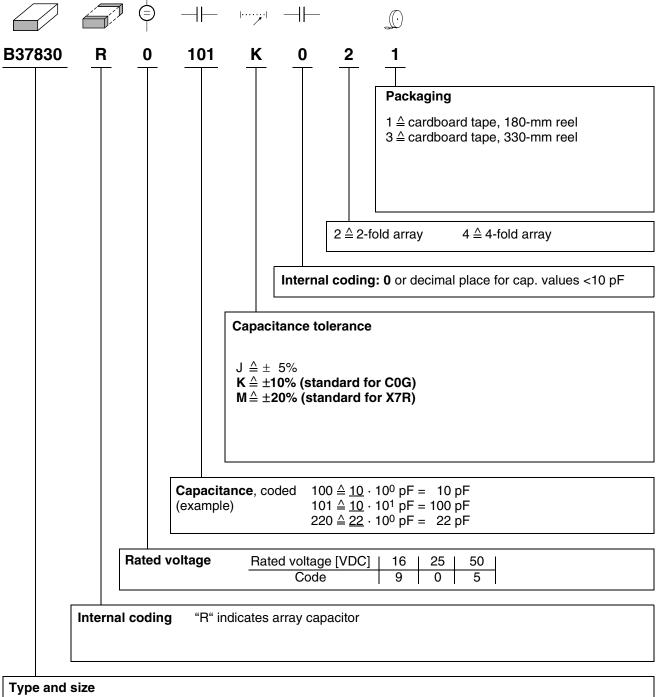
Array capacitors, COG

Date:

October 2006

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Chip size	Temperature characteristic		
( <b>inch</b> / mm)	COG	X7R	
<b>0405</b> / 1012	B37830	B37831	
<b>0508</b> / 1220	B37940	B37941	
<b>0612</b> / 1632	B37871	B37872	

EPCOS

SMD

Multilayer ceramic capacitors

#### C0G

Features

- Reduction of mounting time and mounting costs
- Space saving on the PCB
- To AEC-Q200

#### Applications

- Suitable for electronic circuits with parallel line layout
- Coupling and filtering, particularly in RF circuits
- Resonant circuits
- Filter circuits

#### Termination

■ For soldering: Nickel barrier terminations (Ni)

#### Options

Alternative capacitance tolerances available on request

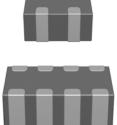
#### **Delivery mode**

Cardboard tape,180-mm and 330-mm reel available

#### **Electrical data**

Temperature characteristic		COG	
Climatic category (IEC 60068-1)		55/125/56	
Standard		EIA	
Dielectric		Class 1	
Rated voltage	V <sub>R</sub>	25, 50	VDC
Test voltage	V <sub>test</sub>	2.5 · V <sub>R</sub> /5 s	VDC
Capacitance range / E series	C <sub>R</sub>	10 pF 1.0 nF (E6)	
Temperature coefficient		$0\pm30\cdot10^{-6}/K$	
Dissipation factor (limit value)	tan $\delta$	<1.0 · 10 <sup>-3</sup>	
Insulation resistance <sup>1)</sup> at + 25 °C	R <sub>ins</sub>	>10 <sup>5</sup>	MΩ
Insulation resistance <sup>1)</sup> at +125 °C	R <sub>ins</sub>	>10 <sup>4</sup>	MΩ
Time constant <sup>1)</sup> at + 25 °C	τ	>1000	s
Time constant <sup>1)</sup> at +125 °C	τ	>100	s
Operating temperature range	T <sub>op</sub>	-55 +125	°C
Ageing		none	

1) For  $C_R$  >10 nF the time constant  $\tau = C \cdot R_{ins}$  is given.







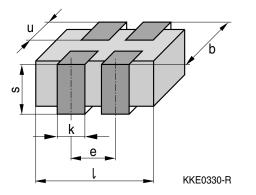
C0G

#### **Capacitance tolerances**

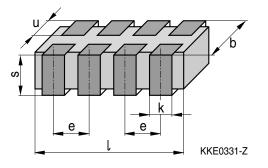
Code letter	J	K (standard)	
Tolerance	±5%	±10%	

#### **Dimensional drawing**

2-fold array (case size 0405)



4-fold array (case sizes 0508 and 0612)



#### Dimensions (mm)

		2-fold array	4-fold array	
Case size	(inch) (mm)	0405 1012	0508 1220	0612 1632
I		1.37 ±0.15	2.00 ±0.2	3.20 ±0.2
b		1.00 +0/-0.15	1.25 ±0.15	1.60 ±0.2
S		0.70 max.	0.85 ±0.1	0.85 ±0.1
k		0.36 ±0.1	0.30 ±0.1	0.40 ±0.15
е		0.64	0.50 ±0.1	0.80 ±0.15
u		0.20 ±0.1	0.20 +0.3/-0.1	0.20 +0.3/-0.1

Tolerances to CECC 32101-801

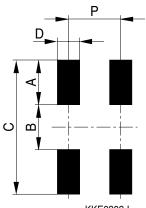
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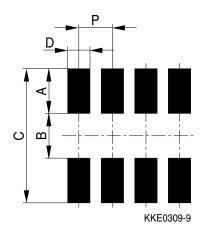
#### **Recommended solder pad**

2-fold array (case size 0405)



KKE0302-L

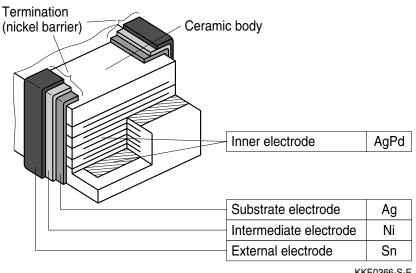
4-fold array (case sizes 0508 and 0612)



#### Recommended dimensions (mm) for reflow soldering

Case size	(inch/mm)	Туре	А	В	С	D	Р
	0405/1012	2-fold array	0.50 0.55	0.45 0.50	1.45 1.60	0.30 0.35	0.64 ±0.10
	0508/1220	4-fold array	0.50 0.70	0.60 0.70	1.60 2.10	0.25 0.35	0.50 ±0.005
	0612/1632	4-fold array	0.70 0.90	0.80 1.00	2.20 2.80	0.30 0.40	0.80 ±0.005

#### **Termination**



KKE0366-S-E

10/06

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#### Product range array capacitors, C0G

C0G

		2-fold arrays		4-fold arrays			
Size <sup>1)</sup>		04	05	0508		0610	
inch			05			0612	
mm			12		20	1632	
Туре		B37	'830	B37	'940	B37871	
	(VDC) (VDC)	25		50		50	
C <sub>R</sub>		25		50		50	
10	pF						
15	pF						
22	pF						
33	pF						
47	pF						
68	pF						
100	pF						
150	pF						
180	pF						
220	pF						
330	pF						
470	pF						
680	pF						
1.0	nF						

<sup>1)</sup>  $l \times b$  (inch) /  $l \times b$  (mm)



C0G; 0405



#### Ordering codes and packing for C0G arrays, 25 VDC, nickel barrier terminations

			Chip thickness	Cardboard tape,	Cardboard tape,
				$\varnothing$ 180-mm reel	Ø 330-mm reel
				* ≙ <b>1</b>	* ≙ 3
C <sub>R</sub> <sup>1)</sup>		Ordering code <sup>2)</sup>	mm	pcs/reel	pcs/reel
Case	e size 04	05, 25 VDC, 2-fold arrays			
10	pF	B37830R0100K02*	0.6 ±0.1	5000	20000
15	pF	B37830R0150K02*	0.6 ±0.1	5000	20000
22	pF	B37830R0220K02*	0.6 ±0.1	5000	20000
33	pF	B37830R0330K02*	0.6 ±0.1	5000	20000
47	pF	B37830R0470K02*	0.6 ±0.1	5000	20000
68	pF	B37830R0680K02*	0.6 ±0.1	5000	20000
100	pF	B37830R0101K02*	0.6 ±0.1	5000	20000
150	pF	B37830R0151K02*	0.6 ±0.1	5000	20000
180	pF	B37830R0181K02*	0.6 ±0.1	5000	20000

<sup>1)</sup> Other capacitance values on request.

<sup>2)</sup> The table contains the ordering codes for the standard capacitance tolerance. For other available capacitance tolerances see page 128.





C0G; 0508 and 0612

#### Ordering codes and packing for C0G arrays, 50 VDC, nickel barrier terminations

			Chip thickness	Cardboard tape, $\varnothing$ 180-mm reel	Cardboard tape, $\emptyset$ 330-mm reel
				* <b>≙ 1</b>	* ≙ 3
$C_R^{(1)}$		Ordering code <sup>2)</sup>	mm	pcs/reel	pcs/reel
Case	e size O	508, 50 VDC, 4-fold array	/S		
10	рF	B37940R5100K04*	0.85 ±0.1	4000	16000
15	pF	B37940R5150K04*	$0.85 \pm 0.1$	4000	16000
22	pF	B37940R5220K04*	$0.85 \pm 0.1$	4000	16000
33	pF	B37940R5330K04*	$0.85 \pm 0.1$	4000	16000
47	pF	B37940R5470K04*	$0.85 \pm 0.1$	4000	16000
68	pF	B37940R5680K04*	$0.85 \pm 0.1$	4000	16000
100	pF	B37940R5101K04*	$0.85 \pm 0.1$	4000	16000
150	pF	B37940R5151K04*	$0.85 \pm 0.1$	4000	16000
220	pF	B37940R5221K04*	$0.85 \pm 0.1$	4000	16000
Case	e size O	612, 50 VDC, 4-fold array	/S	·	·
10	pF	B37871R5100K04*	0.85 ±0.1	4000	16000
15	pF	B37871R5150K04*	$0.85 \pm 0.1$	4000	16000
22	pF	B37871R5220K04*	$0.85 \pm 0.1$	4000	16000
33	pF	B37871R5330K04*	$0.85 \pm 0.1$	4000	16000
47	pF	B37871R5470K04*	$0.85 \pm 0.1$	4000	16000
68	pF	B37871R5680K04*	$0.85 \pm 0.1$	4000	16000
100	pF	B37871R5101K04*	$0.85 \pm 0.1$	4000	16000
150	pF	B37871R5151K04*	$0.85 \pm 0.1$	4000	16000
220	pF	B37871R5221K04*	$0.85 \pm 0.1$	4000	16000
330	pF	B37871R5331K04*	$0.85 \pm 0.1$	4000	16000
470	pF	B37871R5471K04*	$0.85\pm\!0.1$	4000	16000
680	pF	B37871R5681K04*	$0.85 \pm 0.1$	4000	16000
1.(	) nF	B37871R5102K04*	$0.85\pm\!0.1$	4000	16000

1) Other capacitance values on request.

2) The table contains the ordering codes for the standard capacitance tolerance. For other available capacitance tolerances see page 128.

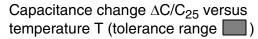
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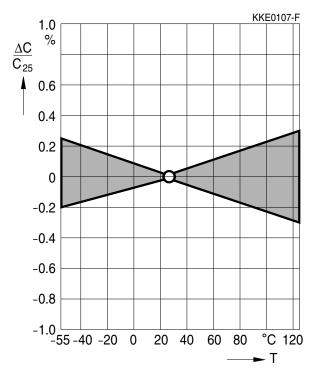




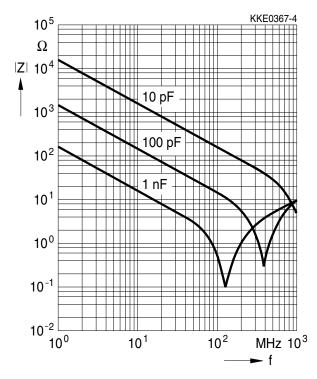
C0G

#### Typical characteristics<sup>1)</sup>

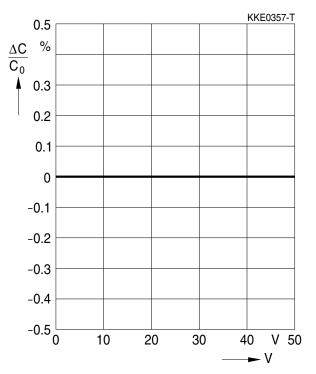




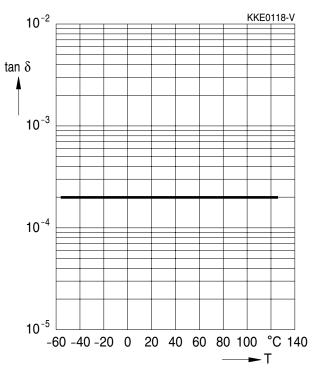
## Impedance |Z| versus frequency f



## Capacitance change ${\bigtriangleup C/C_0}$ versus superimposed DC voltage V



### Dissipation factor tan $\delta$ versus temperature T



1) For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc\_impedance.

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Please read *Cautions and warnings* and *Important notes* at the end of this document.

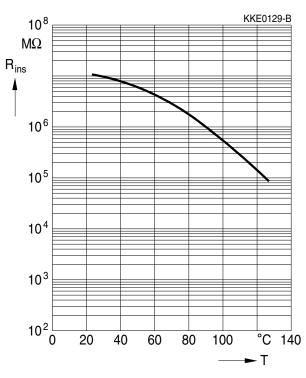




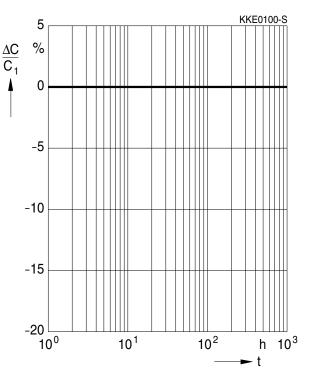
### Typical characteristics<sup>1)</sup>

Insulation resistance  $R_{\text{ins}}$  versus temperature  $\mathsf{T}$ 

C0G



Capacitance change  ${\scriptstyle \Delta C/C_1}$  versus time t



10 10/06

<sup>1)</sup> For more detailed information on frequency behavior and characteristics see www.epcos.com/mlcc\_impedance.



#### **Cautions and warnings**

#### Notes on the selection of ceramic capacitors

In the selection of ceramic capacitors, the following criteria must be considered:

- Depending on the application, ceramic capacitors used to meet high quality requirements should at least satisfy the specifications to AEC-Q200. They must meet quality requirements going beyond this level in terms of ruggedness (e.g. mechanical, thermal or electrical) in the case of critical circuit configurations and applications (e.g. in safety-relevant applications such as ABS and airbag equipment or durable industrial goods).
- 2. At the connection to the battery or power supply (e.g. clamp 15 or 30 in the automobile) and at positions with stranding potential, to reduce the probability of short circuits following a fracture, two ceramic capacitors must be connected in series and/or a ceramic capacitor with integrated series circuit should be used. The MLSC from EPCOS contains such a series circuit in a single component.
- 3. Ceramic capacitors with the temperature characteristics Z5U and Y5V do not satisfy the requirements to AEC-Q200 and are mechanically and electrically less rugged than C0G or X7R/X8R ceramic capacitors. In applications that must satisfy high quality requirements, therefore, these capacitors should not be used as discrete components (see the chapter "Effects on mechanical, thermal and electrical stress", point 1.4).
- 4. For ESD protection, preference should be given to the use of multilayer varistors (MLV) (see the chapter "Effects on mechanical, thermal and electrical stress", point 1.4).
- 5. An application-specific derating or continuous operating voltage must be considered in order to cushion (unexpected) additional stresses (see the chapter "Reliability").

#### The following should be considered in circuit board design

- 1. If technically feasible in the application, preference should be given to components having an optimal geometrical design.
- 2. At least FR4 circuit board material should be used.
- 3. Geometrically optimal circuit boards should be used, ideally those that cannot be deformed.
- 4. Ceramic capacitors must always be placed a sufficient minimum distance from the edge of the circuit board. High bending forces may be exerted there when the panels are separated and during further processing of the board (such as when incorporating it into a housing).
- 5. Ceramic capacitors should always be placed parallel to the possible bending axis of the circuit board.
- 6. No screw connections should be used to fix the board or to connect several boards. Components should not be placed near screw holes. If screw connections are unavoidable, they must be cushioned (for instance by rubber pads).



#### Cautions and warnings

#### The following should be considered in the placement process

- 1. Ensure correct positioning of the ceramic capacitor on the solder pad.
- 2. Caution when using casting, injection-molded and molding compounds and cleaning agents, as these may damage the capacitor.
- 3. Support the circuit board and reduce the placement forces.
- 4. A board should not be straightened (manually) if it has been distorted by soldering.
- 5. Separate panels with a peripheral saw, or better with a milling head (no dicing or breaking).
- 6. Caution in the subsequent placement of heavy or leaded components (e.g. transformers or snap-in components): danger of bending and fracture.
- 7. When testing, transporting, packing or incorporating the board, avoid any deformation of the board not to damage the components.
- 8. Avoid the use of excessive force when plugging a connector into a device soldered onto the board.
- 9. Ceramic capacitors must be soldered only by the mode (reflow or wave soldering) permissible for them (see the chapter "Soldering directions").
- 10. When soldering the most gentle solder profile feasible should be selected (heating time, peak temperature, cooling time) in order to avoid thermal stresses and damage.
- 11. Ensure the correct solder meniscus height and solder quantity.
- 12. Ensure correct dosing of the cement quantity.
- 13. Ceramic capacitors with an AgPd external termination are not suited for the lead-free solder process: they were developed only for conductive adhesion technology.

This listing does not claim to be complete, but merely reflects the experience of EPCOS AG.



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