

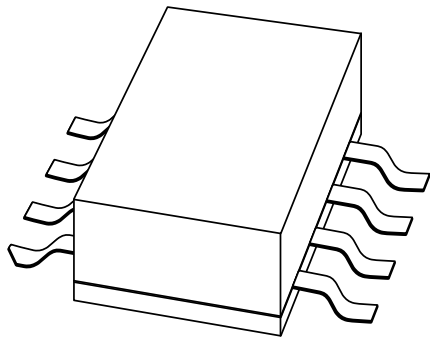
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DATA SHEET



BLF202 HF/VHF power MOS transistor

Product specification
Supersedes data of 1999 Oct 20

2003 Sep 19

HF/VHF power MOS transistor

BLF202

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch.

APPLICATIONS

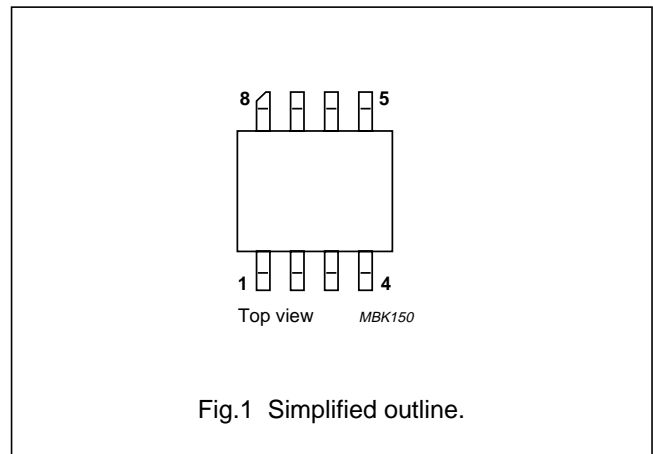
- Communications transmitters in the HF/VHF range with a nominal supply voltage of 12.5 V.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor in an 8-lead SOT409A SMD package with a ceramic cap.

PINNING - SOT409A

PIN	DESCRIPTION
1, 8	source
2, 3	gate
4, 5	source
6, 7	drain



QUICK REFERENCE DATA

RF performance at $T_{mb} = 25\text{ }^\circ\text{C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	2	>10	>50

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

HF/VHF power MOS transistor

BLF202

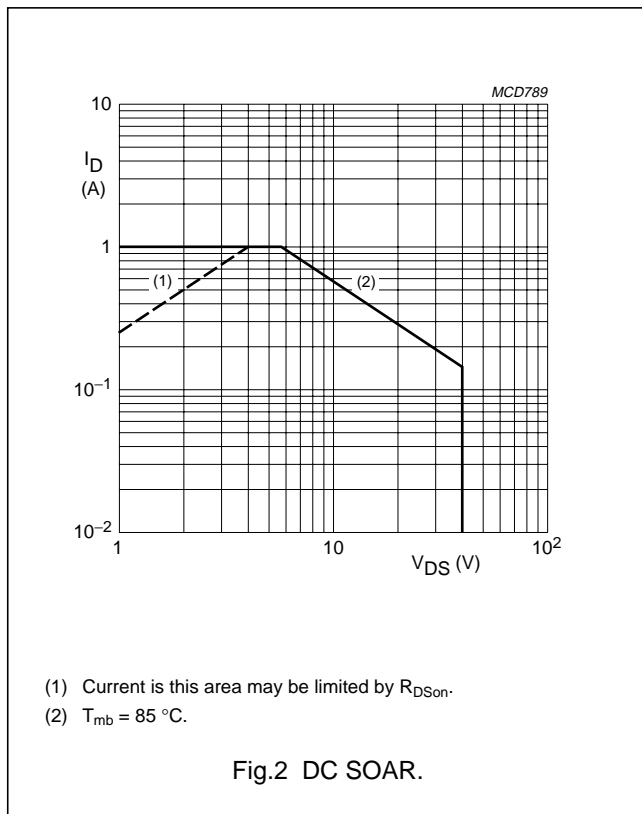
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
V_{GS}	gate-source voltage		–	± 20	V
I_D	drain current (DC)		–	1	A
P_{tot}	total power dissipation	$T_{mb} \leq 85\text{ }^\circ\text{C}$	–	5.7	W
T_{stg}	storage temperature		–65	150	$^\circ\text{C}$
T_j	junction temperature		–	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$T_{mb} \leq 85\text{ }^\circ\text{C}; P_{tot} = 5.7\text{ W}$	20.5	K/W



HF/VHF power MOS transistor

BLF202

CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

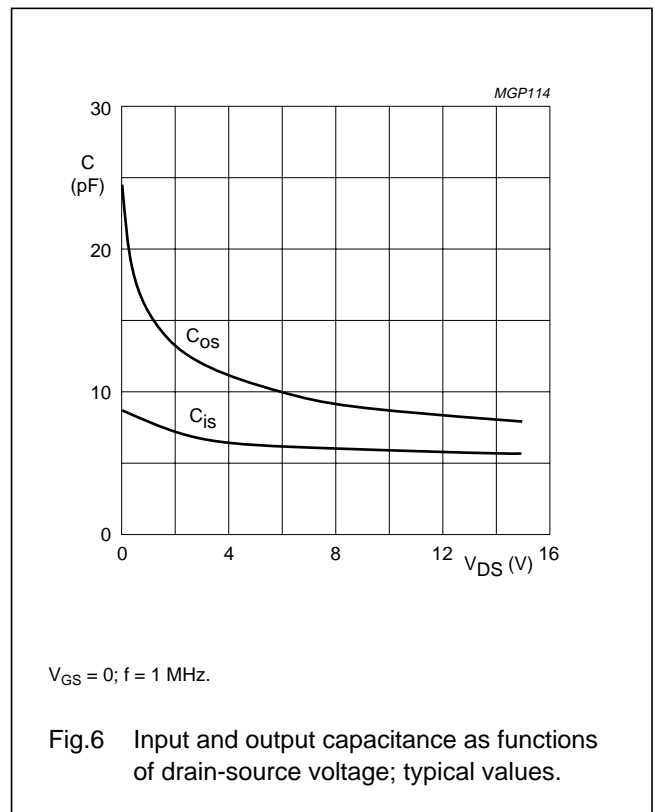
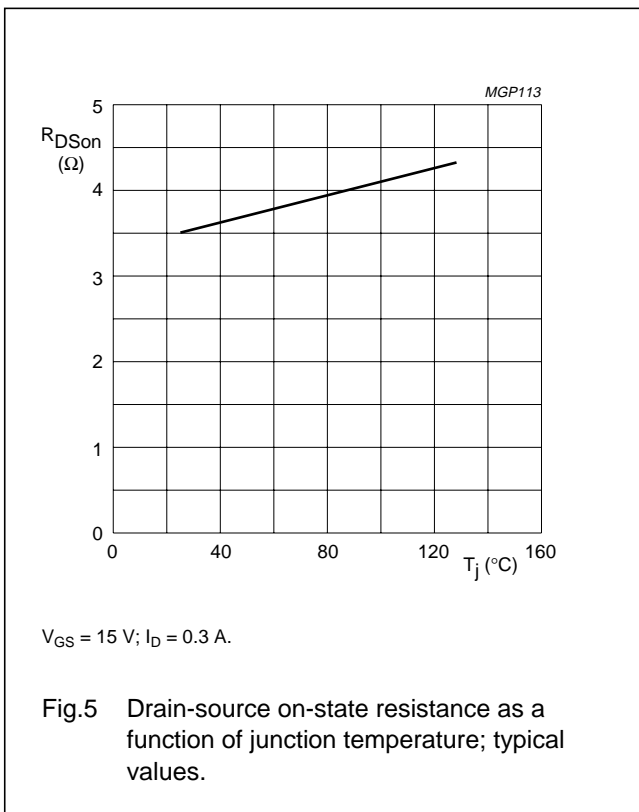
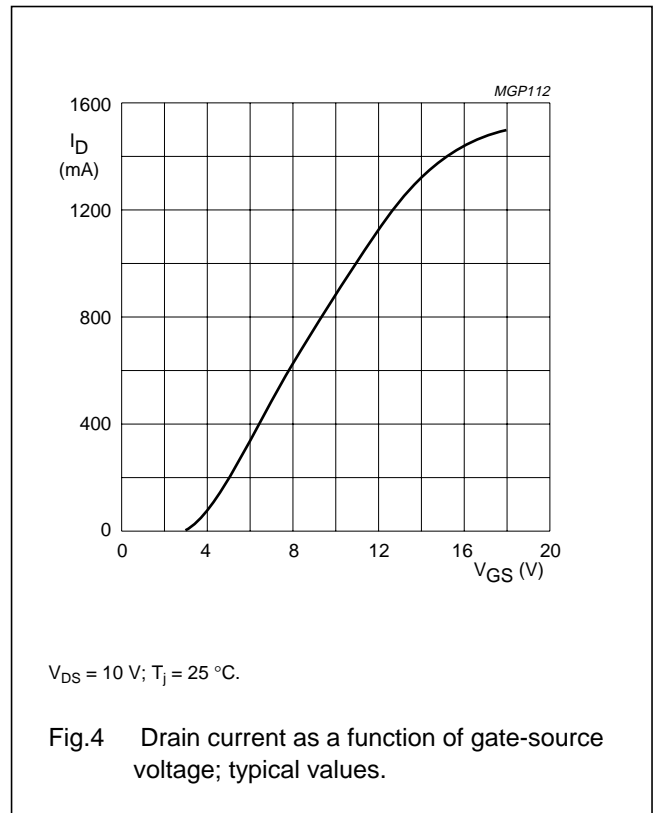
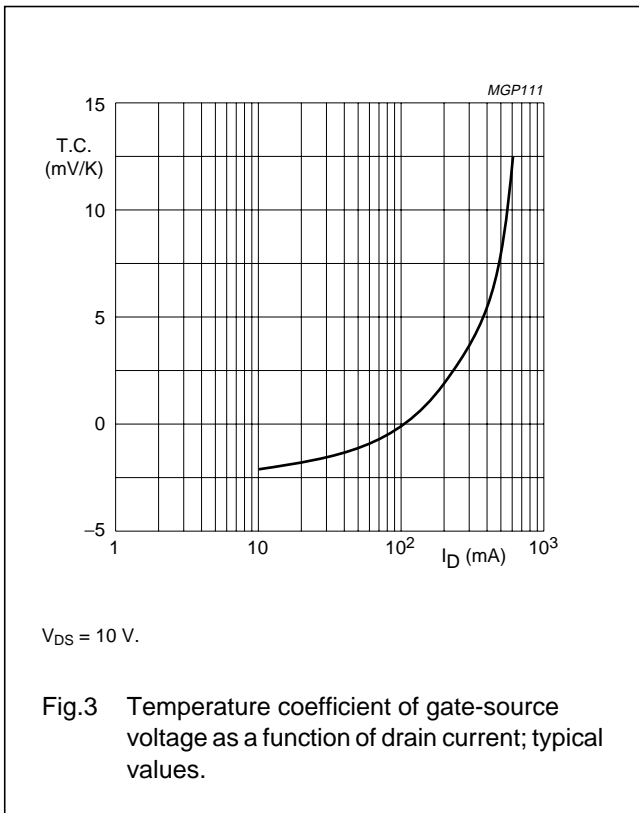
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 3\text{ mA}; V_{GS} = 0$	40	–	–	V
V_{GSth}	gate-source threshold voltage	$I_D = 3\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 12.5\text{ V}$	–	–	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$	–	–	1	μA
I_{DSX}	on-state drain current	$V_{GS} = 15\text{ V}; V_{DS} = 10\text{ V}$	–	1.3	–	A
R_{DSon}	drain-source on-state resistance	$I_D = 0.3\text{ A}; V_{GS} = 15\text{ V}$	–	3.5	4	Ω
g_{fs}	forward transconductance	$I_D = 0.3\text{ A}; V_{DS} = 10\text{ V}$	80	135	–	mS
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 12.5\text{ V}; f = 1\text{ MHz}$	–	5.3	–	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 12.5\text{ V}; f = 1\text{ MHz}$	–	7.8	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 12.5\text{ V}; f = 1\text{ MHz}$	–	1.8	–	pF

 V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			

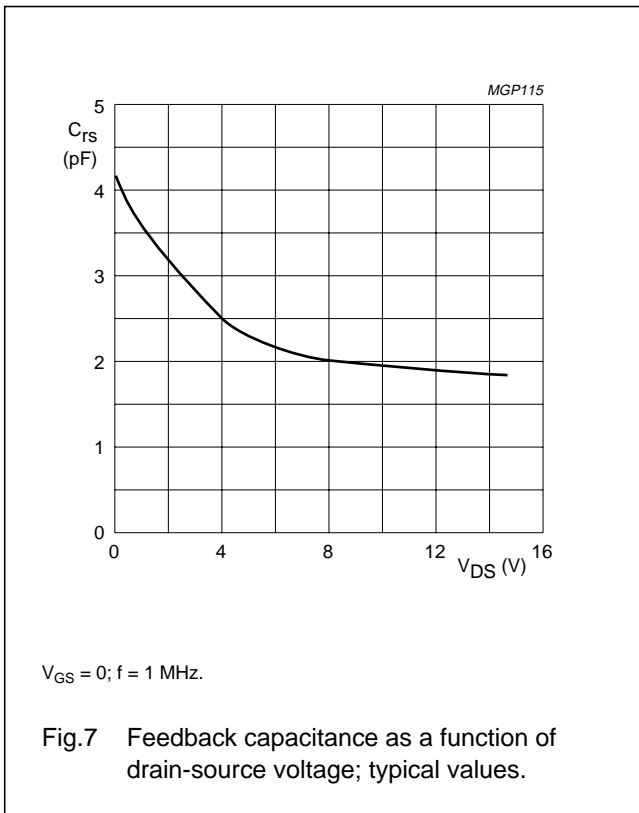
HF/VHF power MOS transistor

BLF202



HF/VHF power MOS transistor

BLF202



APPLICATION INFORMATION FOR CLASS-B OPERATION

$T_{mb} = 25$ °C; $R_{GS} = 237$ Ω ; unless otherwise specified.

RF performance in CW operation in a common source class-B test circuit.

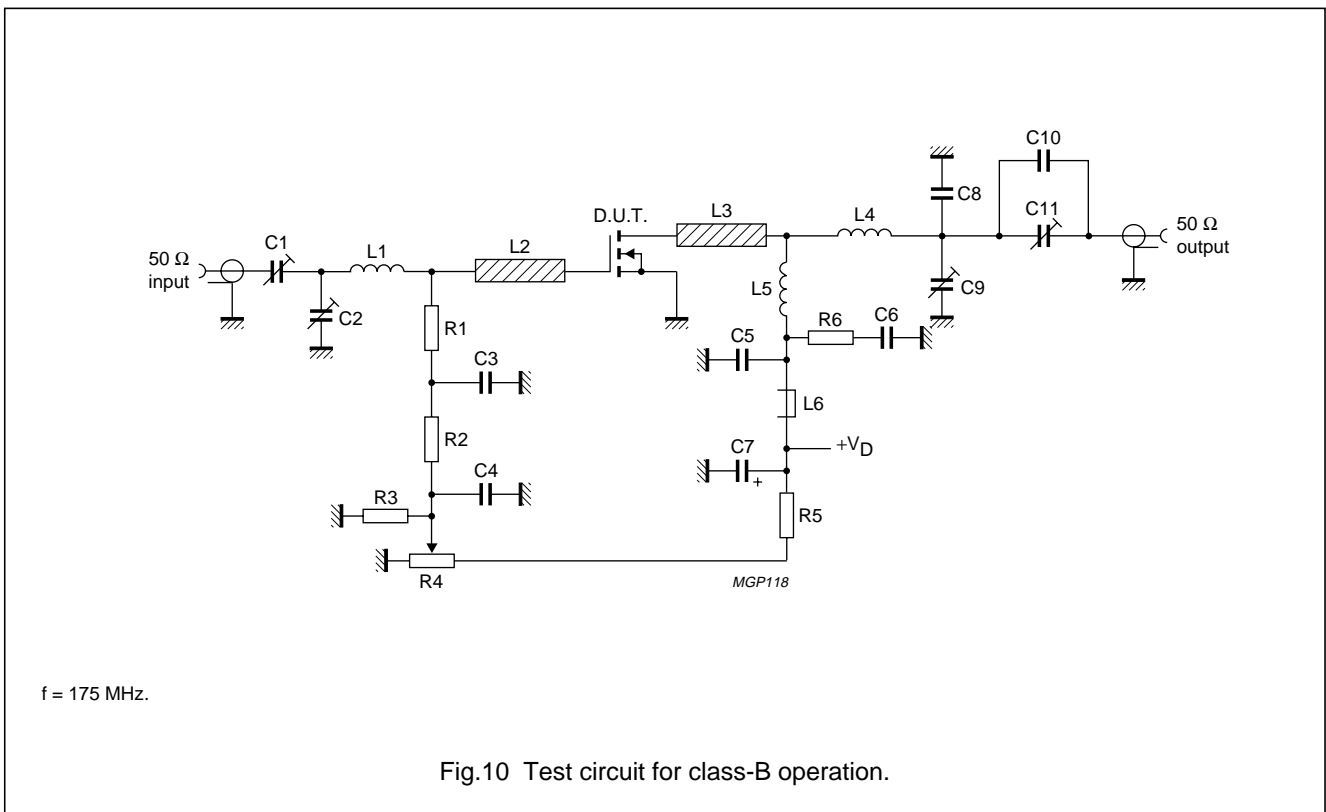
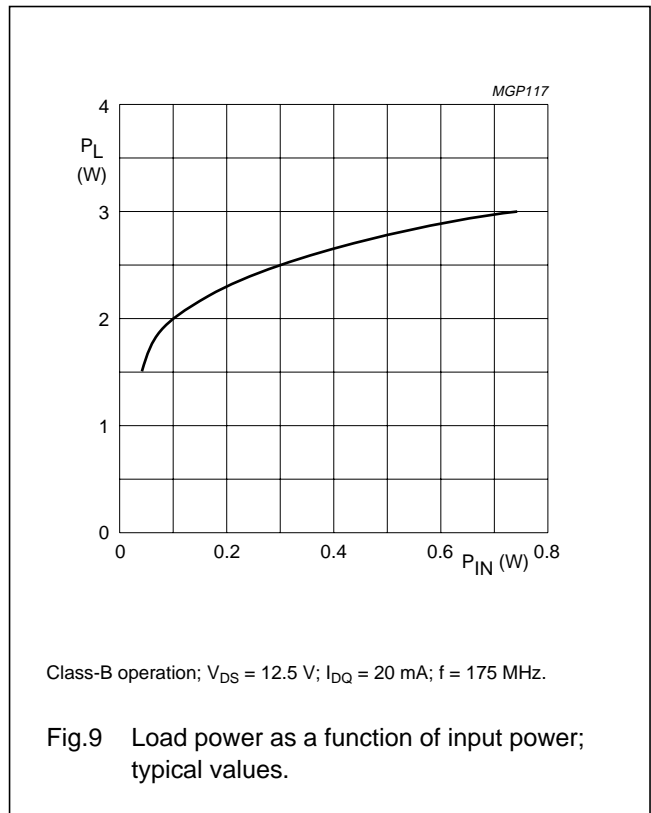
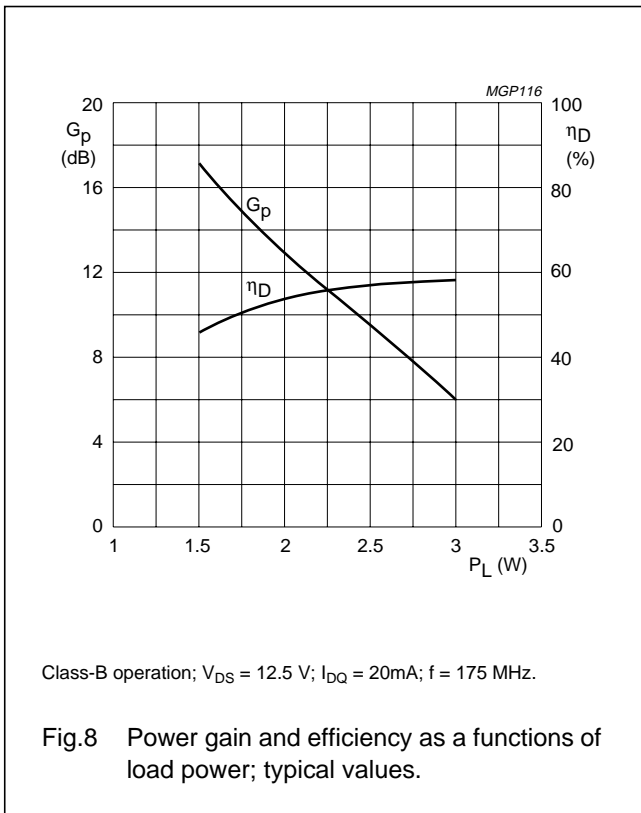
MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	175	12.5	20	2	>10 typ. 13	>50 typ. 55

Ruggedness in class-B operation

The BLF202 is capable of withstanding a load mismatch corresponding to VSWR = 50:1 through all phases under the following conditions: $V_{DS} = 15.5$ V; $f = 175$ MHz at rated load power.

HF/VHF power MOS transistor

BLF202



HF/VHF power MOS transistor

BLF202

List of components (see Fig.10)

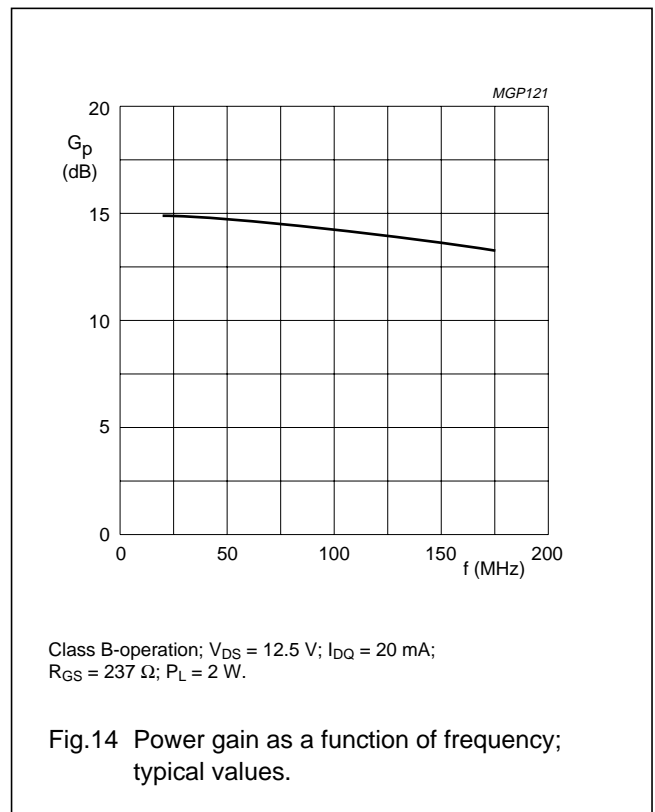
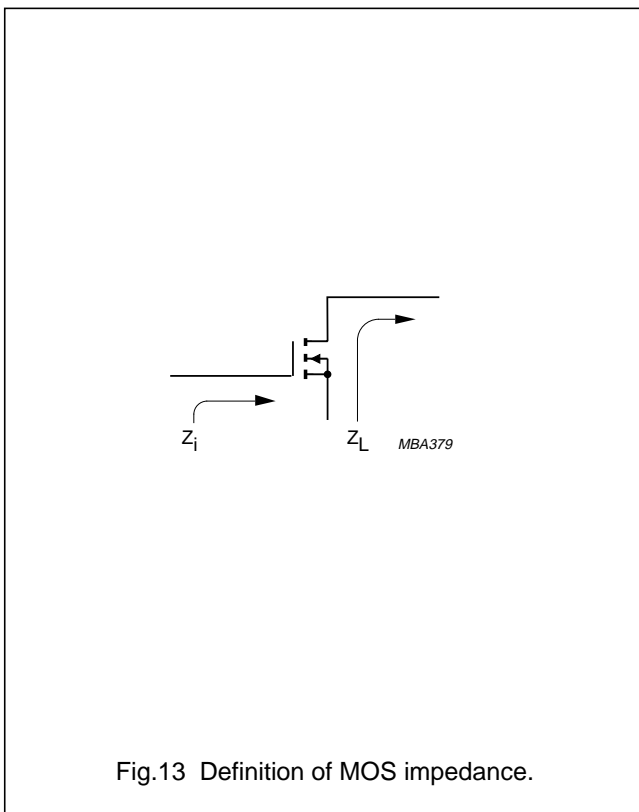
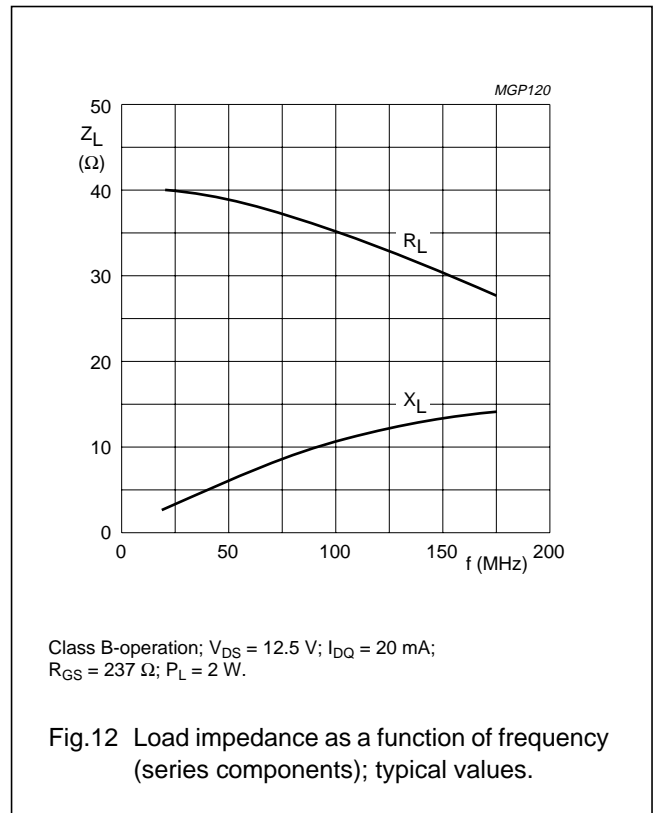
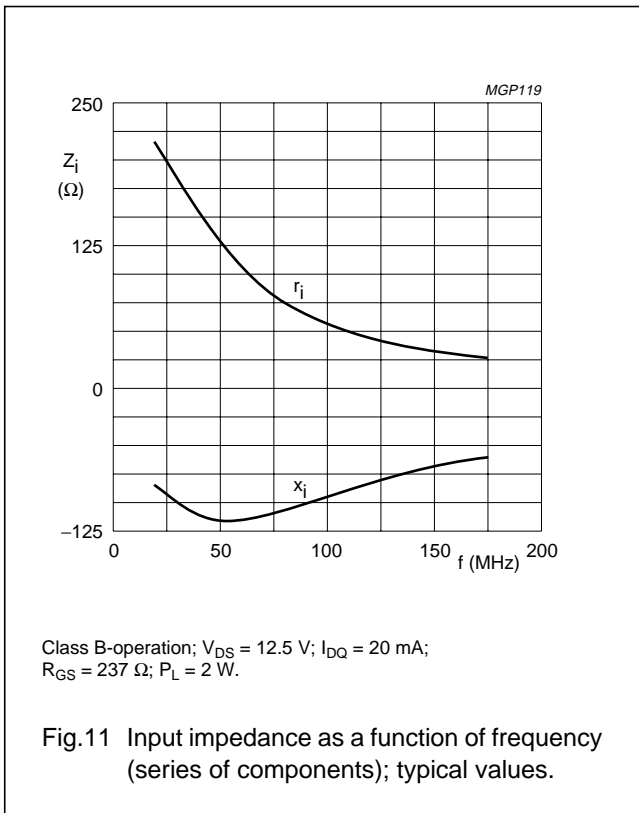
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C11	film dielectric trimmer	2 to 9 pF		2222 809 09005
C2, C9	film dielectric trimmer	2 to 9 pF		2222 809 09002
C3, C5	multilayer ceramic chip capacitor; note 1	1 nF; 500 V		
C4, C6	multilayer ceramic chip capacitor	2 × 100 nF in parallel, 50 V		2222 852 47104
C7	Sprague electrolytic tantalum capacitor	2.2 μF; 35 V		
C8	multilayer ceramic chip capacitor; note 1	5.1 pF; 500 V		
C10	multilayer ceramic chip capacitor; note 1	9.1 pF; 500 V		
L1	8 turns enamelled 0.8 mm copper wire	137 nH	length 5.1 mm; int. dia. 4 mm; leads 2 × 5 mm	
L2, L3	stripline; note 2	81 Ω	8 mm × 2 mm	
L4	3 turns enamelled 1 mm copper wire	57 nH	length 5 mm; int. dia. 6 mm; leads 2 × 5 mm	
L5	9 turns enamelled 1 mm copper wire	355 nH	length 11 mm; int. dia. 7 mm; leads 2 × 5 mm	
L6	grade 3B Ferroxcube RF choke			4312 020 36642
R1	0.4 W metal film resistor	237 Ω		2322 151 72371
R2	0.4 W metal film resistor	1 kΩ		2322 151 71002
R3	0.4 W metal film resistor	1 MΩ		2322 151 71005
R4	10 turns cermet potentiometer	5 kΩ		
R5	0.4 W metal film resistor	7.5 kΩ		2322 151 77502
R6	1 W metal film resistor	10 Ω		2322 153 51009

Notes

- American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
- The striplines are on a double copper-clad printed-circuit board, with PTFE fibre-glass dielectric ($\epsilon_r = 2.2$), thickness 1.6 mm.

HF/VHF power MOS transistor

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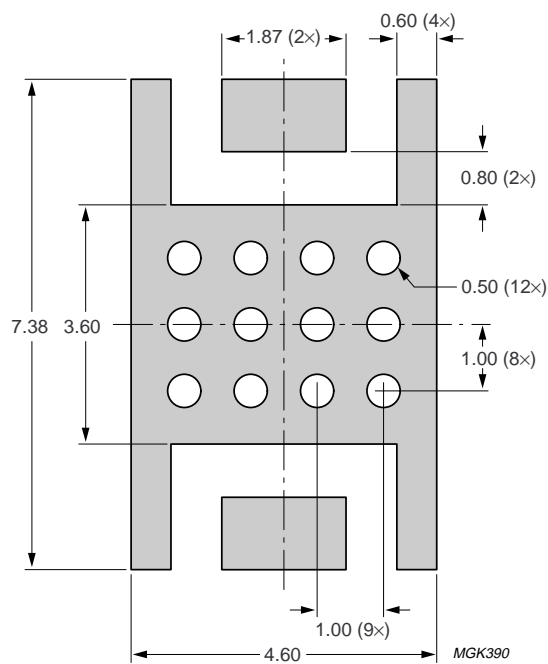
HF/VHF power MOS transistor

BLF202

MOUNTING RECOMMENDATIONS

Both the metallized ground plate and the device leads contribute to the heat flow. It is recommended that the transistor be mounted on a grounded metallized area of the printed-circuit board. This area should be of maximum 0.8 mm thickness and include at least 12 x 0.5 diameter through metallized holes filled with solder.

A thermal resistance $R_{th(mb-h)}$ of 5 K/W can be achieved if heatsink compound is applied when the transistor is mounted on the printed-circuit board.



Dimensions in mm.

Fig.15 Footprint SOT409A.

HF/VHF power MOS transistor

BLF202

BLF202 scattering parameters $V_{DS} = 12.5\text{ V}$; $I_D = 20\text{ mA}$; note 1

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	S ₁₁	∠ Φ	S ₂₁	∠ Φ	S ₁₂	∠ Φ	S ₂₂	∠ Φ
5	1.00	-2.00	5.76	178.30	0.01	88.30	0.97	-2.40
10	1.00	-4.00	5.75	176.50	0.01	86.70	0.97	-4.90
20	1.00	-7.90	5.72	172.90	0.02	83.40	0.97	-9.70
30	0.99	-11.90	5.69	169.40	0.03	80.20	0.97	-14.50
40	0.99	-15.80	5.65	165.90	0.04	77.00	0.96	-19.30
50	0.98	-19.60	5.58	162.40	0.05	73.80	0.96	-23.90
60	0.97	-23.40	5.51	159.00	0.06	70.70	0.95	-28.50
70	0.96	-27.00	5.42	-155.70	0.07	67.70	0.94	-33.00
80	0.94	-30.70	5.33	152.40	0.08	64.80	0.93	-37.40
90	0.93	-34.10	5.23	149.30	0.09	62.00	0.92	-41.60
100	0.92	-37.50	5.12	146.40	0.10	59.40	0.92	-45.60
125	0.89	-45.60	4.86	139.30	0.12	53.10	0.89	-55.30
150	0.85	-53.00	4.58	132.60	0.13	47.20	0.87	-64.10
175	0.82	-59.80	4.29	126.60	0.14	42.00	0.85	-72.00
200	0.79	-66.00	4.03	121.20	0.15	37.70	0.83	-79.20
250	0.74	-77.00	3.55	111.30	0.17	29.30	0.79	-91.70
300	0.70	-86.30	3.15	103.30	0.17	23.10	0.77	-101.90
350	0.68	-94.30	2.80	96.00	0.18	17.30	0.76	-110.30
400	0.66	-101.40	2.52	89.80	0.18	12.90	0.75	-117.20
450	0.64	-107.80	2.27	83.80	0.18	8.60	0.74	-123.20
500	0.64	-113.50	2.07	78.80	0.18	5.20	0.74	-128.30
600	0.63	-123.80	1.75	69.60	0.17	-0.70	0.74	-136.60
700	0.64	-132.60	1.51	61.40	0.15	-5.30	0.75	-143.20
800	0.65	-140.60	1.32	54.40	0.14	-8.20	0.76	-148.60
900	0.67	-148.10	1.16	48.20	0.12	-9.70	0.77	-153.30
1000	0.68	-155.00	1.04	42.90	0.11	-9.20	0.78	-157.40

Note

- For more extensive s-parameters see internet:
<http://www.semiconductors.philips.com/markets/communications/wirelesscommunications/broadcast>.

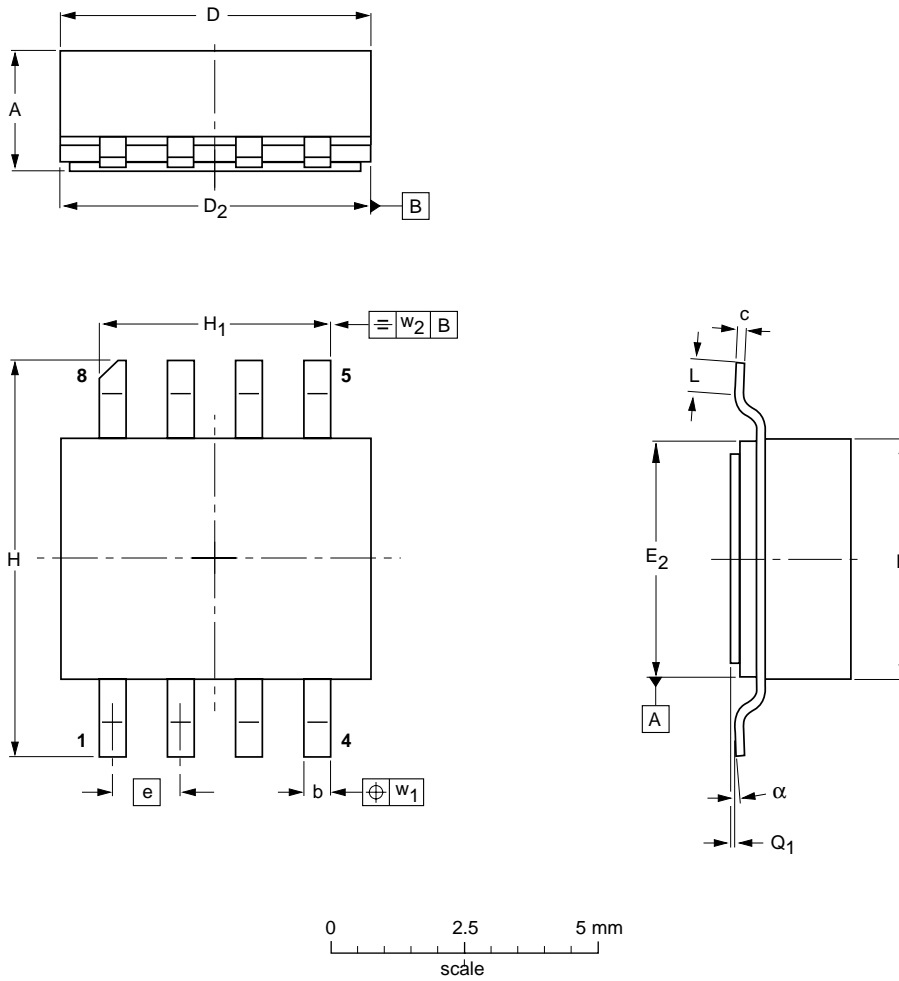
HF/VHF power MOS transistor

BLF202

PACKAGE OUTLINE

Ceramic surface mounted package; 8 leads

SOT409A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₂	E	E ₂	e	H	H ₁	L	Q ₁	w ₁	w ₂	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						98-01-27

HF/VHF power MOS transistor

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Printed in The Netherlands

613524/02/pp14

Date of release: 2003 Sep 19

Document order number: 9397 750 11595

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