阅读申明

1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描叙上的差异，建议读者做出适当判断。
4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.

2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader’ s learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.

3. All product information provided on the website refer to solutions from manufacturers’ technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.

4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with “Datasheets”.

N-channel dual-gate MOS-FET BF909AWR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

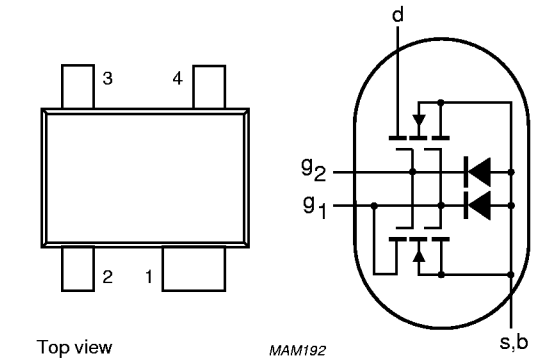
- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communication equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



Marking code: MG.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	280	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	3.6	4.3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C; see Fig.2; note 1	–	280	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.

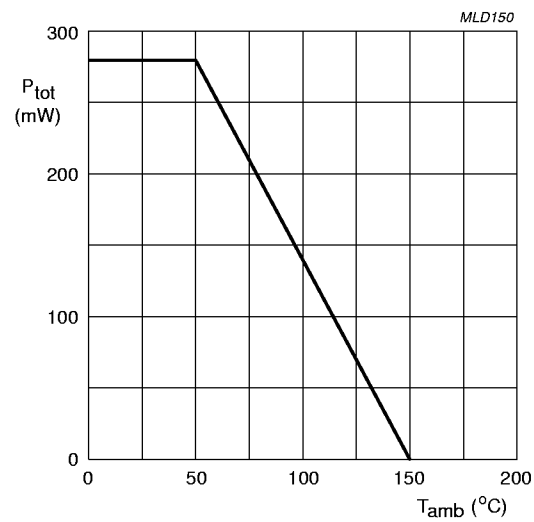


Fig.2 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. Soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = V_{DS} = 5 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	12	20	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G2\text{-}S}$ = V_{DS} = 0; $V_{G1\text{-}S}$ = 5 V	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G1\text{-}S}$ = V_{DS} = 0; $V_{G2\text{-}S}$ = 5 V	–	50	nA

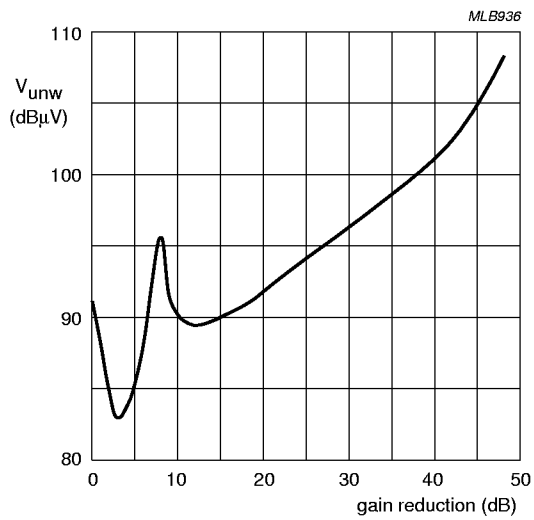
Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V.

DYNAMIC CHARACTERISTICS

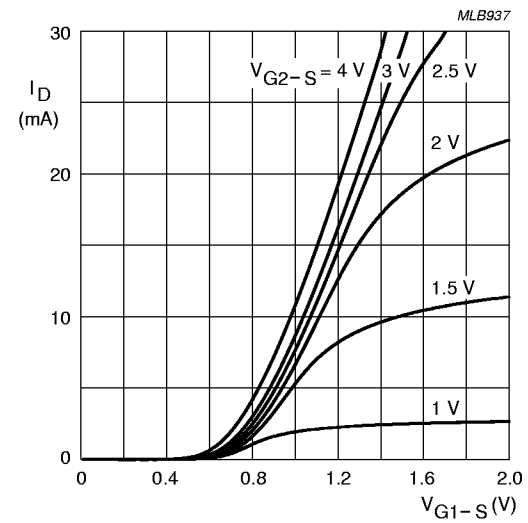
Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	3.6	4.3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	2.3	3	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	2.4	3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	30	50	fF
F	noise figure	f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	2	2.8	dB



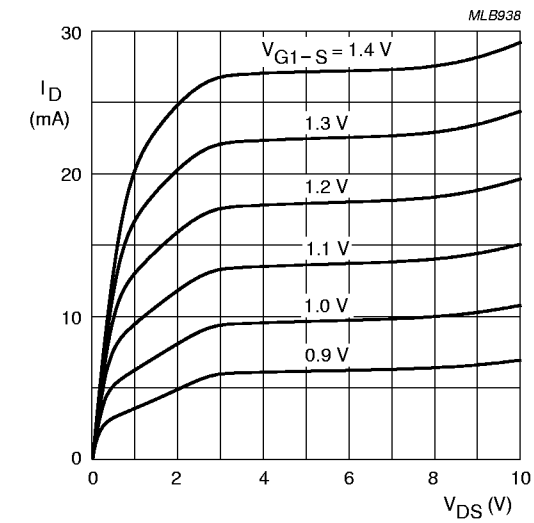
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.3 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.17.



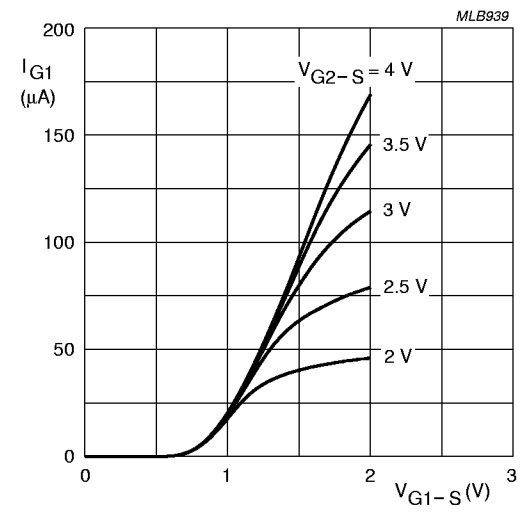
V_{DS} = 5 V; T_j = 25 °C.

Fig.4 Transfer characteristics; typical values.



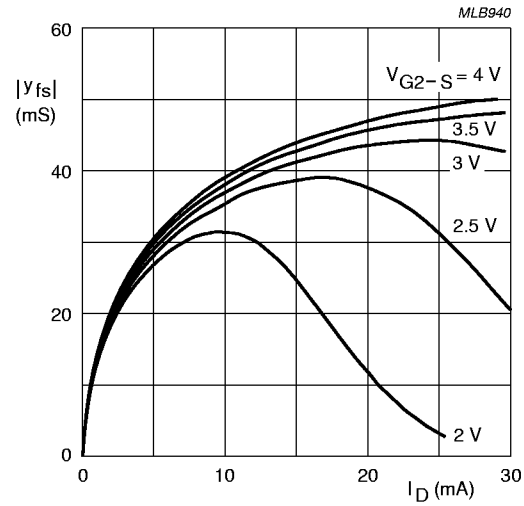
V_{G2-S} = 4 V; T_j = 25 °C.

Fig.5 Output characteristics; typical values.



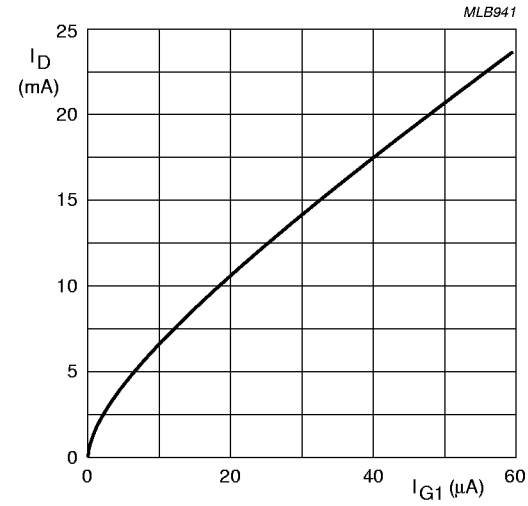
V_{DS} = 5 V; T_j = 25 °C.

Fig.6 Gate 1 current as a function of gate 1 voltage; typical values.



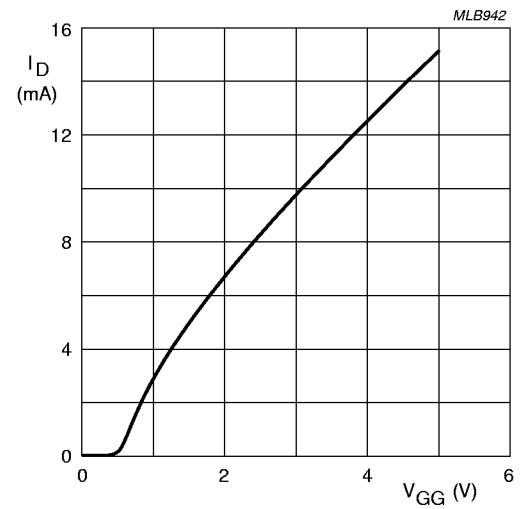
V_{DS} = 5 V; T_j = 25 °C.

Fig.7 Forward transfer admittance as a function of drain current; typical values.



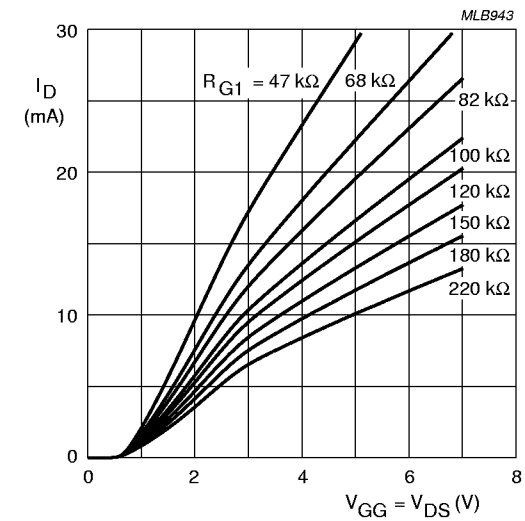
V_{DS} = 5 V; V_{G2-S} = 4 V; T_j = 25 °C.

Fig.8 Drain current as a function of gate 1 current; typical values.



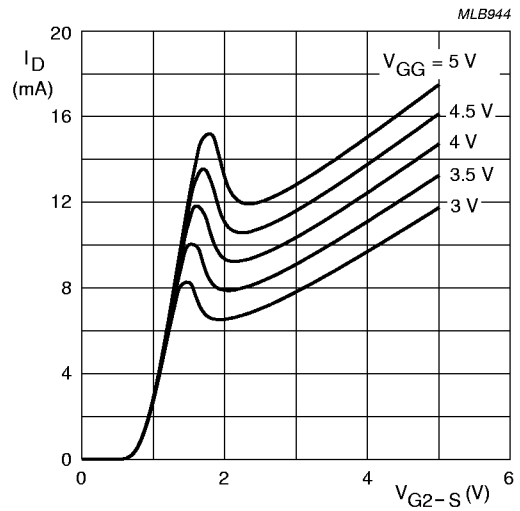
V_{DS} = 5 V; V_{G2-S} = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.17.



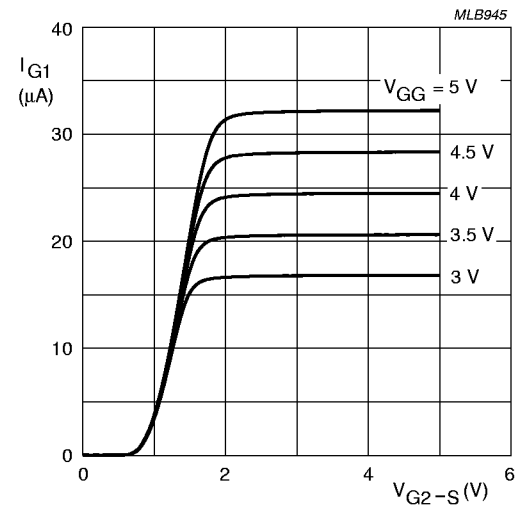
V_{G2-S} = 4 V; R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.17.



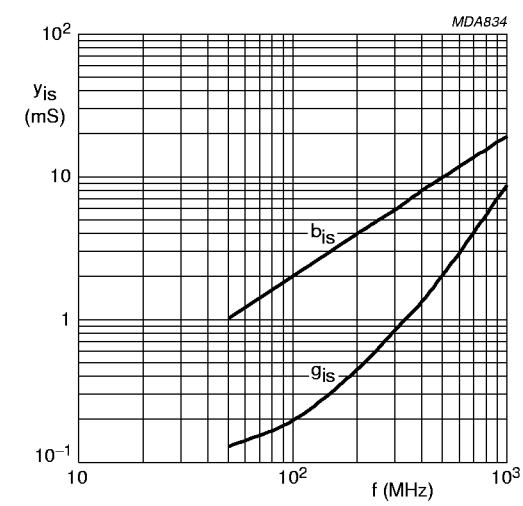
V_{DS} = 5 V; T_j = 25 °C; R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.11 Drain current as a function of gate 2 voltage; typical values; see Fig.17.



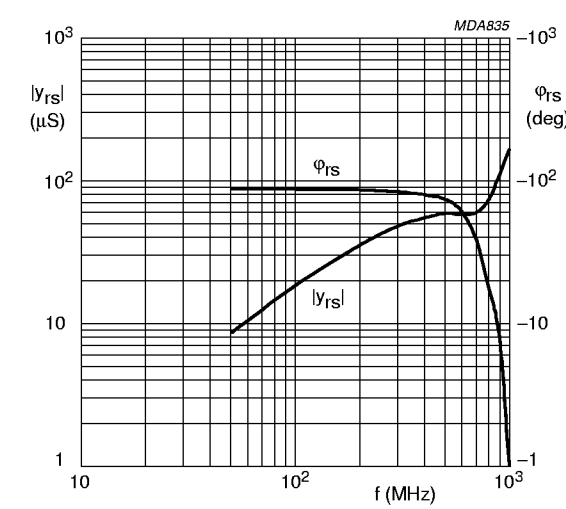
V_{DS} = 5 V; T_j = 25 °C; R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.12 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.17.



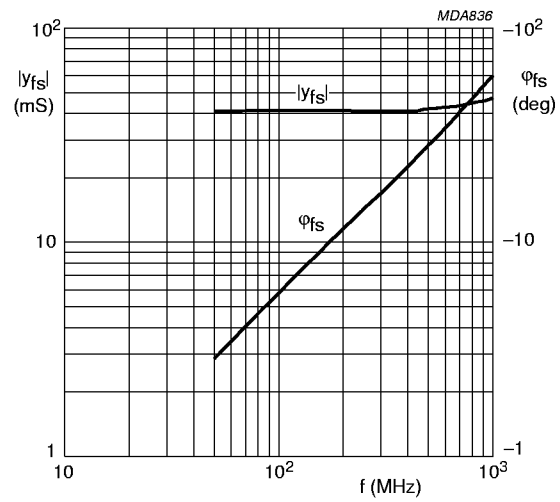
V_{DS} = 5 V; V_{G2} = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.13 Input admittance as a function of frequency; typical values.



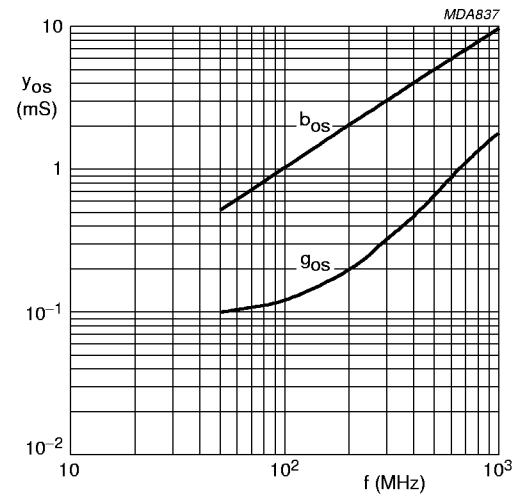
V_{DS} = 5 V; V_{G2} = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V; I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Output admittance as a function of frequency; typical values.

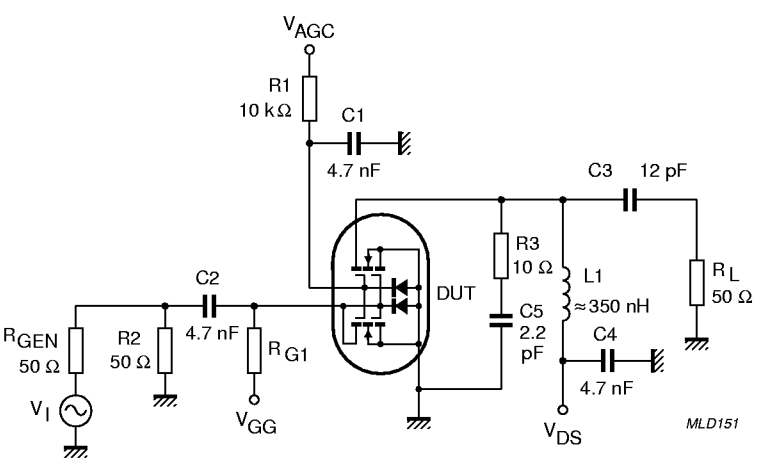


Fig.17 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C

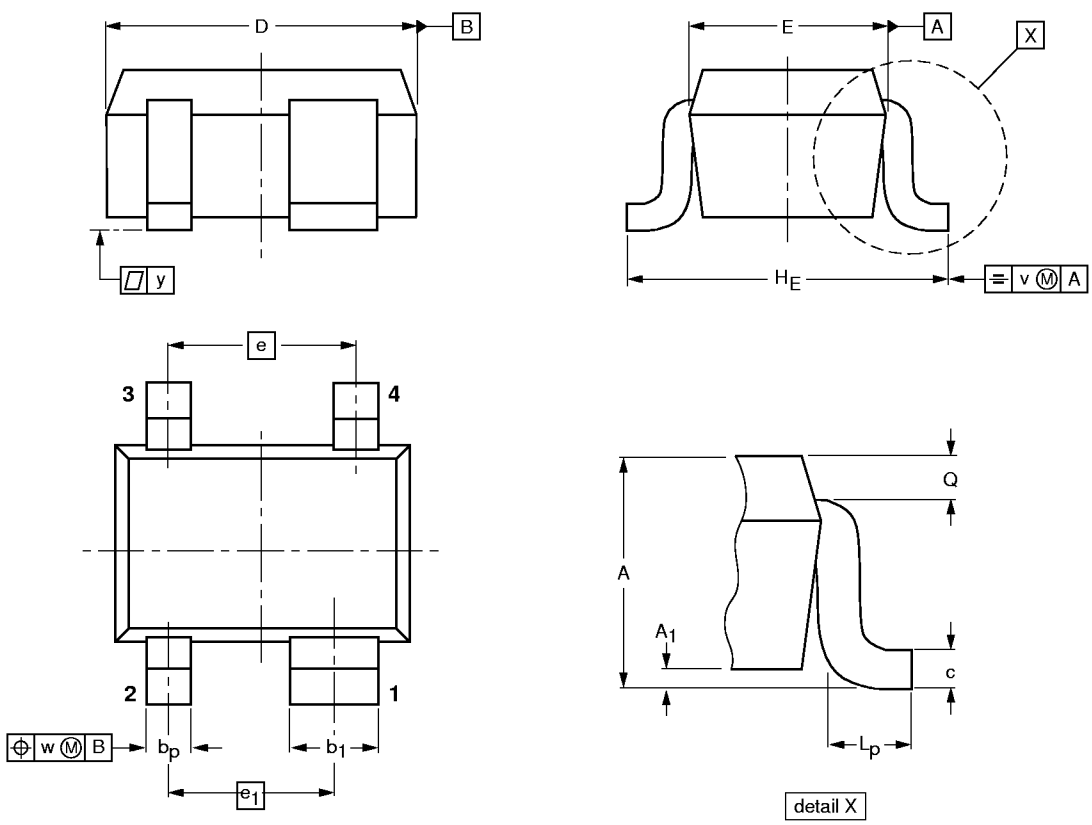
f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	−6.0	4.070	172.7	0.001	86.9	0.989	−3.1
100	0.980	−11.8	4.041	165.4	0.002	82.9	0.987	−6.1
200	0.956	−23.0	3.897	151.3	0.003	73.4	0.978	−12.1
300	0.911	−33.3	3.654	136.9	0.004	70.6	0.962	−17.7
400	0.888	−44.2	3.531	125.4	0.005	67.4	0.951	−23.3
500	0.845	−53.5	3.265	113.4	0.005	66.6	0.934	−28.6
600	0.803	−62.3	3.055	102.3	0.005	75.0	0.917	−33.6
700	0.758	−70.9	2.836	91.3	0.004	93.1	0.902	−38.5
800	0.719	−78.8	2.653	80.9	0.004	115.2	0.889	−43.5
900	0.683	−86.4	2.456	70.9	0.006	132.7	0.878	−48.3
1000	0.653	−93.9	2.299	61.4	0.008	141.0	0.870	−53.3

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

PACKAGE OUTLINE

Plastic surface mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21