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NSBA114EDXV6T1, NSBA114EDXV6T5

Preferred Devices

Dual Bias Resistor Transistors

PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSBA114EDXV6T1 series, two BRT devices are housed in the SOT-563 package which is ideal for low-power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- Lead Free Solder Plating

MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-50	Vdc
Collector-Emitter Voltage	V_{CEO}	-50	Vdc
Collector Current	I_C	-100	mA dc

THERMAL CHARACTERISTICS

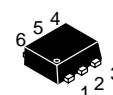
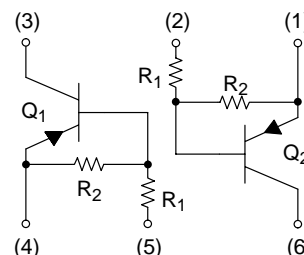
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C/W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C/W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad



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<http://onsemi.com>



SOT-563
CASE 463A
PLASTIC

MARKING DIAGRAM



xx = Specific Device Code
(see table on page 2)
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping
NSBA114EDXV6T1	SOT-563	4 mm pitch 4000/Tape & Reel
NSBA114EDXV6T5	SOT-563	2 mm pitch 8000/Tape & Reel

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

NSBA114EDXV6T1, NSBA114EDXV6T5

DEVICE MARKING AND RESISTOR VALUES

Device	Package	Marking	R1 (k Ω)	R2 (k Ω)
NSBA114EDXV6T1	SOT-563	0A	10	10
NSBA124EDXV6T1	SOT-563	0B	22	22
NSBA144EDXV6T1	SOT-563	0C	47	47
NSBA114YDXV6T1	SOT-563	0D	10	47
NSBA114TDXV6T1 (Notes 2)	SOT-563	0E	10	∞
NSBA143TDXV6T1 (Notes 2)	SOT-563	0F	4.7	∞
NSBA113EDXV6T1 (Notes 2)	SOT-563	0G	1.0	1.0
NSBA123EDXV6T1 (Notes 2)	SOT-563	0H	2.2	2.2
NSBA143EDXV6T1 (Notes 2)	SOT-563	0J	4.7	4.7
NSBA143ZDXV6T1 (Notes 2)	SOT-563	0K	4.7	47
NSBA124XDXV6T1 (Notes 2)	SOT-563	0L	22	47
NSBA123JDXV6T1 (Notes 2)	SOT-563	0M	2.2	47
NSBA115EDXV6T1 (Notes 2)	SOT-563	0N	100	100
NSBA144WDXV6T1 (Notes 2)	SOT-563	0P	47	22

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q₁ and Q₂)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Base Cutoff Current ($V_{CB} = -50\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	–100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = -50\text{ V}$, $I_B = 0$)	I_{CEO}	–	–	–500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = -6.0\text{ V}$, $I_C = 0$)	I_{EBO}	–	–	–0.5	mAdc
NSBA114EDXV6T1		–	–	–0.2	
NSBA124EDXV6T1		–	–	–0.1	
NSBA144EDXV6T1		–	–	–0.2	
NSBA114YDXV6T1		–	–	–0.9	
NSBA114TDXV6T1		–	–	–1.9	
NSBA143TDXV6T1		–	–	–4.3	
NSBA113EDXV6T1		–	–	–2.3	
NSBA123EDXV6T1		–	–	–1.5	
NSBA143EDXV6T1		–	–	–0.18	
NSBA143ZDXV6T1		–	–	–0.13	
NSBA124XDXV6T1		–	–	–0.2	
NSBA123JDXV6T1		–	–	–0.05	
NSBA115EDXV6T1		–	–	–0.13	
NSBA144WDXV6T1		–	–		
Collector-Base Breakdown Voltage ($I_C = -10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	–50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 3) ($I_C = -2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	–50	–	–	Vdc

ON CHARACTERISTICS (Note 3)

Collector-Emitter Saturation Voltage ($I_C = -10\text{ mA}$, $I_E = -0.3\text{ mA}$) ($I_C = -10\text{ mA}$, $I_B = -5\text{ mA}$) NSBA113EDXV6T1/NSBA123EDXV6T1 ($I_C = -10\text{ mA}$, $I_B = -1\text{ mA}$) NSBA114TDXV6T1/NSBA143TDXV6T1 NSBA143EDXV6T1/NSBA143ZDXV6T1/NSBA124XDXV6T1	$V_{CE(sat)}$	–	–	–0.25	Vdc
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2. New resistor combinations. Updated curves to follow in subsequent data sheets.
3. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

NSBA114EDXV6T1, NSBA114EDXV6T5

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q_1 and Q_2) (continued)

[illegible]

2. New resistor combinations. Updated curves to follow in subsequent data sheets.

3. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2.0\%$

NSBA114EDXV6T1, NSBA114EDXV6T5

ALL NSBA114EDXV6T1 SERIES DEVICES

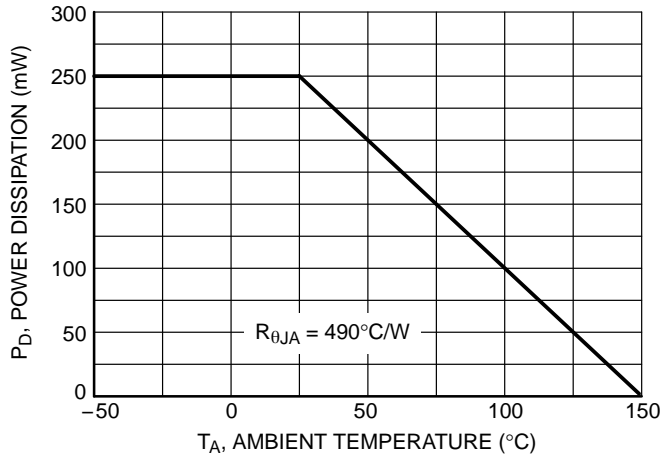


Figure 1. Derating Curve – ALL DEVICES

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114EDXV6T1

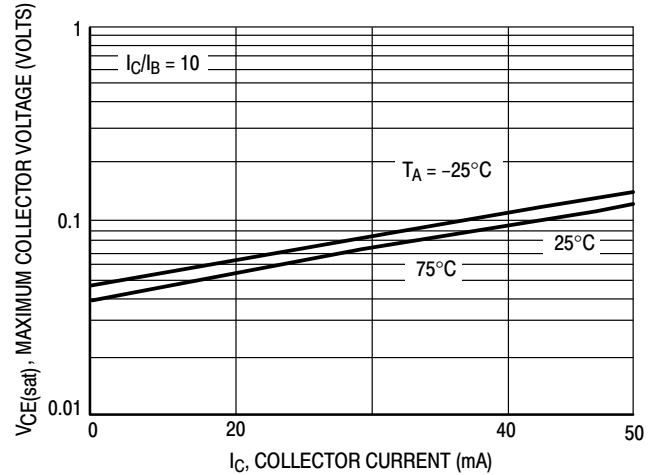


Figure 2. $V_{CE(sat)}$ versus I_C

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114EDXV6T1

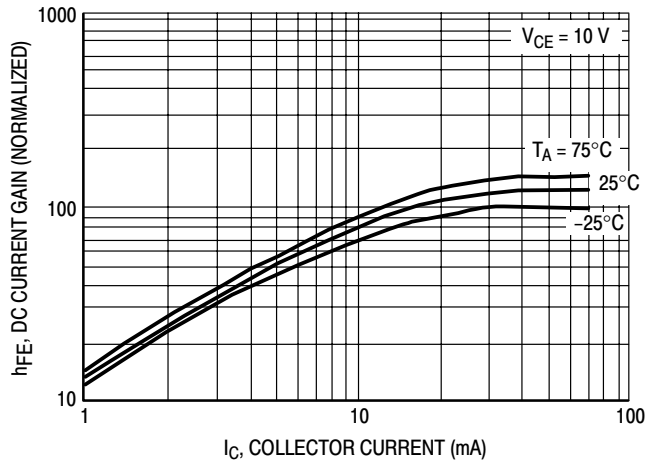


Figure 3. DC Current Gain

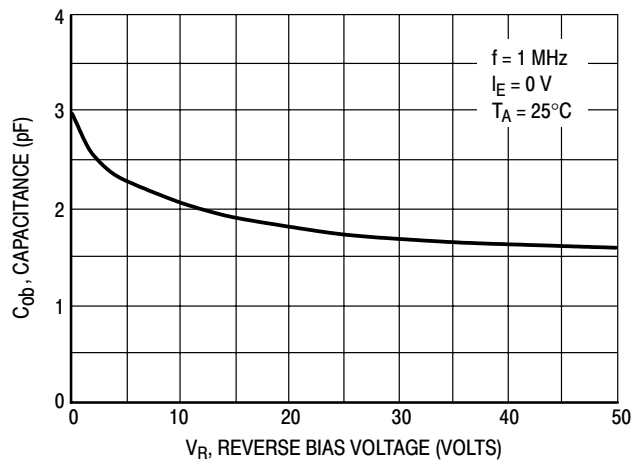


Figure 4. Output Capacitance

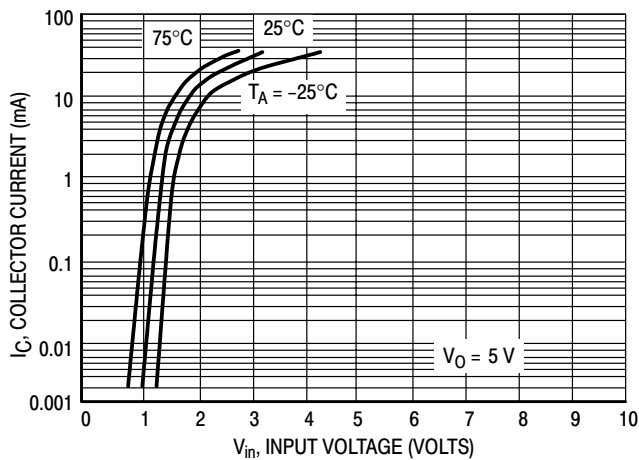


Figure 5. Output Current versus Input Voltage

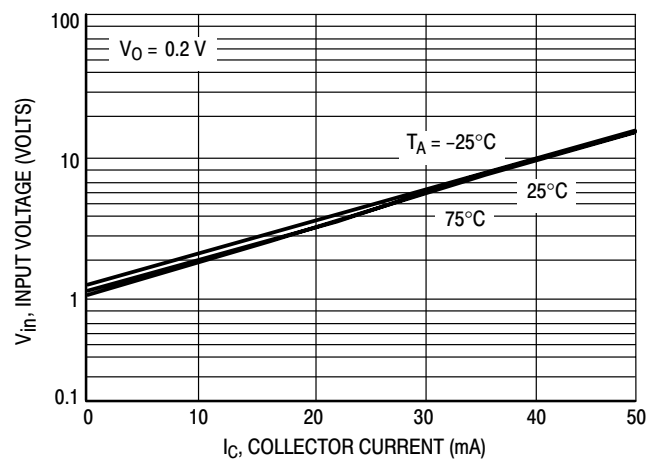


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA124EDXV6T1

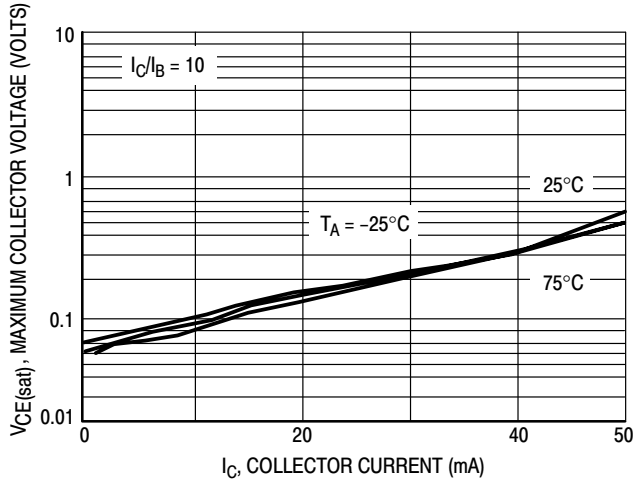


Figure 7. $V_{CE(sat)}$ versus I_C

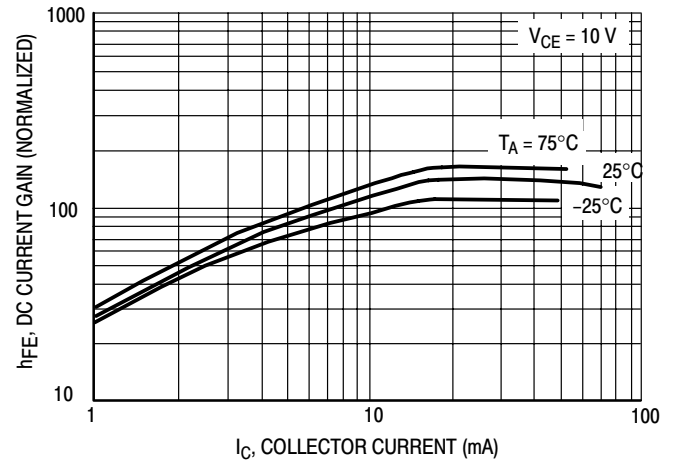


Figure 8. DC Current Gain

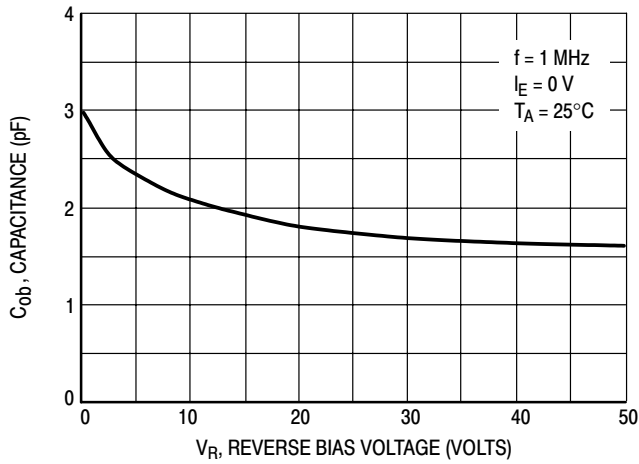


Figure 9. Output Capacitance

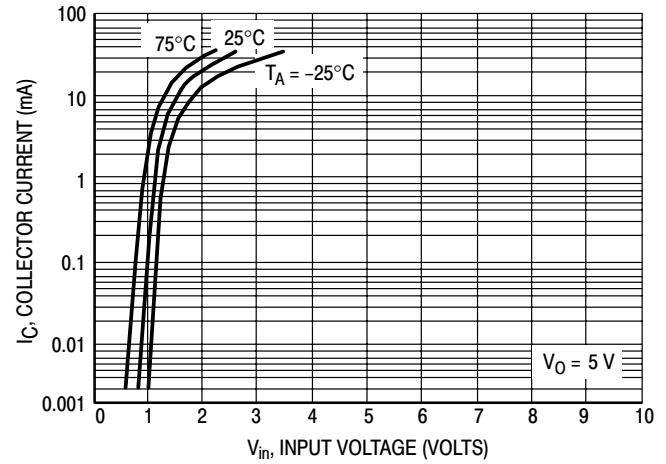


Figure 10. Output Current versus Input Voltage

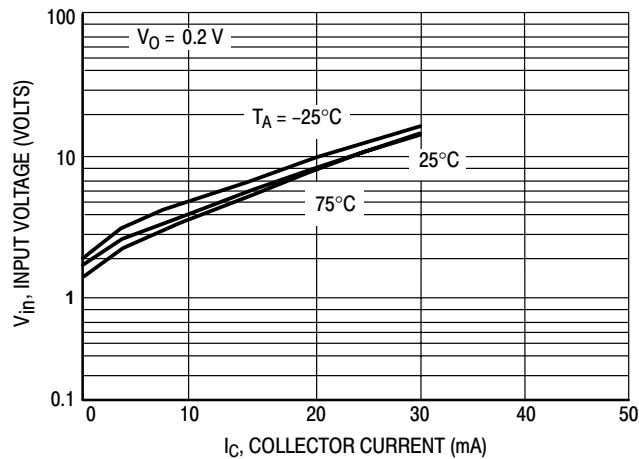


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA144EDXV6T1

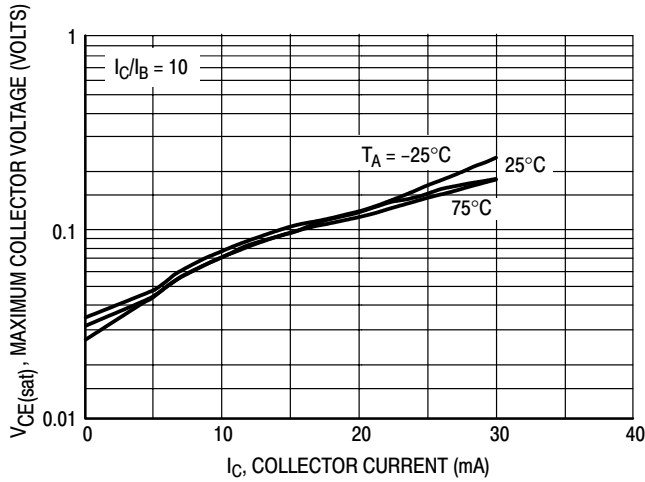


Figure 12. $V_{CE(sat)}$ versus I_C

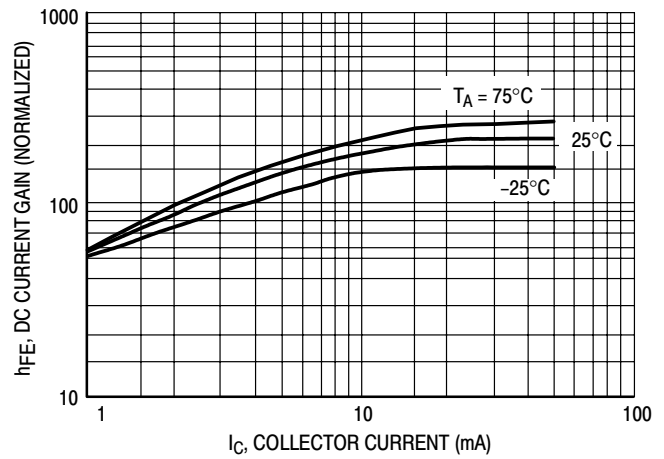


Figure 13. DC Current Gain

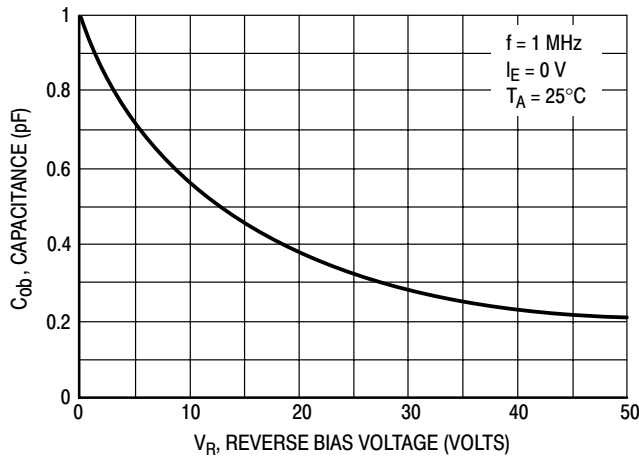


Figure 14. Output Capacitance

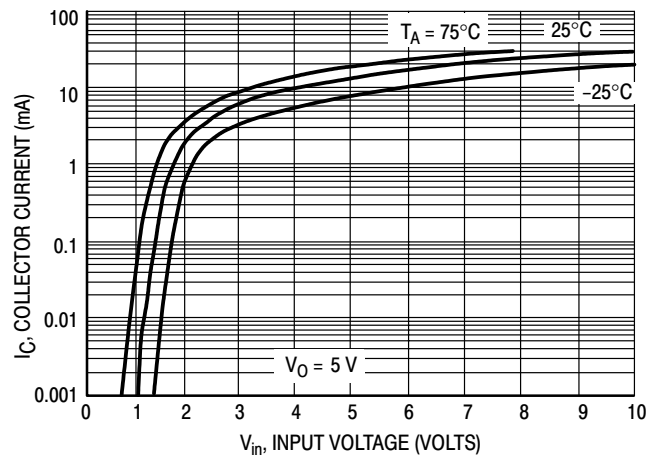


Figure 15. Output Current versus Input Voltage

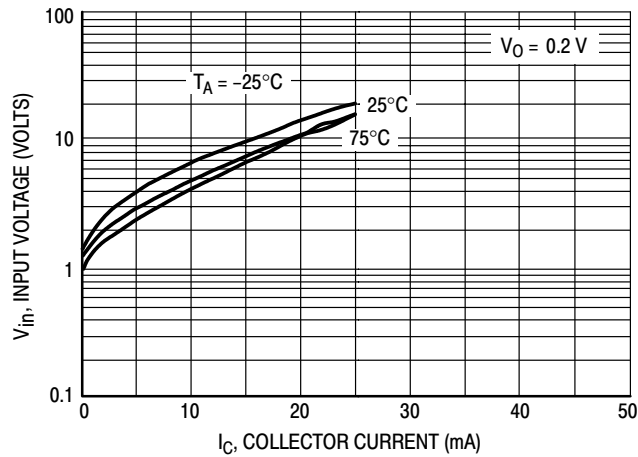


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114YDXV6T1

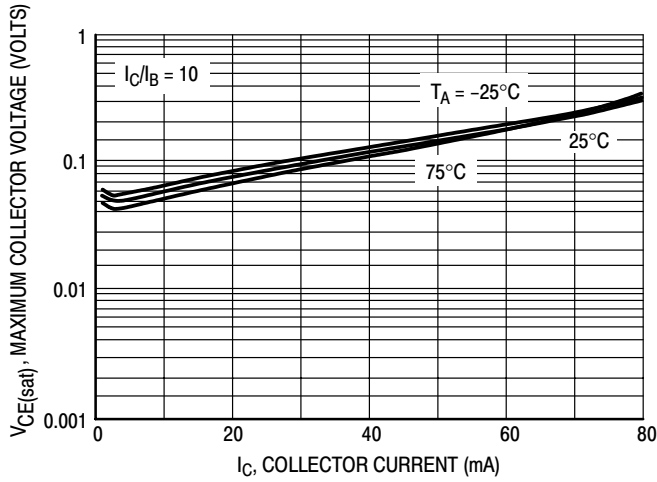


Figure 17. $V_{CE(sat)}$ versus I_C

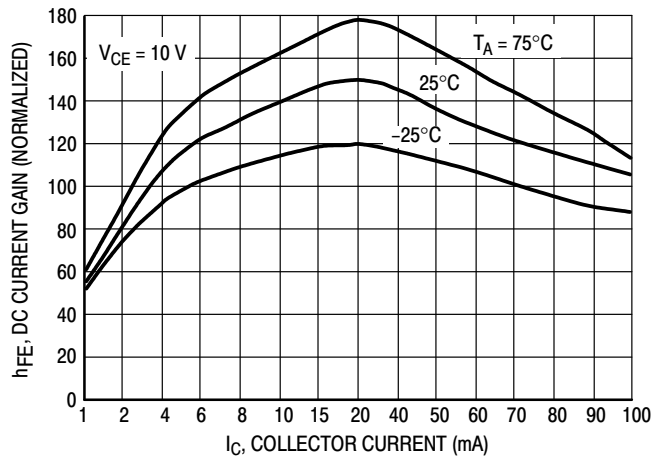


Figure 18. DC Current Gain

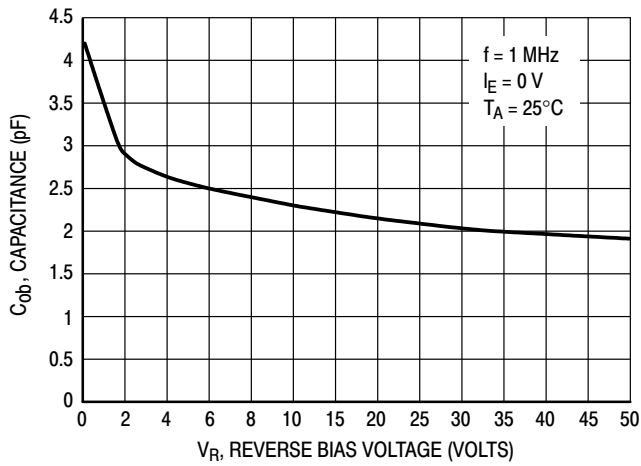


Figure 19. Output Capacitance

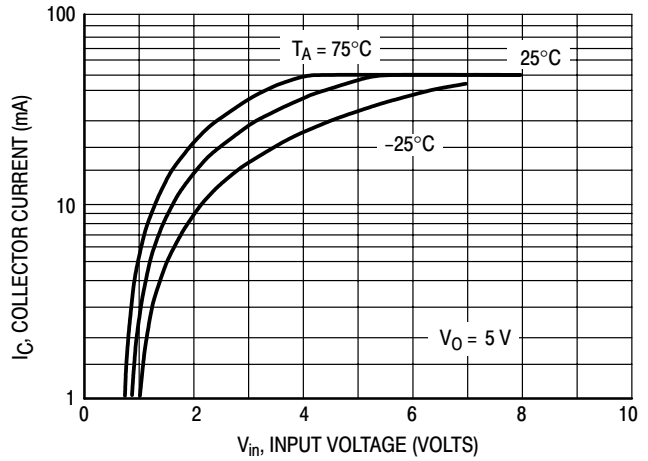


Figure 20. Output Current versus Input Voltage

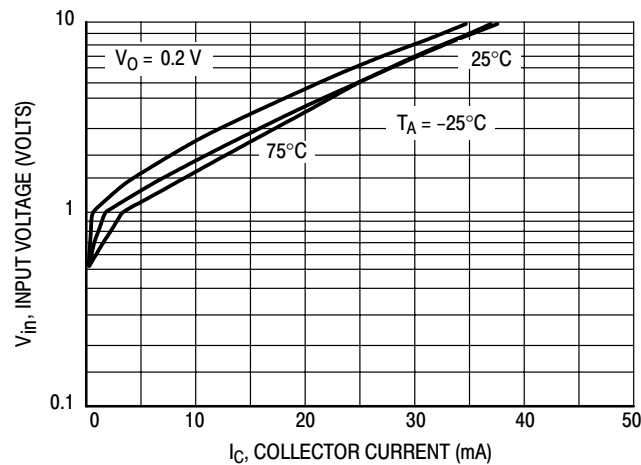


Figure 21. Input Voltage versus Output Current

NSBA114EDXV6T1, NSBA114EDXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA114TDXV6T1

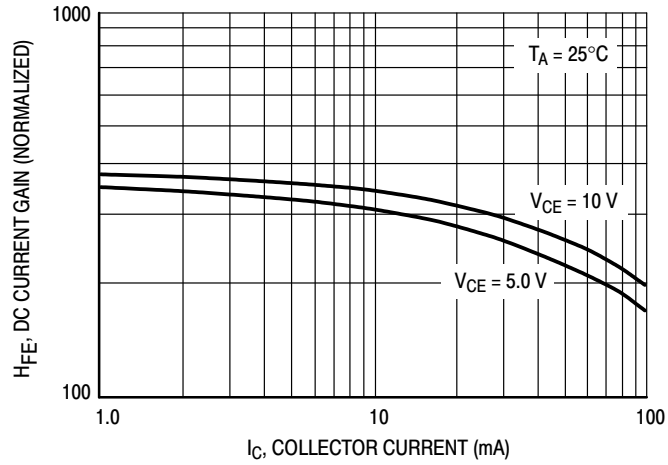


Figure 22. DC Current Gain

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA143TDXV6T1

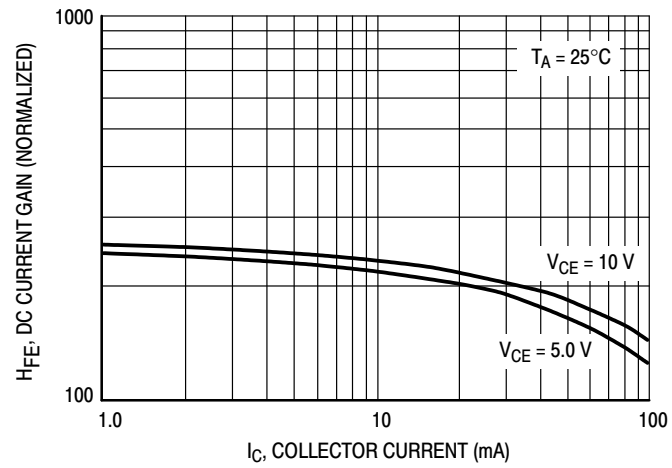


Figure 23. DC Current Gain

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA115EDXV6T1

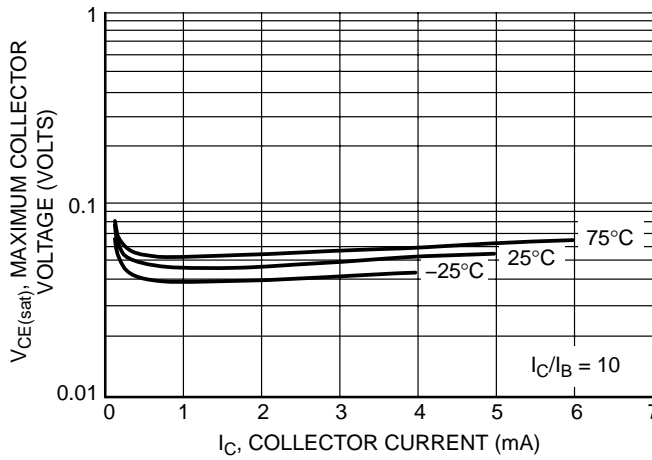


Figure 24. Maximum Collector Voltage versus Collector Current

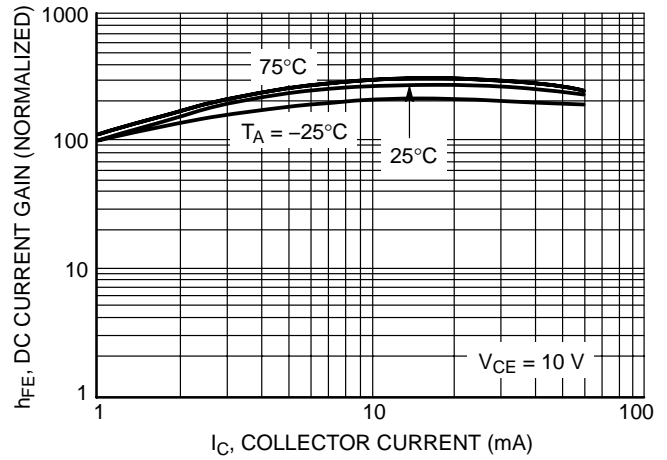


Figure 25. DC Current Gain

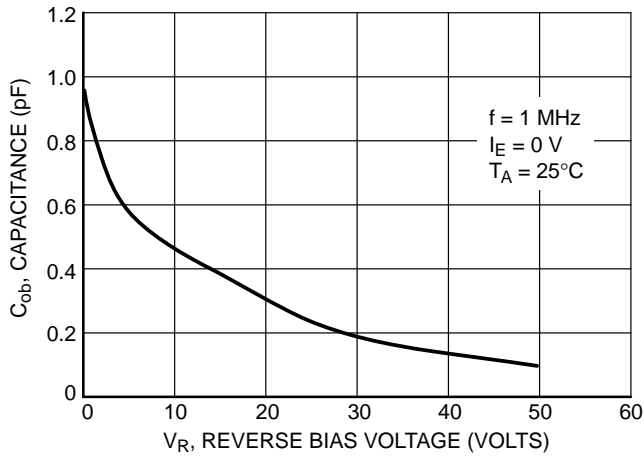


Figure 26. Output Capacitance

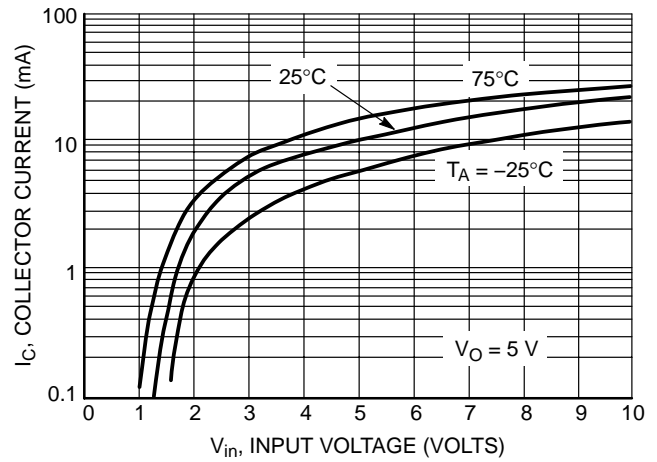


Figure 27. Output Current versus Input Voltage

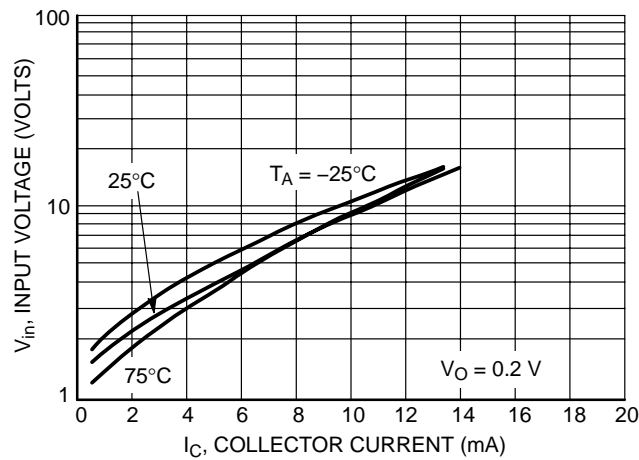


Figure 28. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBA144WDXV6T1

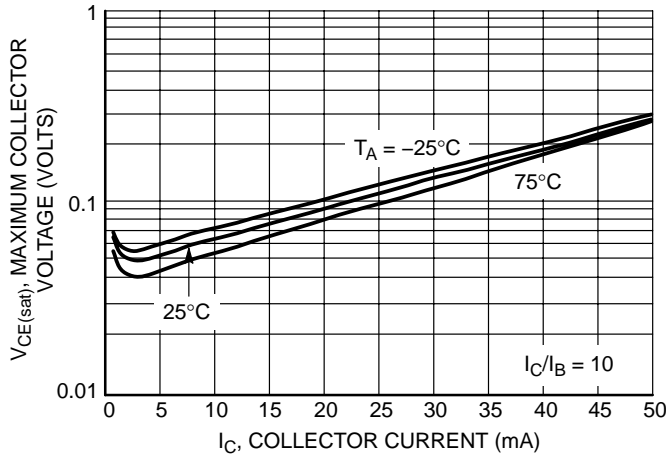


Figure 29. Maximum Collector Voltage versus Collector Current

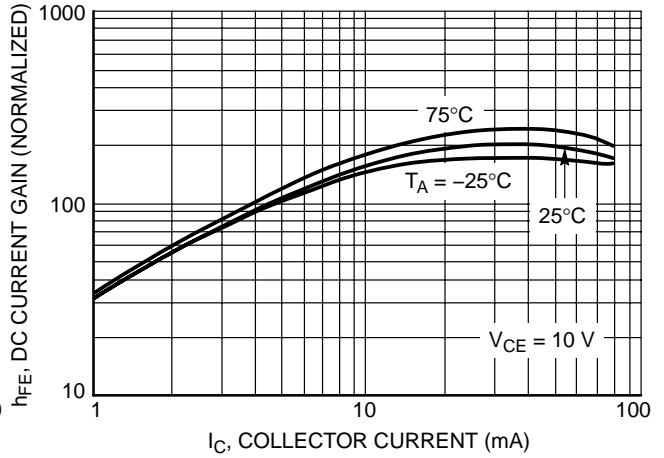


Figure 30. DC Current Gain

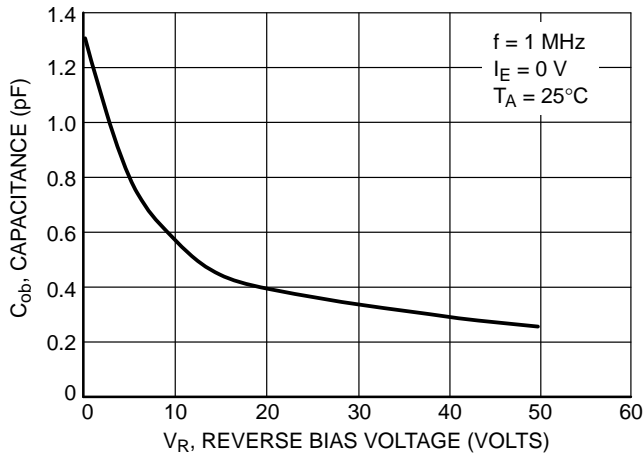


Figure 31. Output Capacitance

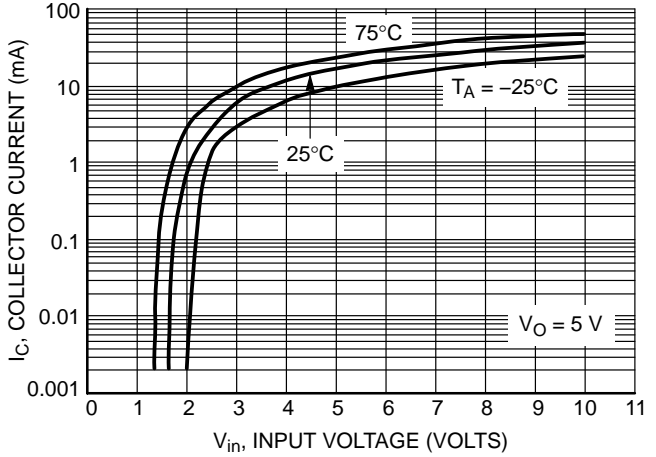


Figure 32. Output Current versus Input Voltage

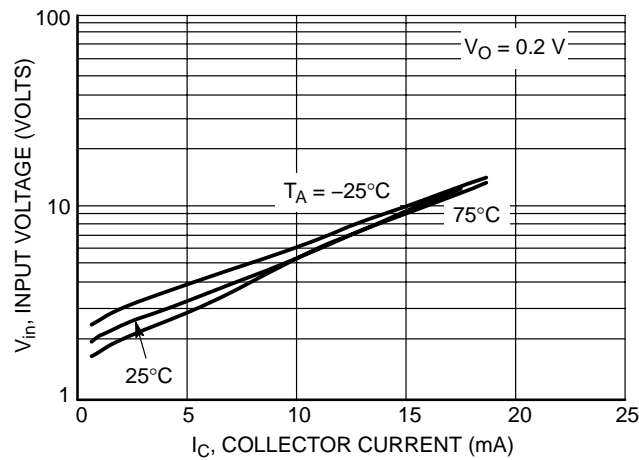
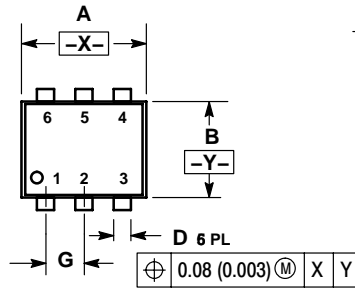


Figure 33. Input Voltage versus Output Current

NSBA114EDXV6T1, NSBA114EDXV6T5

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:

- PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:

- PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

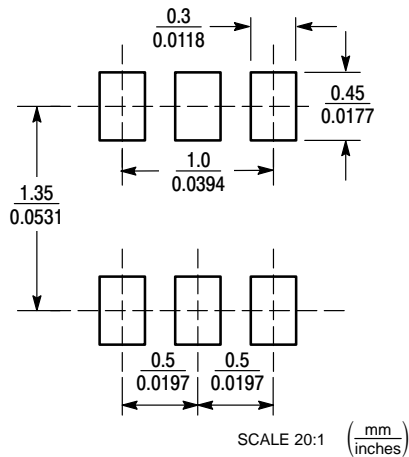
STYLE 3:

- PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1


STYLE 4:

- PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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