

## 阅读申明

- 1.本站收集的数据手册和产品资料都来自互联网，版权归原作者所有。如读者和版权方有任何异议请及时告之，我们将妥善解决。
- 2.本站提供的中文数据手册是英文数据手册的中文翻译，其目的是协助用户阅读，该译文无法自动跟随原稿更新，同时也可能存在翻译上的不当。建议读者以英文原稿为参考以便获得更精准的信息。
- 3.本站提供的产品资料，来自厂商的技术支持或者使用者的心得体会等，其内容可能存在描述上的差异，建议读者做出适当判断。
- 4.如需与我们联系，请发邮件到marketing@iczoom.com，主题请标有“数据手册”字样。

## Read Statement

1. The datasheets and other product information on the site are all from network reference or other public materials, and the copyright belongs to the original author and original published source. If readers and copyright owners have any objections, please contact us and we will deal with it in a timely manner.
2. The Chinese datasheets provided on the website is a Chinese translation of the English datasheets. Its purpose is for reader's learning exchange only and do not involve commercial purposes. The translation cannot be automatically updated with the original manuscript, and there may also be improper translations. Readers are advised to use the English manuscript as a reference for more accurate information.
3. All product information provided on the website refer to solutions from manufacturers' technical support or users the contents may have differences in description, and readers are advised to take the original article as the standard.
4. If you have any questions, please contact us at marketing@iczoom.com and mark the subject with "Datasheets" .

# NSB1706DMW5T1

## Dual Bias Resistor Transistor

### NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSB1706DMW5T1, two BRT devices are housed in the SC-88A package which is ideal for low power surface mount applications where board space is at a premium.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Pb-Free Package is Available

#### MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for  $Q_1$  and  $Q_2$ )

| Rating                    | Symbol    | Value | Unit |
|---------------------------|-----------|-------|------|
| Collector-Base Voltage    | $V_{CBO}$ | 50    | Vdc  |
| Collector-Emitter Voltage | $V_{CEO}$ | 50    | Vdc  |
| Collector Current         | $I_C$     | 100   | mAdc |

#### THERMAL CHARACTERISTICS

| Characteristic (One Junction Heated)  | Symbol          | Max  | Unit                       |
|---|-----------------|--|----------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$           | 187 (Note 1)<br>256 (Note 2)<br>1.5 (Note 1)<br>2.0 (Note 2) | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient   | $R_{\theta JA}$ | 670 (Note 1)<br>490 (Note 2)                                 | $^\circ\text{C}/\text{W}$  |
| Characteristic (Both Junctions Heated)  | Symbol          | Max  | Unit                       |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$           | 250 (Note 1)<br>385 (Note 2)<br>2.0 (Note 1)<br>3.0 (Note 2) | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Ambient   | $R_{\theta JA}$ | 493 (Note 1)<br>325 (Note 2)                                 | $^\circ\text{C}/\text{W}$  |
| Thermal Resistance, Junction-to-Lead  | $R_{\theta JL}$ | 188 (Note 1)<br>208 (Note 2)                                 | $^\circ\text{C}/\text{W}$  |
| Junction and Storage Temperature  | $T_J, T_{stg}$  | -55 to +150  | $^\circ\text{C}$           |

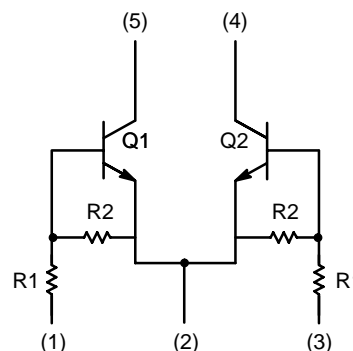
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 inch Pad.



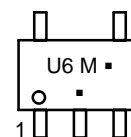
ON Semiconductor®

<http://onsemi.com>



SC-88A  
CASE 419A  
STYLE 1

#### MARKING DIAGRAM



U6 = Device Marking  
M = Date Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

| Device         | Package          | Shipping†        |
|----------------|------------------|------------------|
| NSB1706DMW5T1  | SC-88A           | 3000/Tape & Reel |
| NSB1706DMW5T1G | SC-88A (Pb-Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSB1706DMW5T1

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted, common for Q<sub>1</sub> and Q<sub>2</sub>)

| Characteristic  | Symbol               | Min | Typ | Max  | Unit |
|---|----------------------|-----|-----|------|------|
| <b>OFF CHARACTERISTICS</b>  |                      |     |     |      |      |
| Collector-Base Cutoff Current<br>(V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)                 | I <sub>CBO</sub>     | –   | –   | 100  | nAdc |
| Collector-Emitter Cutoff Current<br>(V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)              | I <sub>CEO</sub>     | –   | –   | 500  | nAdc |
| Emitter-Base Cutoff Current<br>(V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)                  | I <sub>EBO</sub>     | –   | –   | 0.18 | mAdc |
| Collector-Base Breakdown Voltage<br>(I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)              | V <sub>(BR)CBO</sub> | 50  | –   | –    | Vdc  |
| Collector-Emitter Breakdown Voltage (Note 3)<br>(I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0) | V <sub>(BR)CEO</sub> | 50  | –   | –    | Vdc  |

## ON CHARACTERISTICS (Note 3)

|   |                      |       |     |       |     |
|---|----------------------|-------|-----|-------|-----|
| DC Current Gain<br>(V <sub>CE</sub> = 10 V, I <sub>C</sub> = 5.0 mA)                                | h <sub>FE</sub>      | 80    | 200 | –     |     |
| Collector-Emitter Saturation Voltage<br>(I <sub>C</sub> = 10 mA, I <sub>B</sub> = 1 mA)             | V <sub>CE(sat)</sub> | –     | –   | 0.25  | Vdc |
| Output Voltage (on)<br>(V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 2.5 V, R <sub>L</sub> = 1.0 kΩ)   | V <sub>OL</sub>      | –     | –   | 0.2   | Vdc |
| Output Voltage (off)<br>(V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.25 V, R <sub>L</sub> = 1.0 kΩ) | V <sub>OH</sub>      | 4.9   | –   | –     | Vdc |
| Input Resistor  | R1                   | 3.3   | 4.7 | 6.1   | kΩ  |
| Resistor Ratio  | R1/R2                | 0.055 | 0.1 | 0.185 |     |

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

NOTE: New resistor combinations. Updated curves to follow in subsequent data sheets.

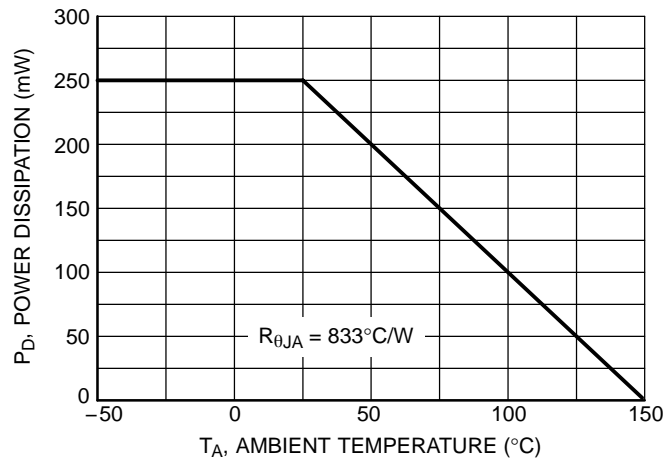
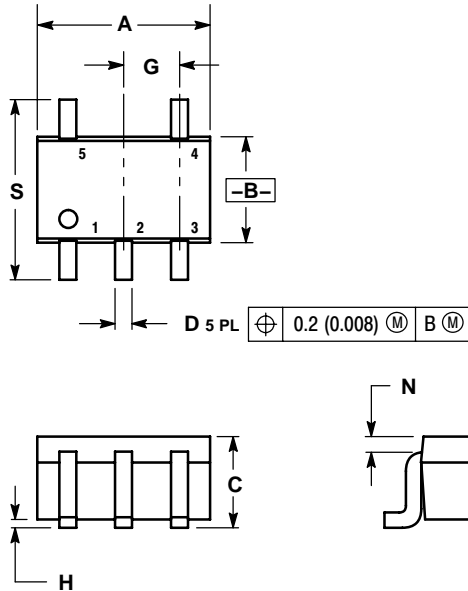


Figure 1. Derating Curve

# NSB1706DMW5T1

## PACKAGE DIMENSIONS

SC-88A, SOT-353, SC-70  
CASE 419A-02  
ISSUE J



**NOTES:**

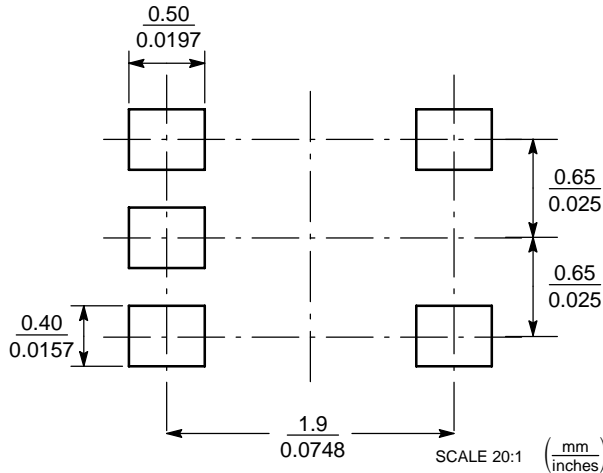
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES    |       | MILLIMETERS |      |
|-----|-----------|-------|-------------|------|
|     | MIN       | MAX   | MIN         | MAX  |
| A   | 0.071     | 0.087 | 1.80        | 2.20 |
| B   | 0.045     | 0.053 | 1.15        | 1.35 |
| C   | 0.031     | 0.043 | 0.80        | 1.10 |
| D   | 0.004     | 0.012 | 0.10        | 0.30 |
| G   | 0.026 BSC |       | 0.65 BSC    |      |
| H   | ---       | 0.004 | ---         | 0.10 |
| J   | 0.004     | 0.010 | 0.10        | 0.25 |
| K   | 0.004     | 0.012 | 0.10        | 0.30 |
| N   | 0.008 REF |       | 0.20 REF    |      |
| S   | 0.079     | 0.087 | 2.00        | 2.20 |

**STYLE 1:**

- PIN 1. BASE
- EMITTER
- BASE
- COLLECTOR
- COLLECTOR

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative