

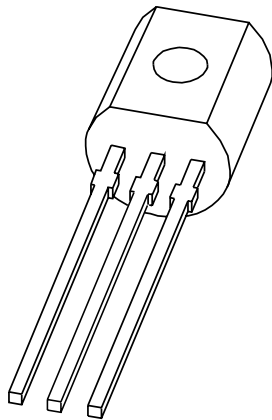
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# DATA SHEET



## **PN2907A** PNP switching transistor

Product data sheet  
Supersedes data of 1997 May 05

2004 Oct 11

# PNP switching transistor

# PN2907A

### FEATURES

- High current (max. 600 mA)
- Low voltage (max. 60 V).

### APPLICATIONS

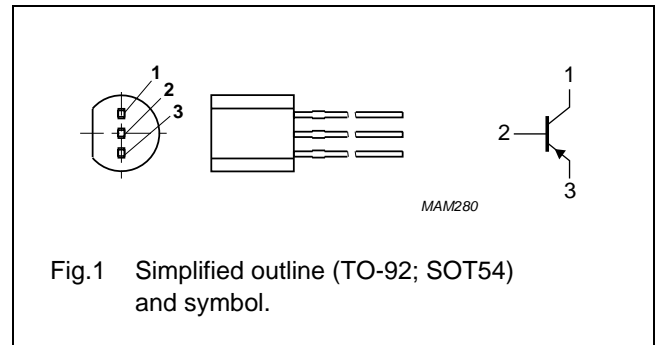
- Switching and linear amplification.

### DESCRIPTION

PNP switching transistor in a TO-92; SOT54 plastic package. NPN complement: PN2222A.

### PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–60	V
$V_{CEO}$	collector-emitter voltage	open base	–	–60	V
$I_C$	collector current (DC)		–	–600	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	500	mW
$h_{FE}$	DC current gain	$V_{CE} = -10\text{ V}; I_C = -150\text{ mA}$	100	300	
$f_T$	transition frequency	$V_{CE} = -20\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz}$	200	–	MHz
$t_{off}$	turn-off time	$I_{Con} = -150\text{ mA}; I_{Bon} = -15\text{ mA}; I_{Boff} = 15\text{ mA}$	–	365	ns

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PN2907A	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## PNP switching transistor

PN2907A

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–60	V
$V_{CEO}$	collector-emitter voltage	open base	–	–60	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–600	mA
$I_{CM}$	peak collector current		–	–800	mA
$I_{BM}$	peak base current		–	–200	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	500	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	ambient temperature		–65	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	250	K/W

**Note**

1. Transistor mounted on an FR4 printed-circuit board.

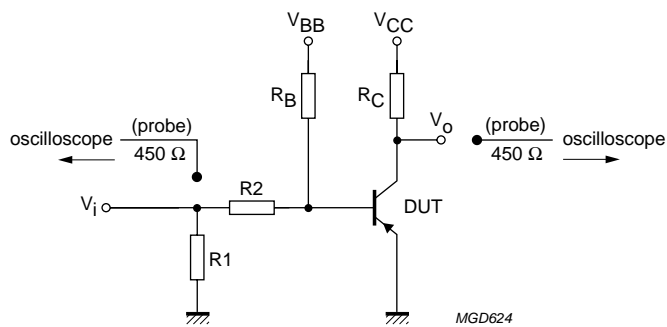
**CHARACTERISTICS** $T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0\text{ A}$	–	–10	nA
		$V_{CB} = -50\text{ V}; I_E = 0\text{ A}; T_j = 125\text{ °C}$	–	–10	μA
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	–	–50	nA
$h_{FE}$	DC current gain	$V_{CE} = -10\text{ V}; I_C = -0.1\text{ mA}$	75	–	
		$V_{CE} = -10\text{ V}; I_C = -1\text{ mA}$	100	–	
		$V_{CE} = -10\text{ V}; I_C = -10\text{ mA}$	100	–	
		$V_{CE} = -10\text{ V}; I_C = -150\text{ mA}$	100	300	
		$V_{CE} = -10\text{ V}; I_C = -500\text{ mA}$	50	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -150\text{ mA}; I_B = -15\text{ mA}$	–	–400	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–1.6	V
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -150\text{ mA}; I_B = -15\text{ mA}$	–	–1.3	V
		$I_C = -150\text{ mA}; I_B = -50\text{ mA}$	–	–2.6	V
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_C = 0\text{ A}; f = 1\text{ MHz}$	–	8	pF
$C_e$	emitter capacitance	$V_{EB} = -2\text{ V}; I_C = I_E = 0\text{ A}; f = 1\text{ MHz}$	–	30	pF
$f_T$	transition frequency	$V_{CE} = -20\text{ V}; I_C = -50\text{ mA}; f = 100\text{ MHz}$	200	–	MHz

PNP switching transistor

PN2907A

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Switching times (between 10 % and 90 % levels); see Fig.2</b>					
$t_{on}$	turn-on time	$I_{Con} = -150 \text{ mA}; I_{Bon} = -15 \text{ mA};$ $I_{Boff} = 15 \text{ mA}$	–	40	ns
$t_d$	delay time		–	12	ns
$t_r$	rise time		–	30	ns
$t_{off}$	turn-off time		–	365	ns
$t_s$	storage time		–	300	ns
$t_f$	fall time		–	65	ns



$V_i = -9.5 \text{ V}; T = 500 \text{ } \mu\text{s}; t_p = 10 \text{ } \mu\text{s}; t_r = t_f \leq 3 \text{ ns}.$   
 $R_1 = 68 \text{ } \Omega; R_2 = 325 \text{ } \Omega; R_B = 325 \text{ } \Omega; R_C = 160 \text{ } \Omega.$   
 $V_{BB} = 3.5 \text{ V}; V_{CC} = -29.5 \text{ V}.$   
 Oscilloscope: input impedance  $Z_i = 50 \text{ } \Omega.$

Fig.2 Test circuit for switching times.

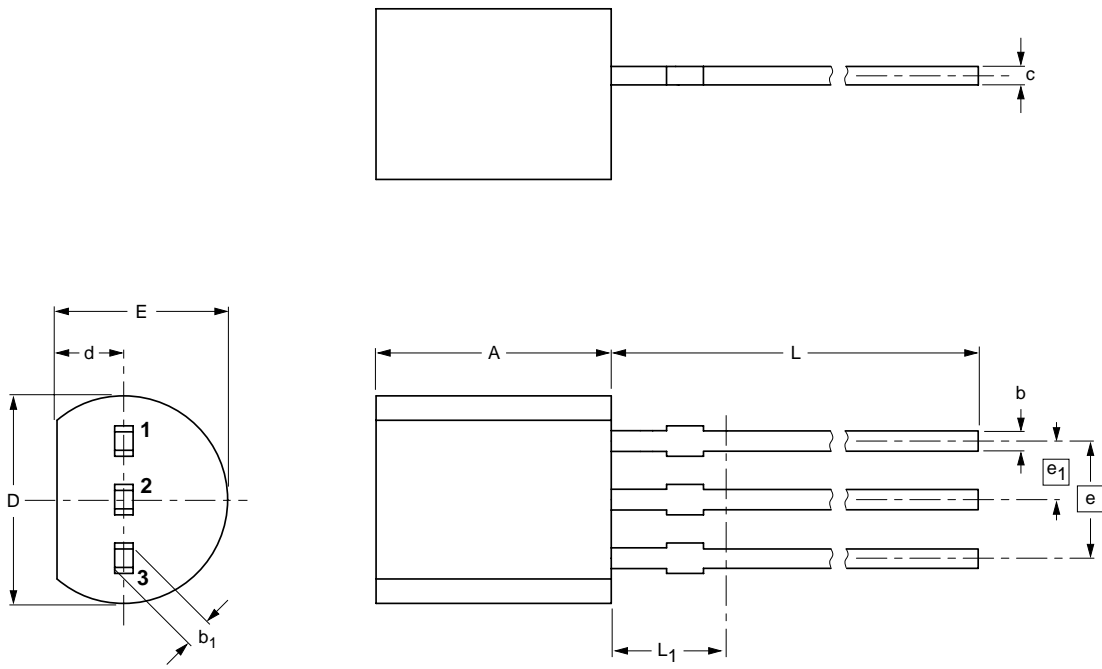
PNP switching transistor

PN2907A

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT54		TO-92	SC-43A		04-06-28 04-11-16

PNP switching transistor

PN2907A

**DATA SHEET STATUS**

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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