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MMUN2111LT1 Series

Preferred Devices

Bias Resistor Transistors

PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-23 package which is designed for low power surface mount applications.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SOT-23 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- Available in 8 mm embossed tape and reel.
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D	246 (Note 1) 400 (Note 2) 2.0 (Note 1) 3.2 (Note 2)	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	508 (Note 1) 311 (Note 2)	°C/W
Thermal Resistance, Junction-to-Lead	$R_{\theta JL}$	174 (Note 1) 208 (Note 2)	°C/W
Junction and Storage, Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 x 1.0 inch Pad

ON Semiconductor®

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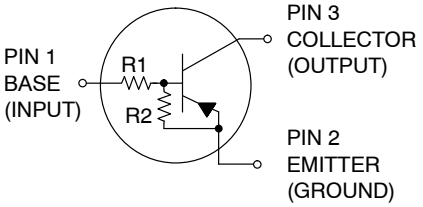


MARKING DIAGRAM

A6x = Device Code
x = A − L (Refer to page 2)
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMUN21xxLT1	SOT−23	3000/Tape & Reel
MMUN21xxLT1G	SOT−23 (Pb−Free)	3000/Tape & Reel
MMUN21xxLT3	SOT−23	10000/Tape & Reel
MMUN21xxLT3G	SOT−23 (Pb−Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

DEVICE MARKING AND RESISTOR VALUES

Device*	Package	Marking	R1 (K)	R2 (K)	Shipping
MMUN2111LT1, G MMUN2111LT3, G	SOT−23	A6A	10	10	3000/Tape & Reel 10,000/Tape & Reel
MMUN2112LT1, G	SOT−23	A6B	22	22	3000/Tape & Reel
MMUN2113LT1, G MMUN2113LT3, G	SOT−23	A6C	47	47	3000/Tape & Reel 10,000/Tape & Reel
MMUN2114LT1, G MMUN2114LT3G	SOT−23	A6D	10	47	3000/Tape & Reel 10,000/Tape & Reel
MMUN2115LT1, G	SOT−23	A6E	10	∞	3000/Tape & Reel
MMUN2116LT1, G	SOT−23	A6F	4.7	∞	3000/Tape & Reel
MMUN2130LT1, G (Note 3)	SOT−23	A6G	1.0	1.0	3000/Tape & Reel
MMUN2131LT1, G (Note 3)	SOT−23	A6H	2.2	2.2	3000/Tape & Reel
MMUN2132LT1, G	SOT−23	A6J	4.7	4.7	3000/Tape & Reel
MMUN2133LT1, G	SOT−23	A6K	4.7	47	3000/Tape & Reel
MMUN2134LT1, G (Note 3)	SOT−23	A6L	22	47	3000/Tape & Reel

*The “G” suffix indicates Pb−Free package available.

3. New devices. Updated curves to follow in subsequent data sheets.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	MMUN2111LT1, G	I_{EBO}	–	–	0.5	mAdc
	MMUN2112LT1, G		–	–	0.2	
	MMUN2113LT1, G		–	–	0.1	
	MMUN2114LT1, G		–	–	0.2	
	MMUN2115LT1, G		–	–	0.9	
	MMUN2116LT1, G		–	–	1.9	
	MMUN2130LT1, G		–	–	4.3	
	MMUN2131LT1, G		–	–	2.3	
	MMUN2132LT1, G		–	–	1.5	
	MMUN2133LT1, G		–	–	0.18	
	MMUN2134LT1, G		–	–	0.13	
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 4) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	–	–	Vdc

4. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5)						
DC Current Gain	MMUN2111LT1, G	h_{FE}	35	60	–	
(V_{CE} = 10 V, I_C = 5.0 mA)	MMUN2112LT1, G		60	100	–	
	MMUN2113LT1, G		80	140	–	
	MMUN2114LT1, G		80	140	–	
	MMUN2115LT1, G		160	250	–	
	MMUN2116LT1, G		160	250	–	
	MMUN2130LT1, G		3.0	5.0	–	
	MMUN2131LT1, G		8.0	15	–	
	MMUN2132LT1, G		15	27	–	
	MMUN2133LT1, G		80	140	–	
	MMUN2134LT1, G		80	130	–	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				Vdc
(I_C = 10 mA, I_B = 0.3 mA)	MMUN2111LT1, G		–	–	0.25	
	MMUN2112LT1, G		–	–	0.25	
	MMUN2113LT1, G		–	–	0.25	
	MMUN2114LT1, G		–	–	0.25	
	MMUN2133LT1, G		–	–	0.25	
(I_C = 10 mA, I_B = 5 mA)	MMUN2130LT1, G		–	–	0.25	
	MMUN2131LT1, G		–	–	0.25	
(I_C = 10 mA, I_B = 1 mA)	MMUN2115LT1, G		–	–	0.25	
	MMUN2116LT1, G		–	–	0.25	
	MMUN2132LT1, G		–	–	0.25	
	MMUN2134LT1, G		–	–	0.25	
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	MMUN2111LT1, G		–	–	0.2	
	MMUN2112LT1, G		–	–	0.2	
	MMUN2114LT1, G		–	–	0.2	
	MMUN2115LT1, G		–	–	0.2	
	MMUN2116LT1, G		–	–	0.2	
	MMUN2130LT1, G		–	–	0.2	
	MMUN2131LT1, G		–	–	0.2	
	MMUN2132LT1, G		–	–	0.2	
	MMUN2133LT1, G		–	–	0.2	
	MMUN2134LT1, G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	MMUN2113LT1, G		–	–	0.2	
Output Voltage (off)		V_{OH}				Vdc
(V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	MMUN2111LT1, G		4.9	–	–	
	MMUN2112LT1, G		4.9	–	–	
	MMUN2113LT1, G		4.9	–	–	
	MMUN2114LT1, G		4.9	–	–	
	MMUN2133LT1, G		4.9	–	–	
	MMUN2134LT1, G		4.9	–	–	
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	MMUN2115LT1, G		4.9	–	–	
	MMUN2116LT1, G		4.9	–	–	
	MMUN2131LT1, G		4.9	–	–	
	MMUN2132LT1, G		4.9	–	–	
(V_{CC} = 5.0 V, V_B = 0.050 V, R_L = 1.0 kΩ)	MMUN2130LT1, G		4.9	–	–	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 5)						
Input Resistor	MMUN2111LT1, G	R1	7.0	10	13	k Ω
	MMUN2112LT1, G		15.4	22	28.6	
	MMUN2113LT1, G		32.9	47	61.1	
	MMUN2114LT1, G		7.0	10	13	
	MMUN2115LT1, G		7.0	10	13	
	MMUN2116LT1, G		3.3	4.7	6.1	
	MMUN2130LT1, G		0.7	1.0	1.3	
	MMUN2131LT1, G		1.5	2.2	2.9	
	MMUN2132LT1, G		3.3	4.7	6.1	
	MMUN2133LT1, G		3.3	4.7	6.1	
	MMUN2134LT1, G		15.4	22	28.6	
Resistor Ratio	MMUN2111LT1, G	R_1/R_2	0.8	1.0	1.2	
	MMUN2112LT1, G		0.8	1.0	1.2	
	MMUN2113LT1, G		0.8	1.0	1.2	
	MMUN2114LT1, G		0.17	0.21	0.25	
	MMUN2115LT1, G		–	–	–	
	MMUN2116LT1, G		–	–	–	
	MMUN2130LT1, G		0.8	1.0	1.2	
	MMUN2131LT1, G		0.8	1.0	1.2	
	MMUN2132LT1, G		0.8	1.0	1.2	
	MMUN2133LT1, G		0.055	0.1	0.185	
	MMUN2134LT1, G		0.38	0.47	0.56	

5. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2111LT1

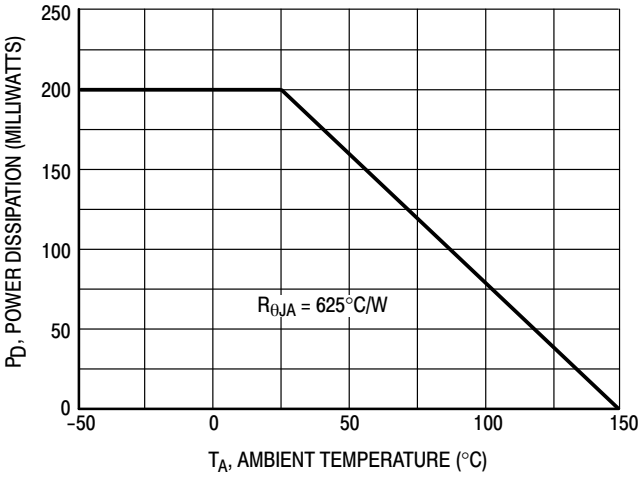


Figure 1. Derating Curve

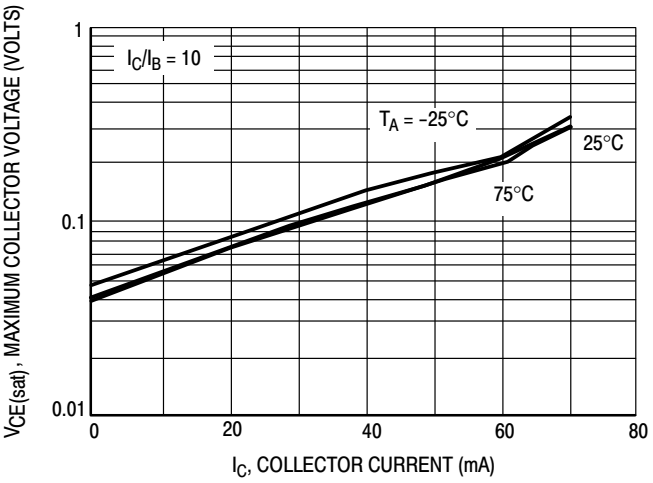


Figure 2. $V_{CE(sat)}$ versus I_C

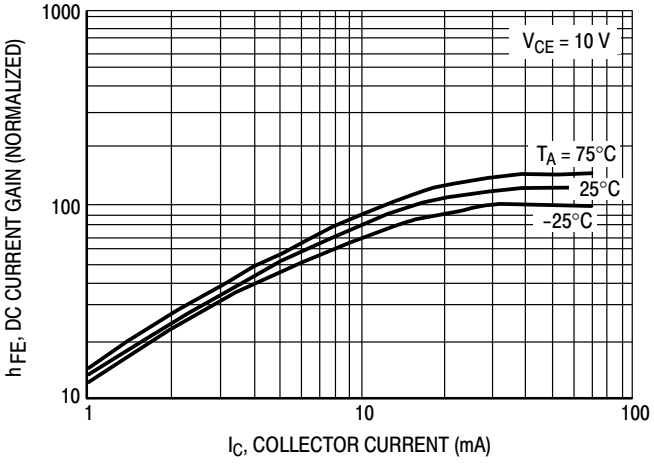


Figure 3. DC Current Gain

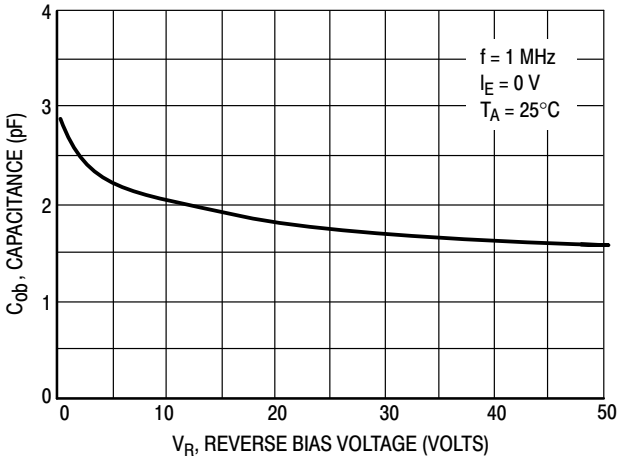


Figure 4. Output Capacitance

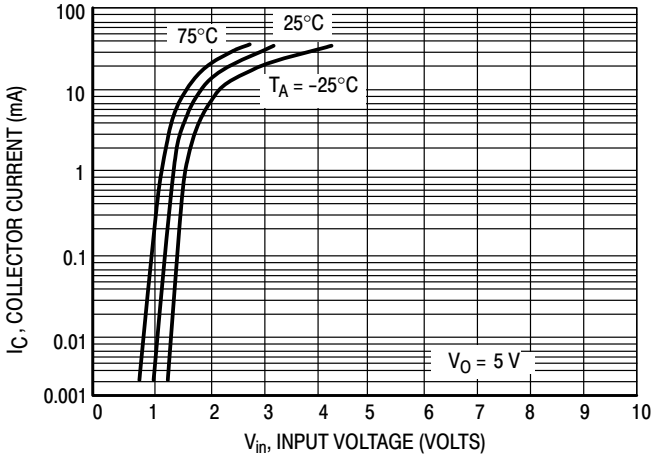


Figure 5. Output Current versus Input Voltage

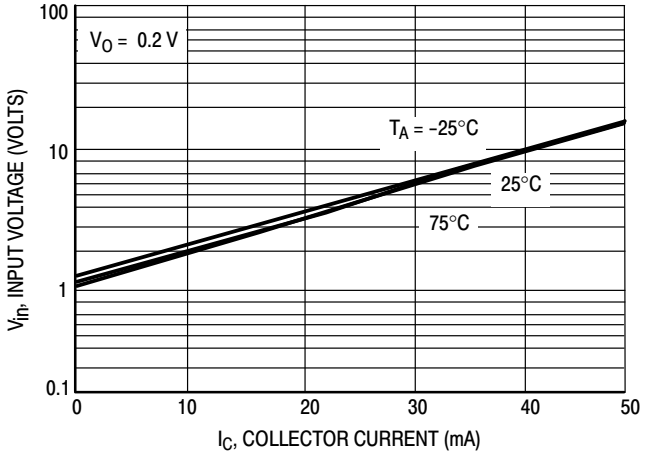


Figure 6. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2112LT1

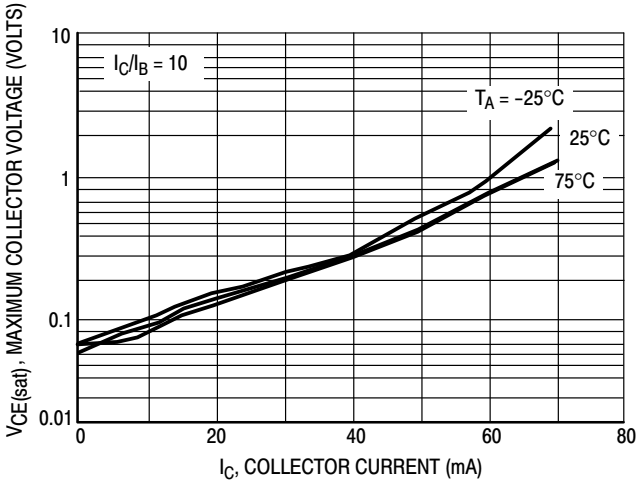


Figure 7. $V_{CE(sat)}$ versus I_C

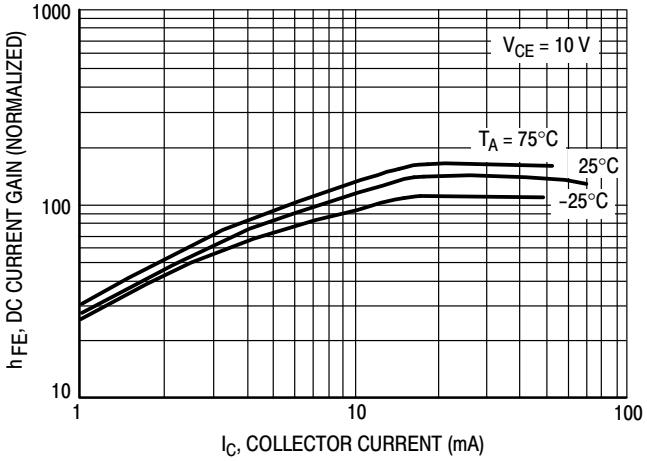


Figure 8. DC Current Gain

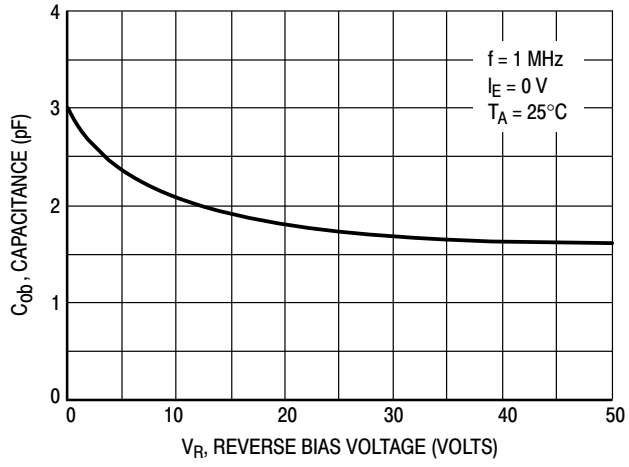


Figure 9. Output Capacitance

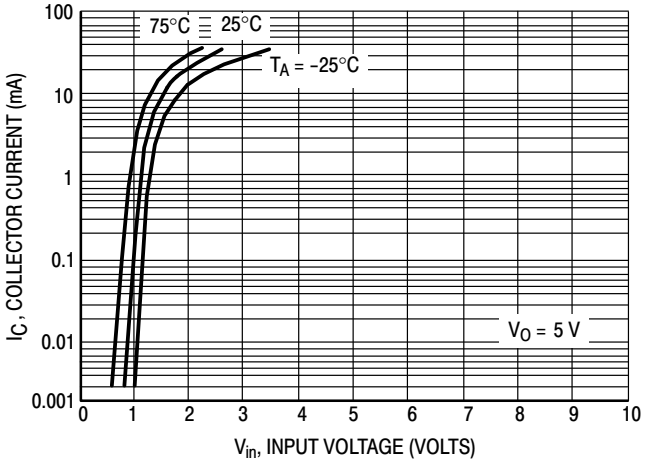


Figure 10. Output Current versus Input Voltage

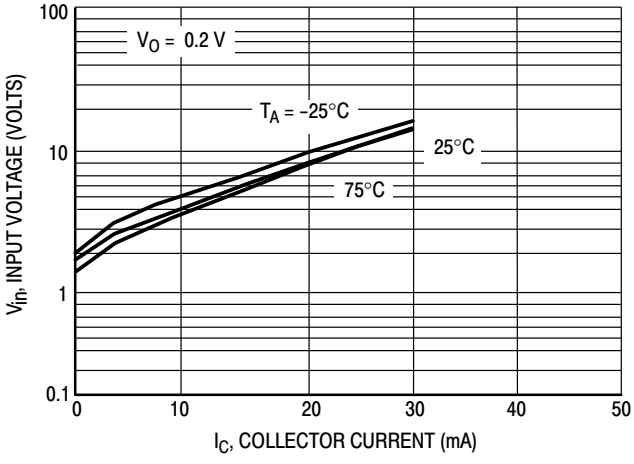


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2113LT1

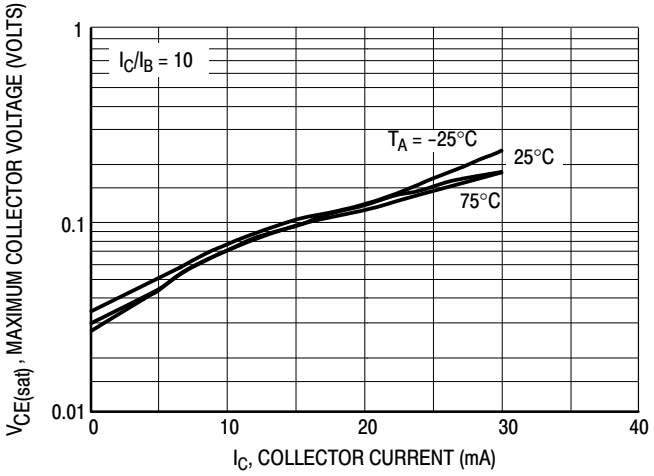


Figure 12. $V_{CE(sat)}$ versus I_C

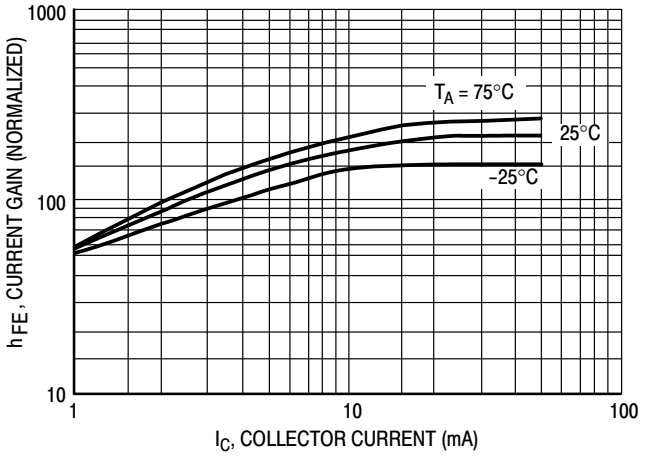


Figure 13. DC Current Gain

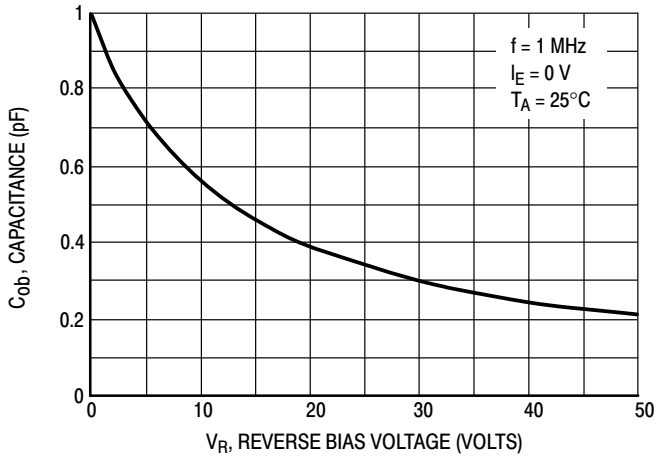


Figure 14. Output Capacitance

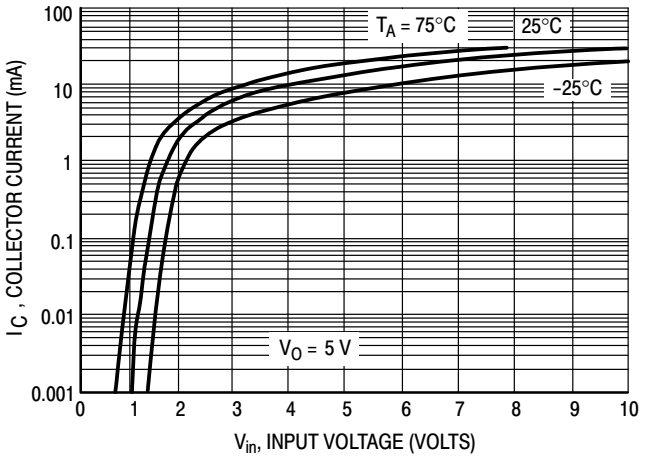


Figure 15. Output Current versus Input Voltage

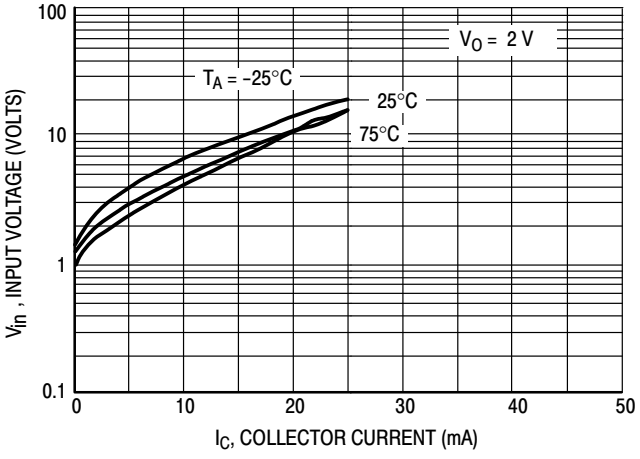


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2114LT1

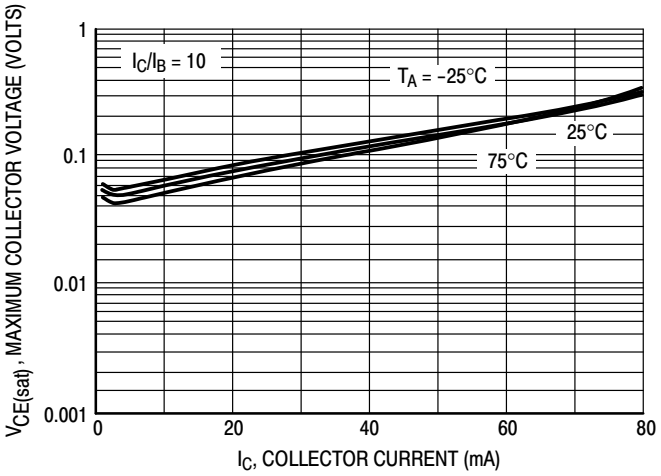


Figure 17. $V_{CE(sat)}$ versus I_C

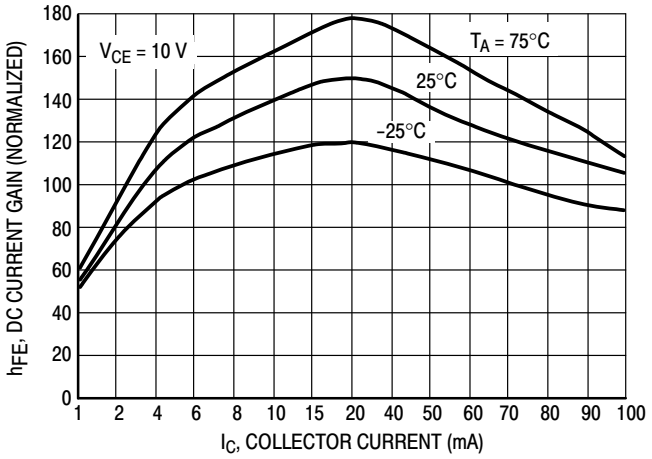


Figure 18. DC Current Gain

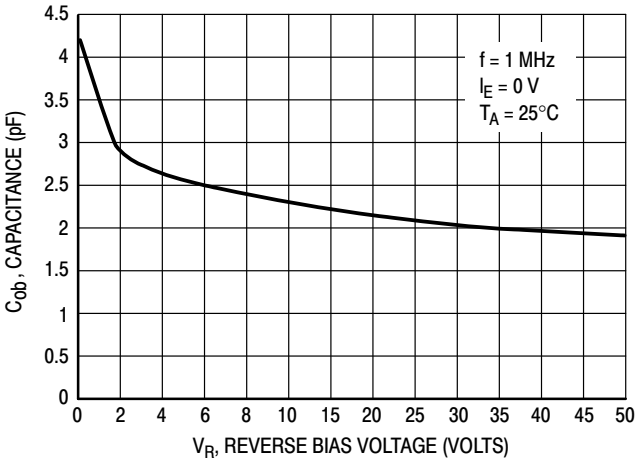


Figure 19. Output Capacitance

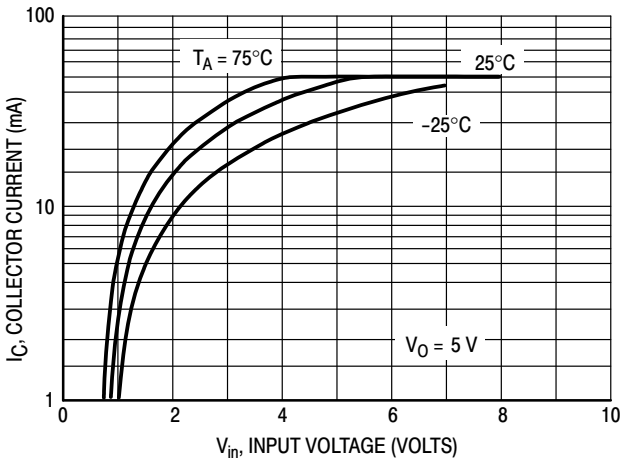


Figure 20. Output Current versus Input Voltage

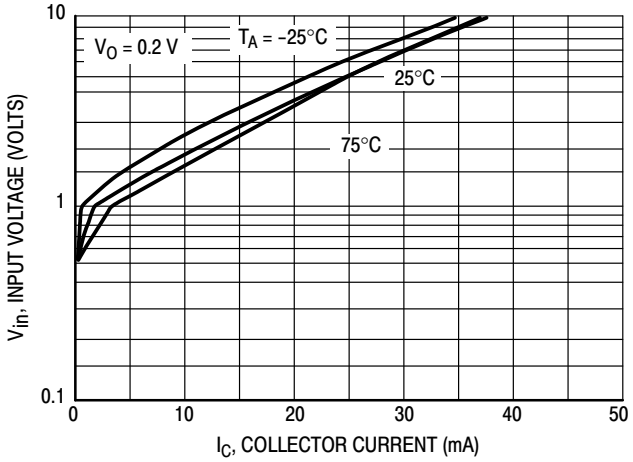


Figure 21. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2115LT1

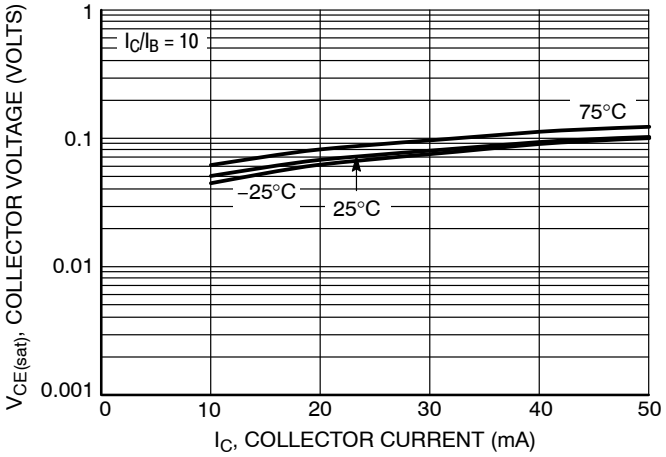


Figure 22. $V_{CE(sat)}$ versus I_C

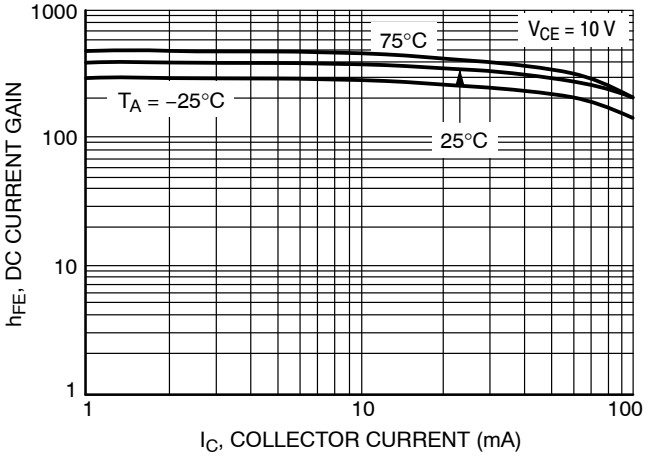


Figure 23. DC Current Gain

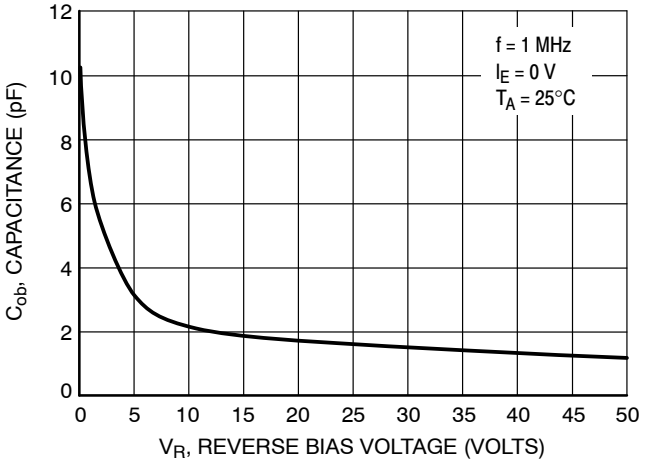


Figure 24. Output Capacitance

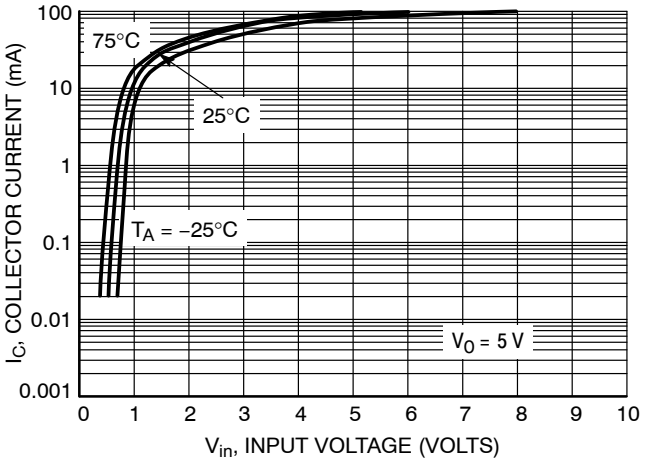


Figure 25. Output Current versus Input Voltage

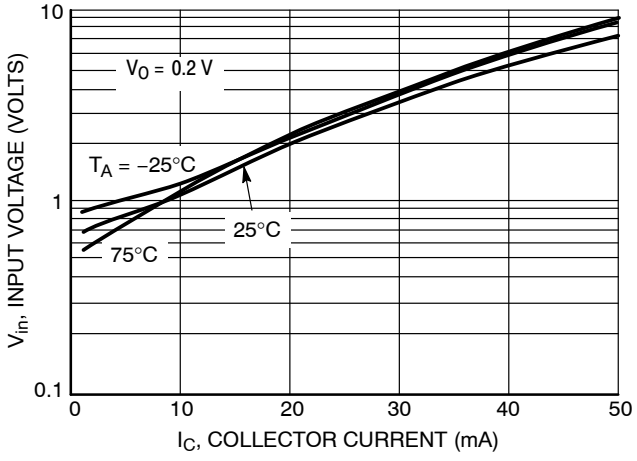


Figure 26. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2116LT1

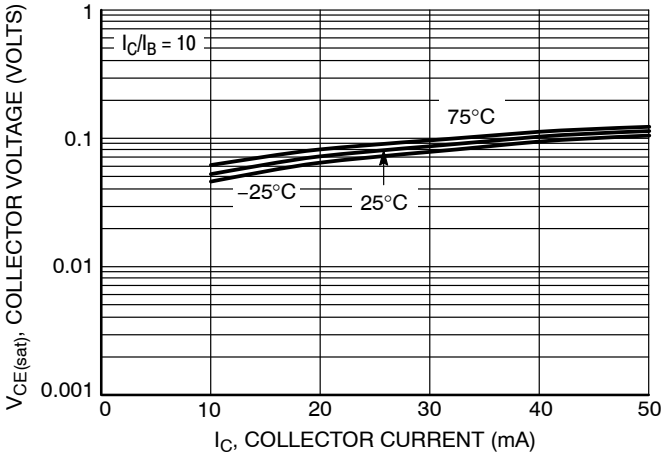


Figure 27. $V_{CE(sat)}$ versus I_C

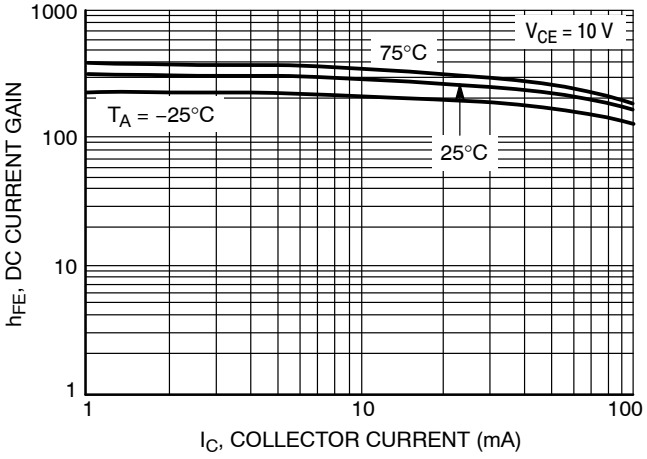


Figure 28. DC Current Gain

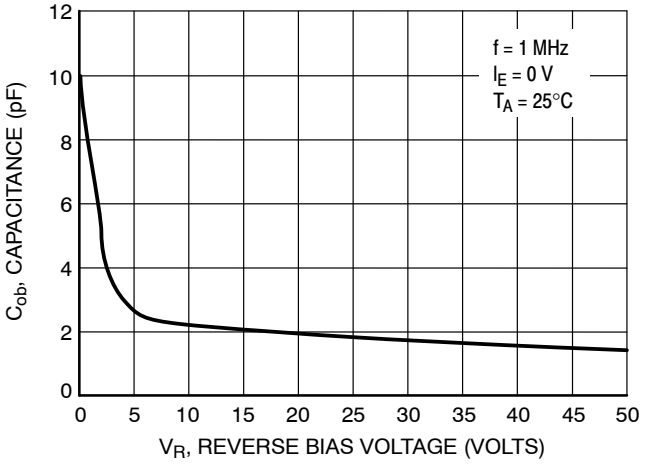


Figure 29. Output Capacitance

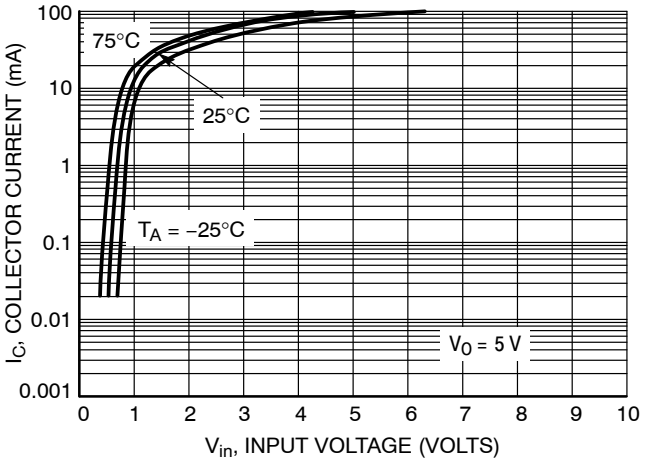


Figure 30. Output Current versus Input Voltage

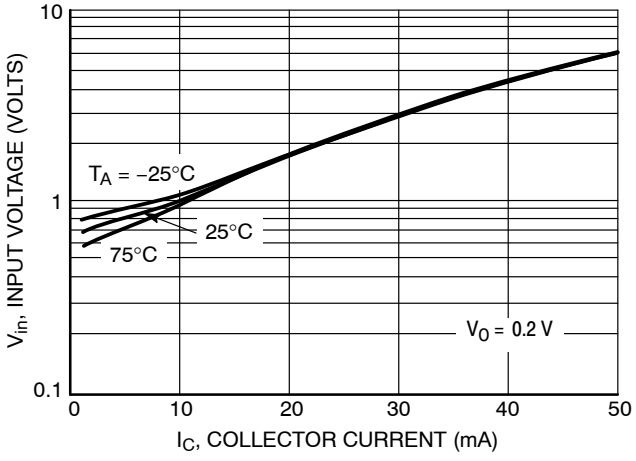


Figure 31. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2132LT1

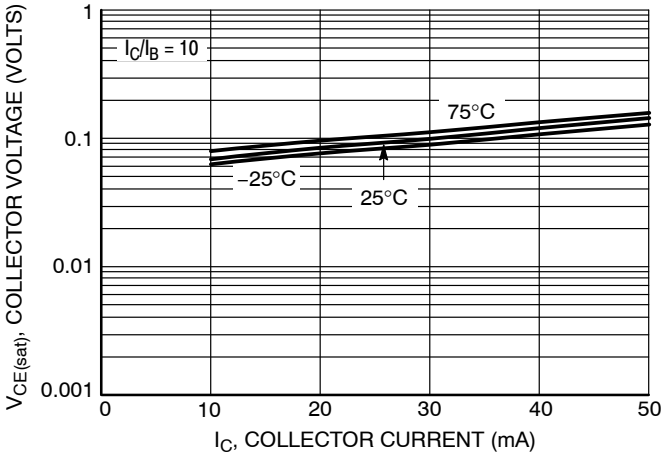


Figure 32. $V_{CE(sat)}$ versus I_C

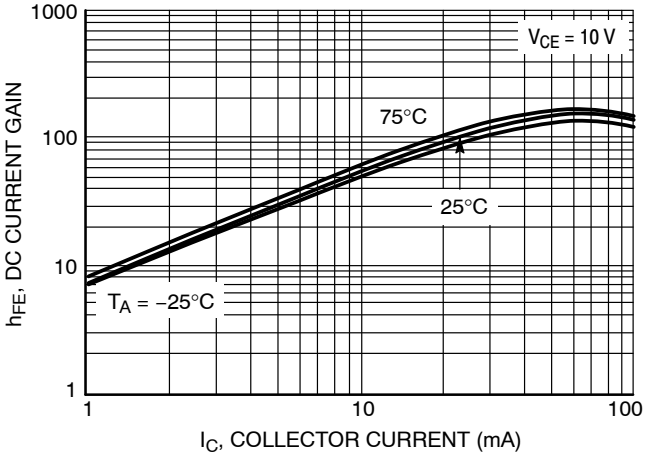


Figure 33. DC Current Gain

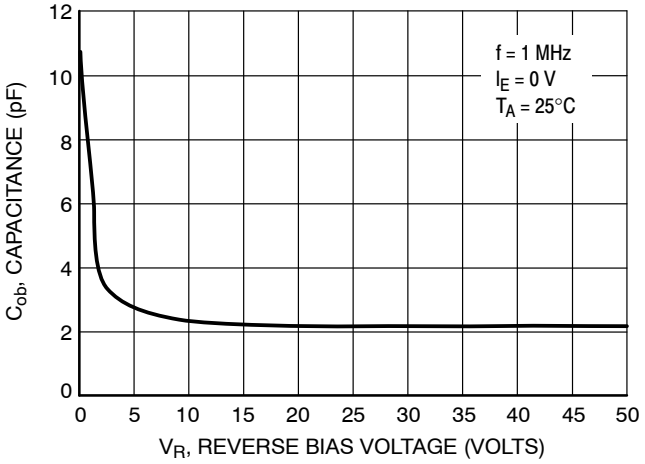


Figure 34. Output Capacitance

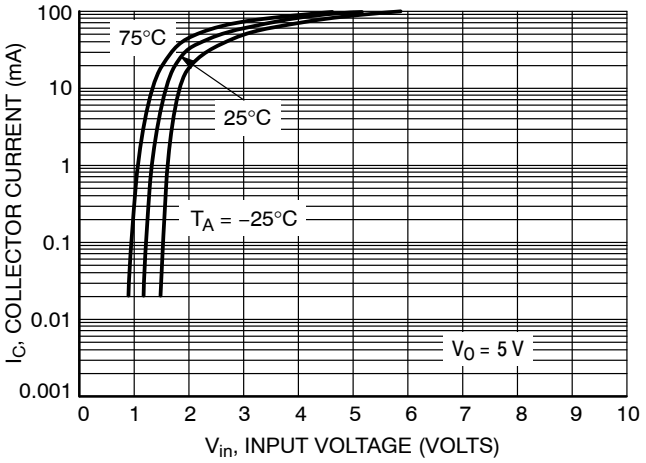


Figure 35. Output Current versus Input Voltage

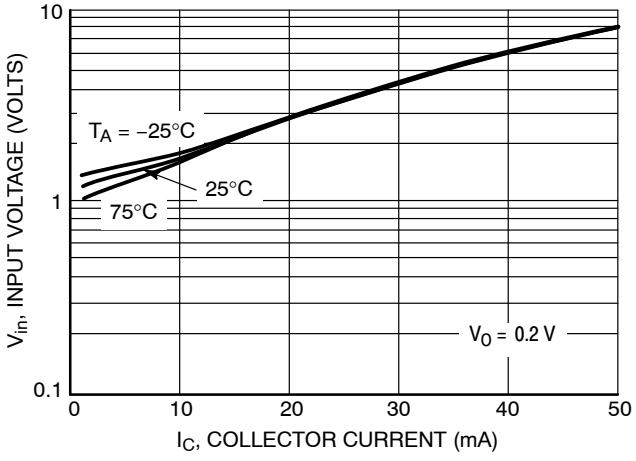


Figure 36. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS
MMUN2133LT1

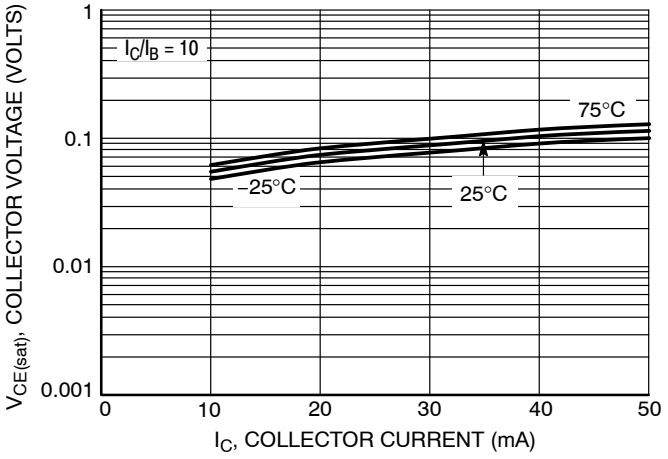


Figure 37. $V_{CE(sat)}$ versus I_C

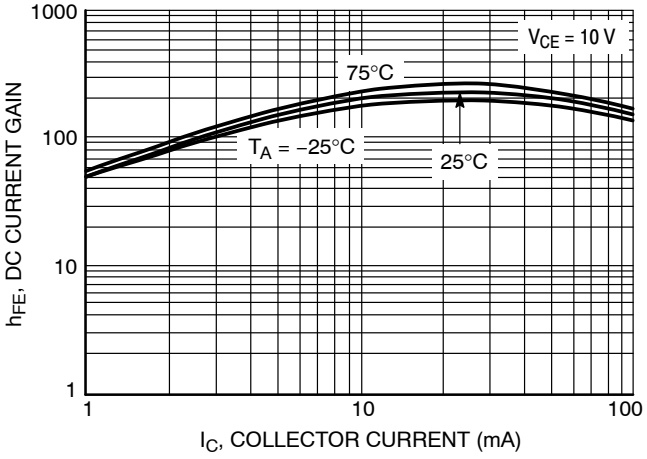


Figure 38. DC Current Gain

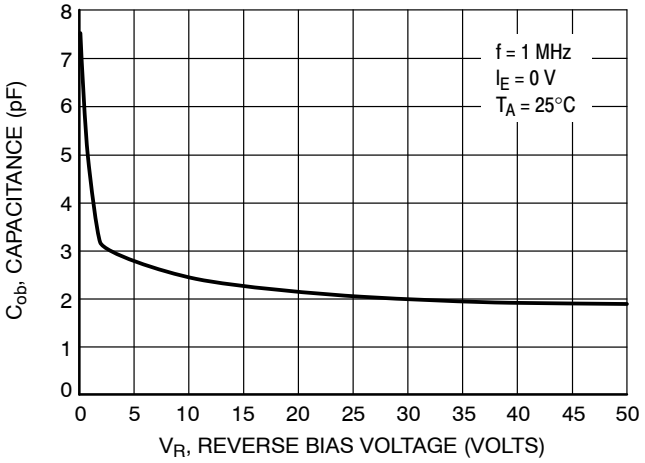


Figure 39. Output Capacitance

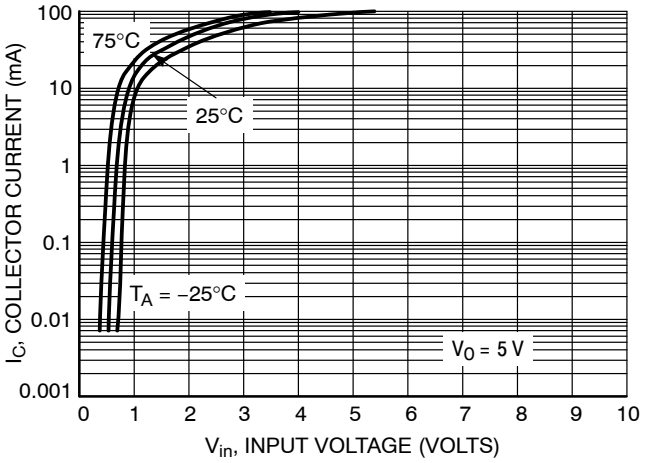


Figure 40. Output Current versus Input Voltage

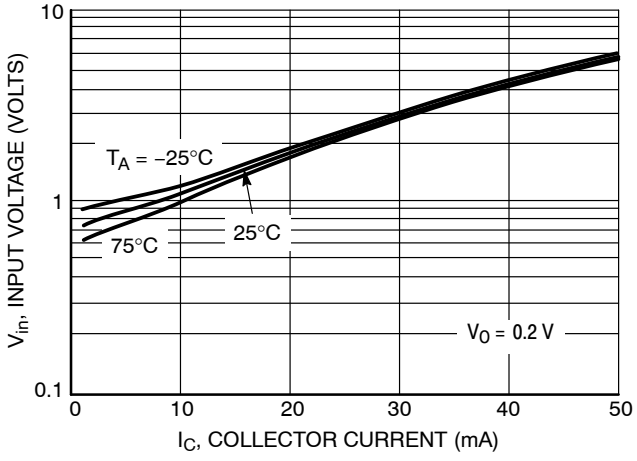


Figure 41. Input Voltage versus Output Current

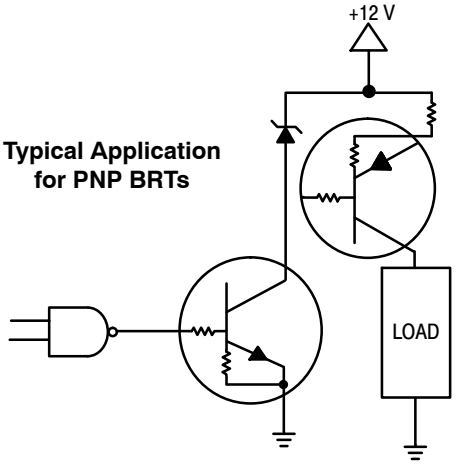
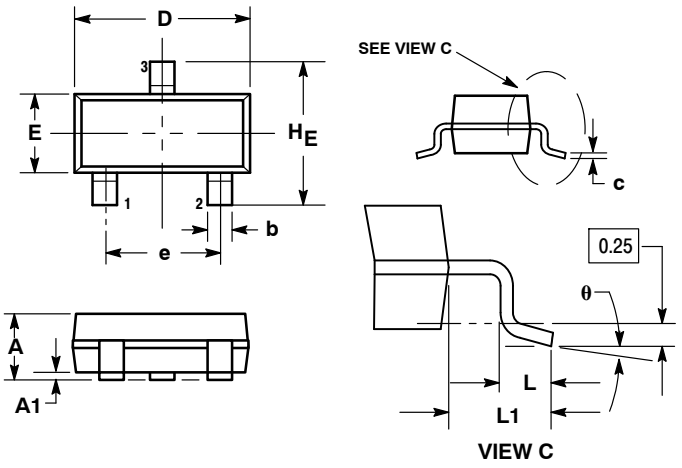


Figure 42. Inexpensive, Unregulated Current Source

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN

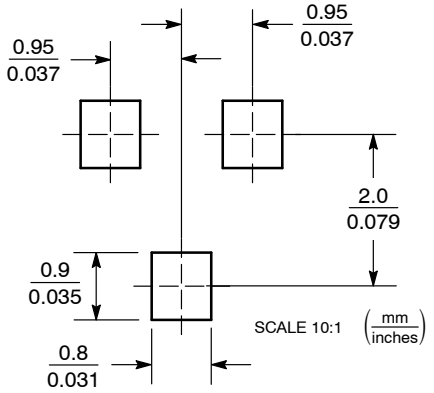


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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