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OT407

Four-quadrant triac, enhanced noise immunity

Rev. 01 — 19 May 2008 Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate triac in a SOT54A (wide pitch) plastic package

1.2 Features

- Sensitive gate
- Direct interfacing to logic level ICs
- Enhanced immunity to voltage transients and noise
- Gate triggering in four quadrants
- Direct interfacing to low power gate drive circuits
- High blocking voltage to 800 V

1.3 Applications

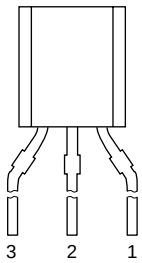
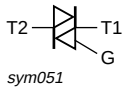
- Home appliances
- Low power AC fan speed controllers
- Low power motor control
- Low power loads in industrial process control

1.4 Quick reference data

- $V_{DRM} \leq 800$ V
- $I_{TSM} \leq 12.5$ A (t = 20 ms)
- $I_{T(RMS)} \leq 1$ A
- $I_{GT} \leq 5$ mA
- $I_{GT} \leq 7$ mA (T2– G+)

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	main terminal 2 (T2)		
2	gate (G)		
3	main terminal 1 (T1)		

SOT54A

sym051

founded by Philips

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
OT407	-	plastic single-ended leaded (through hole) package; 3 leads (wide pitch)	SOT54A

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
V_{RRM}	repetitive peak reverse voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 38$ °C; see Figure 4 and 5	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3			
		t = 20 ms	-	12.5	A
		t = 16.7 ms	-	13.8	A
I^2t	I^2t for fusing	$t_p = 10$ ms	-	1.28	A^2s
dI_T/dt	rate of rise of on-state current	$I_{TM} = 1$ A; $I_G = 20$ mA; $dI_G/dt = 0.2$ A/µs			
		T2+ G+	-	50	A/µs
		T2+ G–	-	50	A/µs
		T2– G–	-	50	A/µs
		T2– G+	-	10	A/µs
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	125	°C

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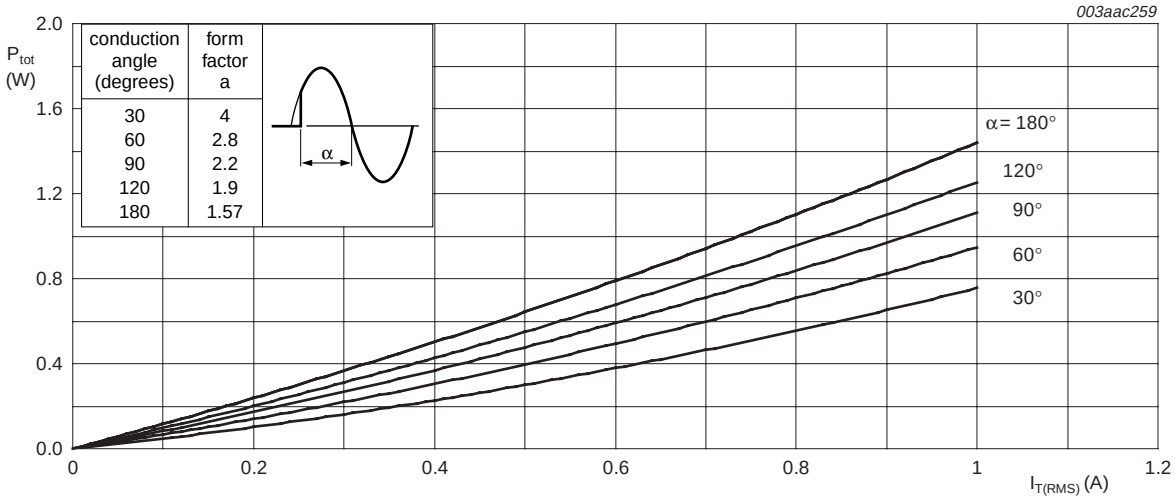
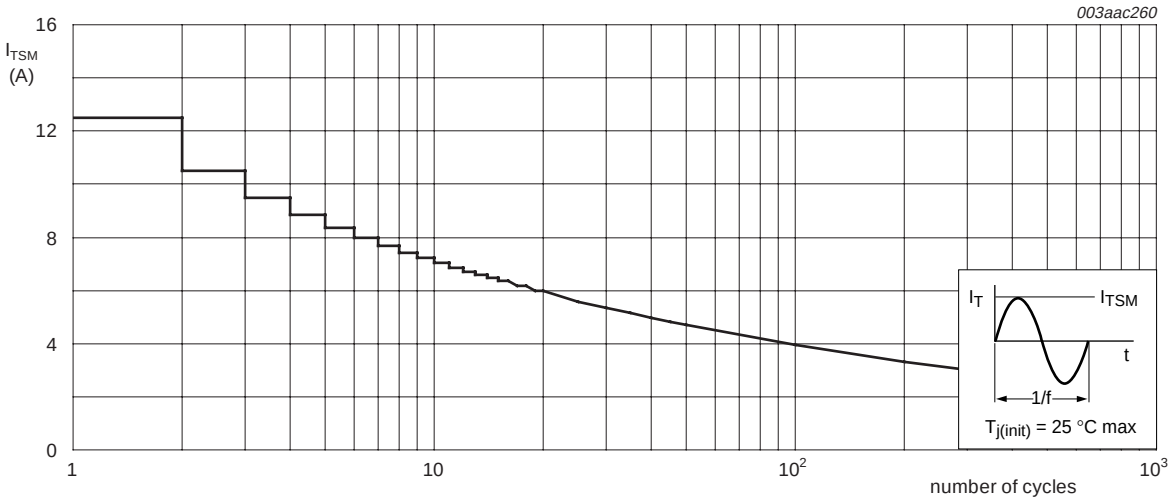


α = conduction angle

Fig 1. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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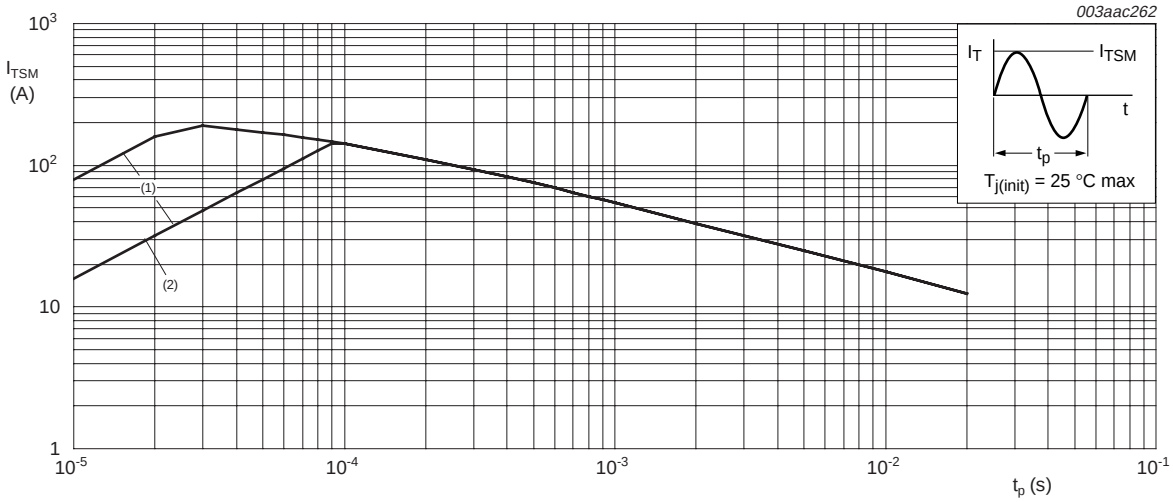
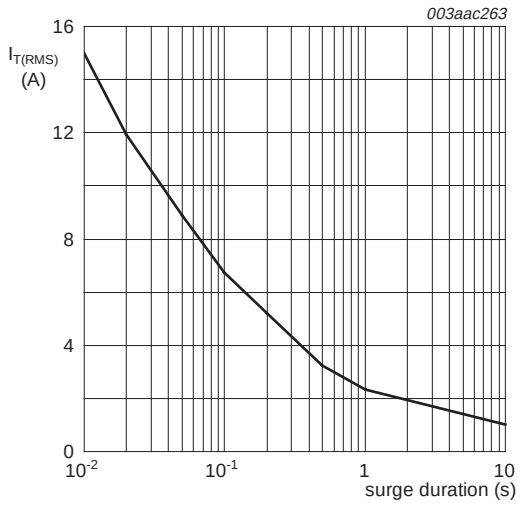


$t_p \leq 20$ ms

(1) dI_T/dt limit

(2) T2– G+ quadrant limit

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values



f = 50 Hz

T_{lead} = 38 °C

Fig 4. RMS on-state current as a function of surge duration; maximum values

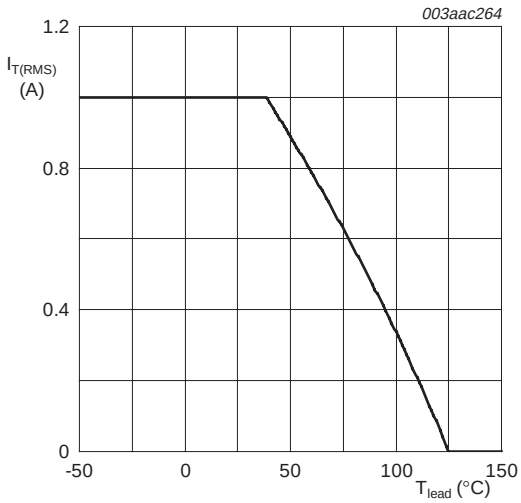


Fig 5. RMS on-state current as a function of solder point temperature; maximum values

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5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	full cycle; see Figure 6	-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W

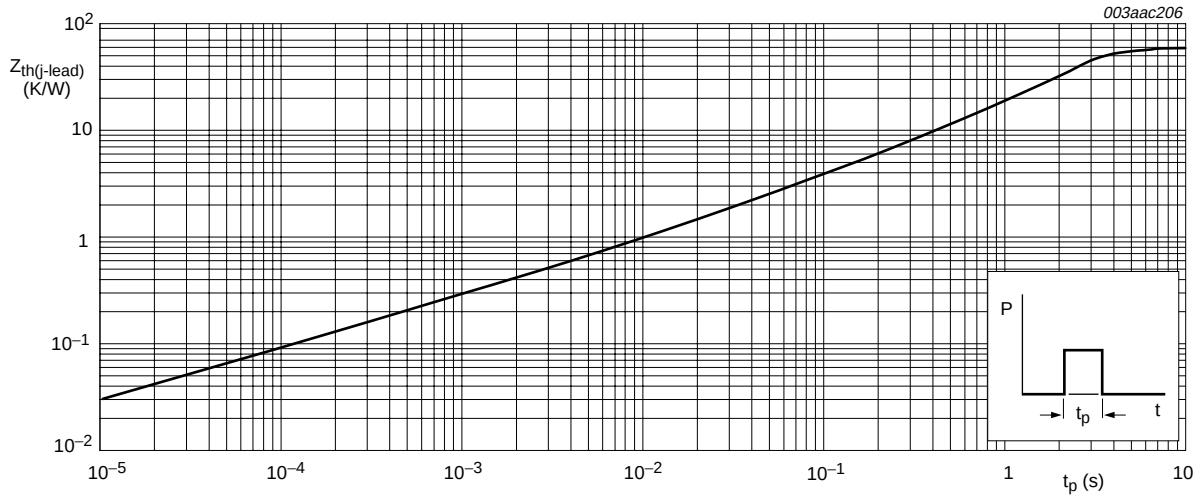

Fig 6. Transient thermal impedance from junction to lead as a function of pulse width

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6. Static characteristics

Table 5. Static characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; see Figure 8				
		T2+ G+	0.25	-	5	mA
		T2+ G–	0.25	-	5	mA
		T2– G–	0.25	-	5	mA
		T2– G+	0.35	-	7	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; see Figure 10				
		T2+ G+	-	-	10	mA
		T2+ G–	-	-	25	mA
		T2– G–	-	-	10	mA
		T2– G+	-	-	10	mA
I_H	holding current	V_D = 12 V; I_G = 0.1 A; see Figure 11	-	-	10	mA
V_T	on-state voltage	I_T = 1 A; see Figure 9	-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; see Figure 7	-	-	1.3	V
		$V_D = V_{DRM}$; I_T = 0.1 A; T_j = 125 °C	0.2	-	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; T_j = 125 °C	-	-	0.5	mA

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7. Dynamic characteristics

Table 6. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 0.67V_{DRM(max)}$; $T_j = 110$ °C; exponential waveform; gate open circuit	20	-	-	V/µs
dV_{com}/dt	rate of change of commutating voltage	$V_{DM} = 400$ V; $T_j = 110$ °C; $I_{TM} = 1$ A; $dI_{com}/dt = 0.44$ A/ms	1	-	-	V/µs

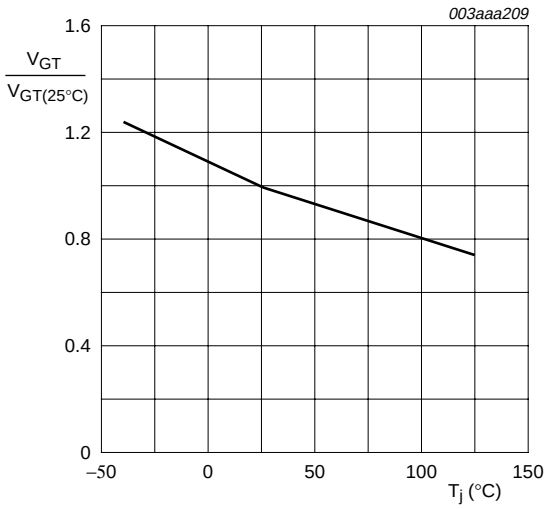
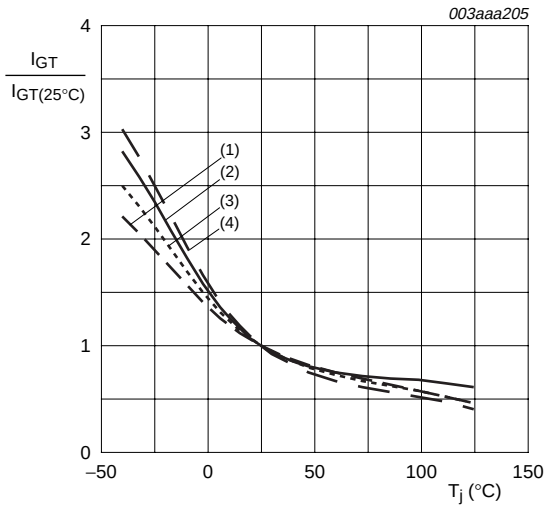


Fig 7. Normalized gate trigger voltage as a function of junction temperature



(1) T2+ G+
(2) T2+ G–
(3) T2– G–
(4) T2– G+

Fig 8. Normalized gate trigger current as a function of junction temperature

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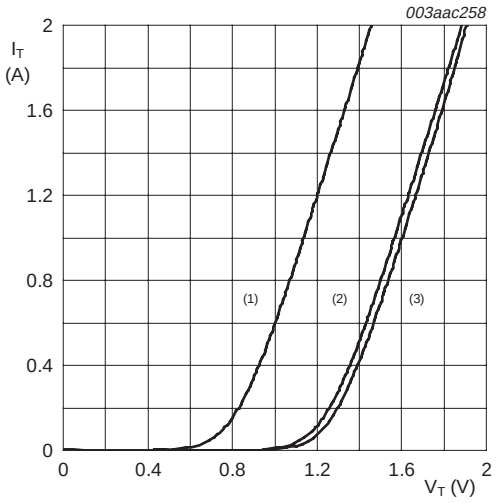

V_o = 1.254 V; R_s = 0.31 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig 9. On-state current as a function of on-state voltage

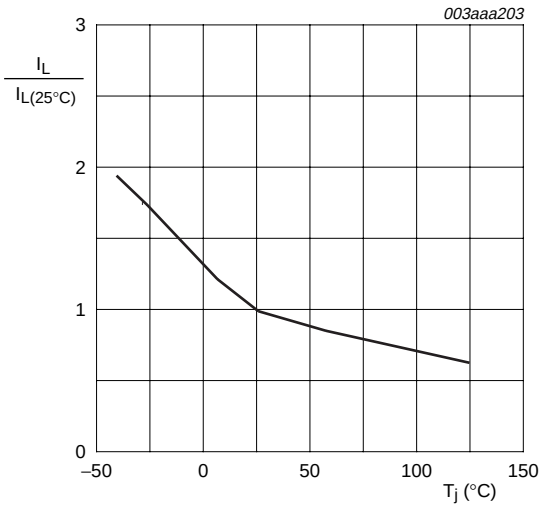

Fig 10. Normalized latching current as a function of junction temperature

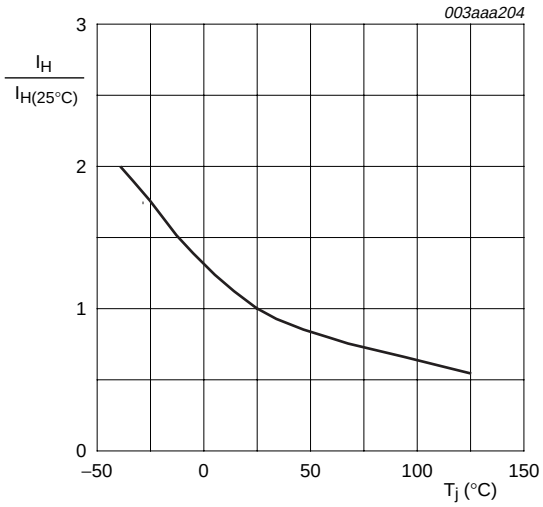

Fig 11. Normalized holding current as a function of junction temperature

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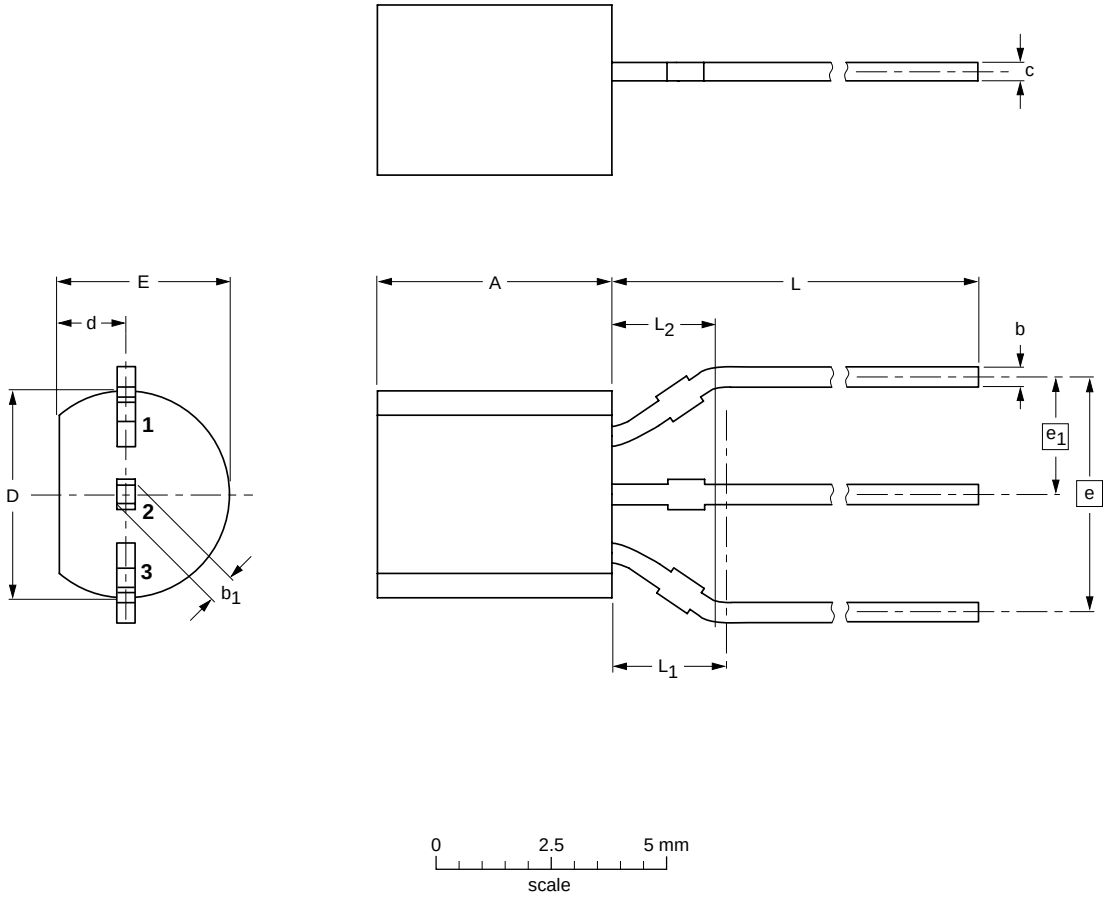
8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch) **SOT54A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.	L_2
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	5.08	2.54	14.5 12.7	3	3 2

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54A						~~97-05-13~~ 04-06-28

Fig 12. Package outline SOT54A

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9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
OT407_1	20080519	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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[2] The term 'short data sheet' is explained in section "Definitions".

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