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ATP AW12P6438BLK0M

4GB DDR3-1600 UNBUFFERED NON-ECC SODIMM

DESCRIPTION

The ATP AW12P6438BLK0M is a high performance 4GB DDR3-1600 Unbuffered NON-ECC SODIMM SDRAM memory module. It is organized as 512M x 64 in a 204-pin Small Outline Dual-In-Line Memory Module (SODIMM) package. The module utilizes eight 512Mx8 DDR3 SDRAMs in FBGA package. The module consists of a 256-byte serial EEPROM, which contains the module configuration information.

KEY FEATURES

- High Density: 4GB (512M x 64)
- DIMM Rank: 1 Rank
- Cycle Time: 1.25ns (800MHz)
- CAS Latency: 11
- Power supply: 1.35V (1.28V~1.45V)
Backward compatible to 1.5V ±0.075V
- Internal self calibration through ZQ
- Burst lengths: 8
- Auto & Self refresh
- Asynchronous Reset
- Minimum Thickness of Golden Finger: 30 Micro-inch
- 7.8 μs refresh interval at lower than T_{CASE} 85°C, 3.9μs refresh interval at 85°C < T_{CASE} < 95 °C
- Dynamic On Die Termination
- Fly-by topology
- PCB Height: 1.18 inches
- RoHS compliant

Part No.	Max Freq	Interface
AW12P6438BLK0M	800MHz (1.25ns@CL=11) x2	SSTL_15

PIN DESCRIPTION

Pin Name	Description	Pin Name	Description
A0~A9, A11~A14	Address Inputs	ODT0	On die termination control
A10/AP	Address Input/Auto precharge	RAS	Row Address Strobe
BA0~BA2	SDRAM Bank Address	CS0	Chip Selects
CAS	Column Address Strobe	SA0~SA1	SPD address
CK0~CK1	Clock Inputs, positive line	SCL	Serial Presence Detect (SPD) Clock Input
CK0 ~ CK1	Clock Inputs, negative line	SDA	SPD Data Input/Output
CKE0	Clock Enables	VDD	Core Power
DM0~DM7	Data Masks	VDDSPD	SPD Power
DQ0~DQ63	Data Input/Output	VSS	Ground
DQS0~DQS7	Data strobes	RESET	This signal resets the DDR3 SDRAM
DQS0 ~ DQS7	Data strobes, negative line	WE	Write Enable
VREFDQ VREFCA	Input/Output Reference	TEST	Logic Analyzer specific test pin (No connect on SO-DIMM)
A12/BC	Address Input/Burst chop	NC	No Connect
VTT	Termination voltage		

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PIN ASSIGNMENT

No.	Designation	No.	Designation	No.	Designation	No.	Designation
1	VREFDQ	2	VSS	105	VDD	106	VDD
3	VSS	4	DQ4	107	A10/AP	108	BA1
5	DQ0	6	DQ5	109	BA0	110	\overline{RAS}
7	DQ1	8	VSS	111	VDD	112	VDD
9	VSS	10	$\overline{DQS0}$	113	\overline{WE}	114	$\overline{CS0}$
11	DM0	12	DQS0	115	\overline{CAS}	116	ODT0
13	VSS	14	VSS	117	VDD	118	VDD
15	DQ2	16	DQ6	119	A13	120	NC
17	DQ3	18	DQ7	121	NC	122	NC
19	VSS	20	VSS	123	VDD	124	VDD
21	DQ8	22	DQ12	125	TEST	126	VREFCA
23	DQ9	24	DQ13	127	VSS	128	VSS
25	VSS	26	VSS	129	DQ32	130	DQ36
27	$\overline{DQS1}$	28	DM1	131	DQ33	132	DQ37
29	DQS1	30	\overline{RESET}	133	VSS	134	VSS
31	VSS	32	VSS	135	$\overline{DQS4}$	136	DM4
33	DQ10	34	DQ14	137	DQS4	138	VSS
35	DQ11	36	DQ15	139	VSS	140	DQ38
37	VSS	38	VSS	141	DQ34	142	DQ39
39	DQ16	40	DQ20	143	DQ35	144	VSS
41	DQ17	42	DQ21	145	VSS	146	DQ44
43	VSS	44	VSS	147	DQ40	148	DQ45
45	$\overline{DQS2}$	46	DM2	149	DQ41	150	VSS
47	DQS2	48	VSS	151	VSS	152	$\overline{DQS5}$
49	VSS	50	DQ22	153	DM5	154	DQS5
51	DQ18	52	DQ23	155	VSS	156	VSS
53	DQ19	54	VSS	157	DQ42	158	DQ46
55	VSS	56	DQ28	159	DQ43	160	DQ47
57	DQ24	58	DQ29	161	VSS	162	VSS
59	DQ25	60	VSS	163	DQ48	164	DQ52
61	VSS	62	$\overline{DQS3}$	165	DQ49	166	DQ53
63	DM3	64	DQS3	167	VSS	168	VSS
65	VSS	66	VSS	169	$\overline{DQS6}$	170	DM6
67	DQ26	68	DQ30	171	DQS6	172	VSS
69	DQ27	70	DQ31	173	VSS	174	DQ54
71	VSS	72	VSS	175	DQ50	176	DQ55
				177	DQ51	178	VSS
73	CKE0	74	NC	179	VSS	180	DQ60
75	VDD	76	VDD	181	DQ56	182	DQ61
77	NC	78	A15 ¹	183	DQ57	184	VSS
79	BA2	80	A14 ¹	185	VSS	186	$\overline{DQS7}$
81	VDD	82	VDD	187	DM7	188	DQS7
83	A12/ \overline{BC}	84	A11	189	VSS	190	VSS
85	A9	86	A7	191	DQ58	192	DQ62
87	VDD	88	VDD	193	DQ59	194	DQ63
89	A8	90	A6	195	VSS	196	VSS
91	A5	92	A4	197	SA0	198	NC
93	VDD	94	VDD	199	VDDSPD	200	SDA
95	A3	96	A2	201	SA1	202	SCL
97	A1	98	A0	203	VTT	204	VTT
99	VDD	100	VDD				
101	CK0	102	CK1				
103	CK0	104	CK1				

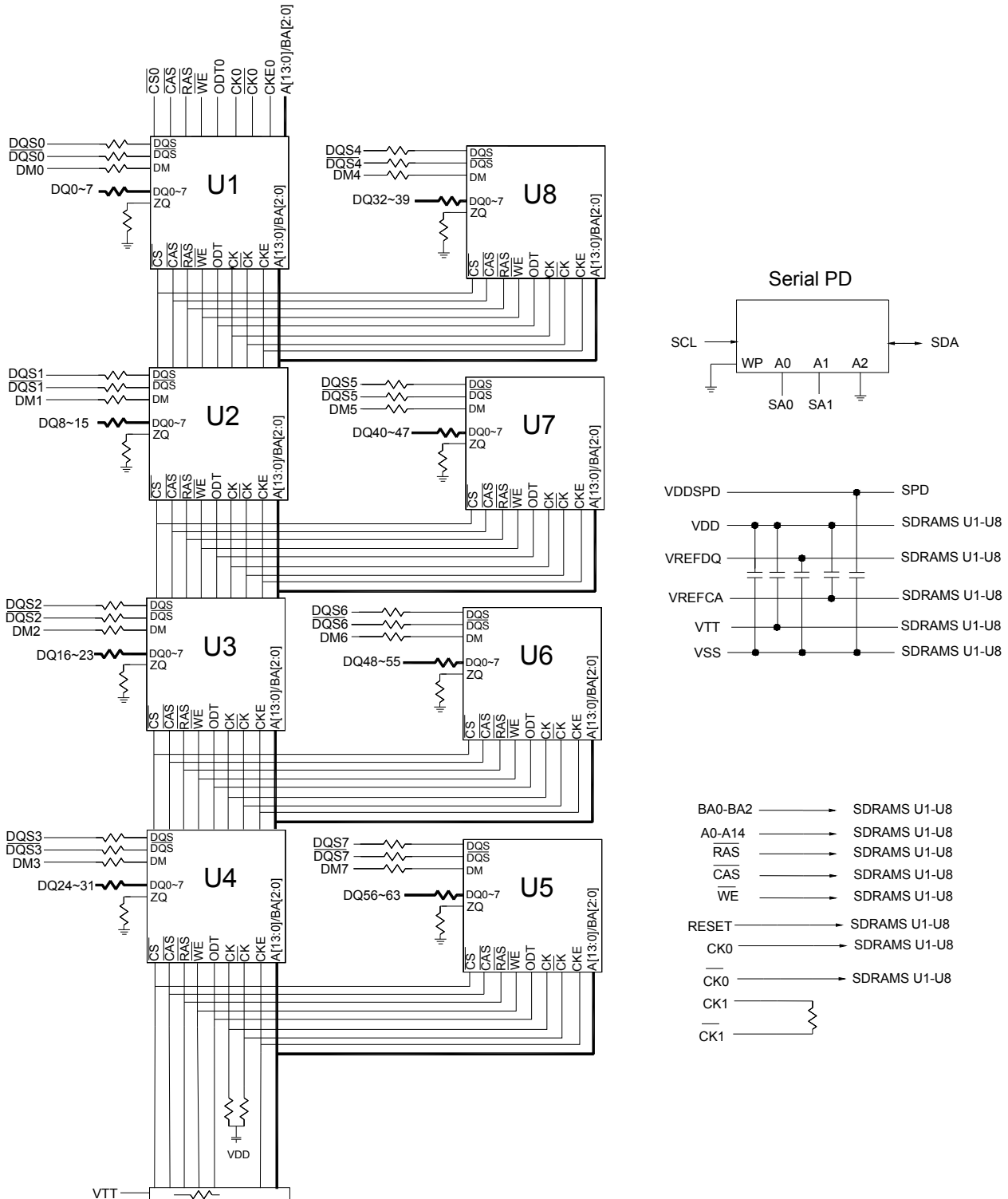
Notes: 1. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

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FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM DC RATINGS

Item	Symbol	Rating	Units	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.4V ~ 1.975V	V	1
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.4V ~ 1.975V	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4V ~ 1.975V	V	1
Storage Temperature	T_{STG}	-55 to +100	°C	1
Operating Temperature	T_{CASE}	0 to +95	°C	1,2,3

Note:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. It is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (Refresh interval =3.9 μ s) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

AC & DC OPERATING CONDITIONS (SSTL- 15)

Recommended operating conditions

Item	Symbol	Min.	Typical	Max.	Units
Supply Voltage	V_{DD}	1.283	1.35	1.45	V
Supply Voltage for Output ⁴	V_{DDQ}	1.283	1.35	1.45	V
$V_{REFCA}(DC)$ ^{1,2}	I/O	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	V
$V_{REFDQ}(DC)$ ^{1,2}	I/O	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	V
Input High Voltage (DC)	$V_{IH}(DC)$	$V_{REF} + 0.090$	-	V_{DD}	V
Input High Voltage (AC)	$V_{IH}(AC)$	$V_{REF} + 0.135$	-	-	V
Input Low Voltage (DC)	$V_{IL}(DC)$	V_{SS}	-	$V_{REF} - 0.090$	V
Input Low Voltage (AC)	$V_{IL}(AC)$	-	-	$V_{REF} - 0.135$	V

Note:

1. The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ} .
2. Peak to peak AC noise on V_{REF} may not exceed $\pm 2\%$ $V_{REF}(DC)$.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.
4. AC parameters are measured with V_{DD} , V_{DDQ} and V_{DDL} tied together.

RELIABILITY

MTBF @25 °C (Hours) ¹	FIT @ 25 °C ²	MTBF @40 °C (Hours) ¹	FIT @ 40 °C ²
12,870,000	77	6,982,000	143

Note:

1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Bellcore Prediction, which based on reliability data of the individual components in the module. It assumes nominal voltage, with all other parameters within specified range.
2. Failures per Billion Device-Hours

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IDD SPECIFICATION PARAMETER & POWER CONSUMPTION

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Value	Units
IDD0	Operating one bank active-precharge current; CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Timing table ; BL: 8; AL: 0/ CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	230	mA
IDD1	Operating one bank active-read-precharge current; CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Timing table ; BL: 8; AL: 0; /CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	350	mA
IDD2P0	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit	80	mA
IDD2P1	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Timing table; BL: 8); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit	90	mA
IDD2N	Precharge standby current; CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog-pling; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	130	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog-pling ; Data IO: FLOATING;DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers	160	mA
IDD2Q	Precharge quiet standby current; CKE: High; External clock: On; tCK, CL: see Timing table; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	120	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	120	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: partially tog-pling ; Data IO: FLOATING; DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	160	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Timing table; BL: 8; AL: 0; /CS: High between RD; Command, Address, Bank Address Inputs: par-tially toggling ; Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	720	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Timing table ; BL: 8; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: par-tially toggling ; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,....; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH;	810	mA
IDD5B	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Timing table ; BL: 8; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: FLOATING;DM:stable at 0; Bank Activity: REF command every nRFC; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	1,220	mA
IDD6	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled; Self-Refresh Temperature Range (SRT): Normale); CKE: Low; External clock: Off; CK and CK: LOW; CL: see Timing table ; BL: 8; AL: 0; /CS, Command, Address, Bank Address, Data IO: FLOATING;DM:stable at 0; Bank Activity: Self- Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2); ODT Signal: FLOATING	120	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Timing table ; BL: 8; AL: CL-1; /CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one ; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0;	1,040	mA
PDIMM	Power Consumption per DIMM System is operating at 800 MHz clock with VDD = 1.35V. This parameter is calculated at a common loading.	1,650	mW

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TIMING PARAMETER

Parameter	Symbol	DDR3-1600		Units
		min	Max	
Clock cycle time at CL=11, CWL=8	tCK	1.25	<1.5	ns
Internal read command to first data	tAA	13.75(13.125 ²)	20	ns
ACT to internal read or write delay time	tRCD	13.75(13.125 ²)		ns
PRE command period	tRP	13.75(13.125 ²)		ns
ACT to ACT or REF command period	tRC	48.75(48.125 ²)		ns
ACTIVE to PRECHARGE command period	tRAS	35	9*tREFI	ns
Average high pulse width	tCH(avg)	0.47	0.53	tCK
Average low pulse width	tCL(avg)	0.47	0.53	tCK
DQS, \overline{DQS} to DQ skew, per group, per access	tDQSQ		100	ps
DQ output hold time from DQS, \overline{DQS}	tQH	0.38		tCK
DQ low-impedance time from CK, \overline{CK}	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, \overline{CK}	tHZ(DQ)		225	ps
Data setup time to DQS, \overline{DQS} referenced to Vih(ac)/Vil(ac) levels	tDS(base)	10		ps
Data hold time to DQS, \overline{DQS} referenced to Vih(ac)/Vil(ac) levels	tDH(base)	45		ps
DQS, \overline{DQS} READ Preamble	tRPRE	0.9	-	tCK
DQS, \overline{DQS} differential READ Postamble	tRPST	0.3		tCK
DQS, \overline{DQS} output high time	tQSH	0.4	-	tCK
DQS, \overline{DQS} output low time	tQSL	0.4	-	tCK
DQS, \overline{DQS} WRITE Preamble	tWPRE	0.9	-	tCK
DQS, \overline{DQS} WRITE Postamble	tWPST	0.3	-	tCK
DQS, \overline{DQS} rising edge output access time from rising CK, \overline{CK}	tDQSCK	-225	225	ps
DQS, \overline{DQS} low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	ps
DQS, \overline{DQS} high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	ps
DQS, \overline{DQS} differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, \overline{DQS} differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, \overline{DQS} rising edge to CK, \overline{CK} rising edge	tDQSS	-0.27	0.27	tCK
DQS, \overline{DQS} falling edge setup time to CK, \overline{CK} rising edge	tDSS	0.18	-	tCK
DQS, \overline{DQS} falling edge hold time to CK, \overline{CK} rising edge	tDSH	0.18	-	tCK
DLL locking time	tDLLK	512		nCK ¹
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)		
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK,7.5ns)		
WRITE recovery time	tWR	15		ns
Mode Register Set command cycle time	tMRD	4		nCK ¹
Mode Register Set command update delay	tMOD	max(12nCK,15ns)		
CAS to \overline{CAS} command delay	tCCD	4		nCK ¹
Auto precharge write recovery + precharge time	tDAL	tWR + roundup (tRP / tCK)		nCK ¹
Multi-Purpose Register Recovery Time	tMPRR	1		nCK ¹
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK,6ns)		
Four activate window for 1KB page size	tFAW	30		ns
Command and Address setup time to CK, \overline{CK} referenced to Vih(ac) / Vil(ac) levels	tIS(base)	45		ps
Command and Address hold time from CK, \overline{CK} referenced to Vih(ac) / Vil(ac) levels	tIH(base)	120		ps
Power-up and RESET calibration time	tZQinitl	512		nCK ¹
Normal operation Full calibration time	tZQoper	256		nCK ¹
Normal operation short calibration time	tZQCS	64		nCK ¹
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK,tRFC+10ns)		
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK,6ns)		
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOPFD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	tCK
RTT dynamic change skew	tADC	0.3	0.7	tCK
2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	160		ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)	tREFI	7.8	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)	tREFI	3.9	3.9	us
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC+10ns)		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)		nCK ¹
Power Down Entry to Exit Timing	tPD	tCK(min)	60ms	tCK
Write leveling output delay	tWLO	0	7.5	ns
Write leveling output error	tWLOE	0	2	ns

1:Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

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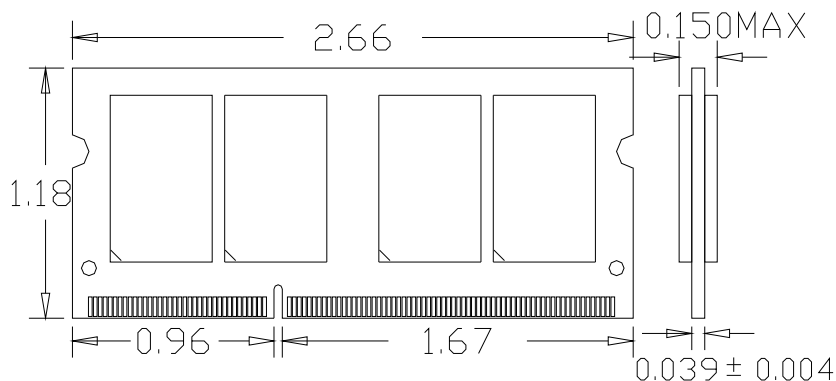
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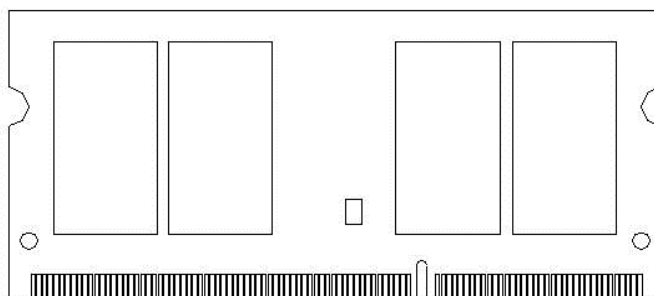
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204-pin DIMM

Front



Back



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